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NCP5209

4-In-1 PWM Buck and Tri-Linear Power Controller

The NCP5209 4−In−1 PWM Buck and Tri−Linear Power Controller is a complete ACPI compliant power solution for MCH and DDR memory. This IC combines the high efficiency of a PWM controller for the VDDQ supply with the simplicity of linear regulator for the VTT termination voltage as well as the MCH core supply voltage.

This IC contains a synchronous PWM buck controller for driving two external N−Ch FETs to form the DDR memory supply voltage (VDDQ). The DDR memory termination regulator (VTT) is designed to track at the half of reference voltage while sourcing and sinking current. The two linear regulator controllers driving two external N−Ch FETs are cascaded to produce the MCH core voltage (VMCH).

Protective features include, soft−start circuitry, undervoltage monitoring of 5VDUAL, 5VATX and 12VATX, and thermal shutdown. The device is housed in a thermal enhanced space−saving QFN−20 package.

Features

- Synchronous PWM Buck Controller for VDDQ
- Integrated Power FETs in VTT Regulator Source/Sink up to 2.0 A
- Two Linear Regulator Drivers for VMCH
- All External Power MOSFETs are N−Channel
- Adjustable VDDQ and VMCH by External Dividers
- VTT Tracks at Half of Reference Voltage or can be Adjusted Externally
- Fixed Switching Frequency of 250 kHz for DDQ Regulator in Normal Mode
- Doubled Switching Frequency of 500 kHz for DDQ Regulator in Standby Mode to Optimize Inductor Current Ripple and Efficiency
- Soft−Start Protection for all Regulators
- Undervoltage Monitoring of Supply Voltages
- Overcurrent Protection for DDQ and VTT Regulators
- Fully Complies with ACPI Power Sequencing Specifications
- Short Circuit Protection Prevents Damage to Power Supply Due to Reverse DIMM Insertion
- Thermal Shutdown
- 5x6 QFN−20 Package

Applications

- DDR I and DDR II Memory and MCH Power Supply

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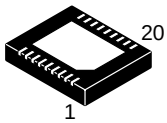
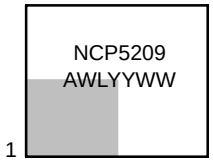


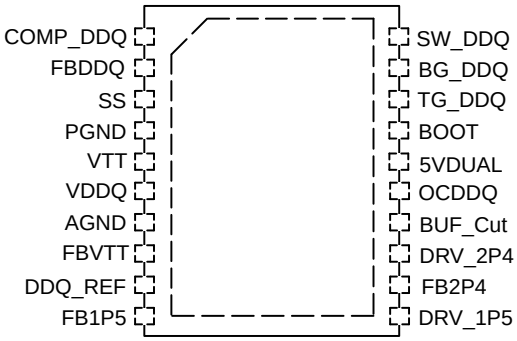
QFN−20
MN SUFFIX
CASE 505AB

MARKING DIAGRAM



NCP5209 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN CONNECTIONS



NOTE: Pin 21 is the thermal pad on the bottom of the device.

ORDERING INFORMATION

Device	Package	Shipping†
NCP5209MNR2	6x5 mm QFN−20	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

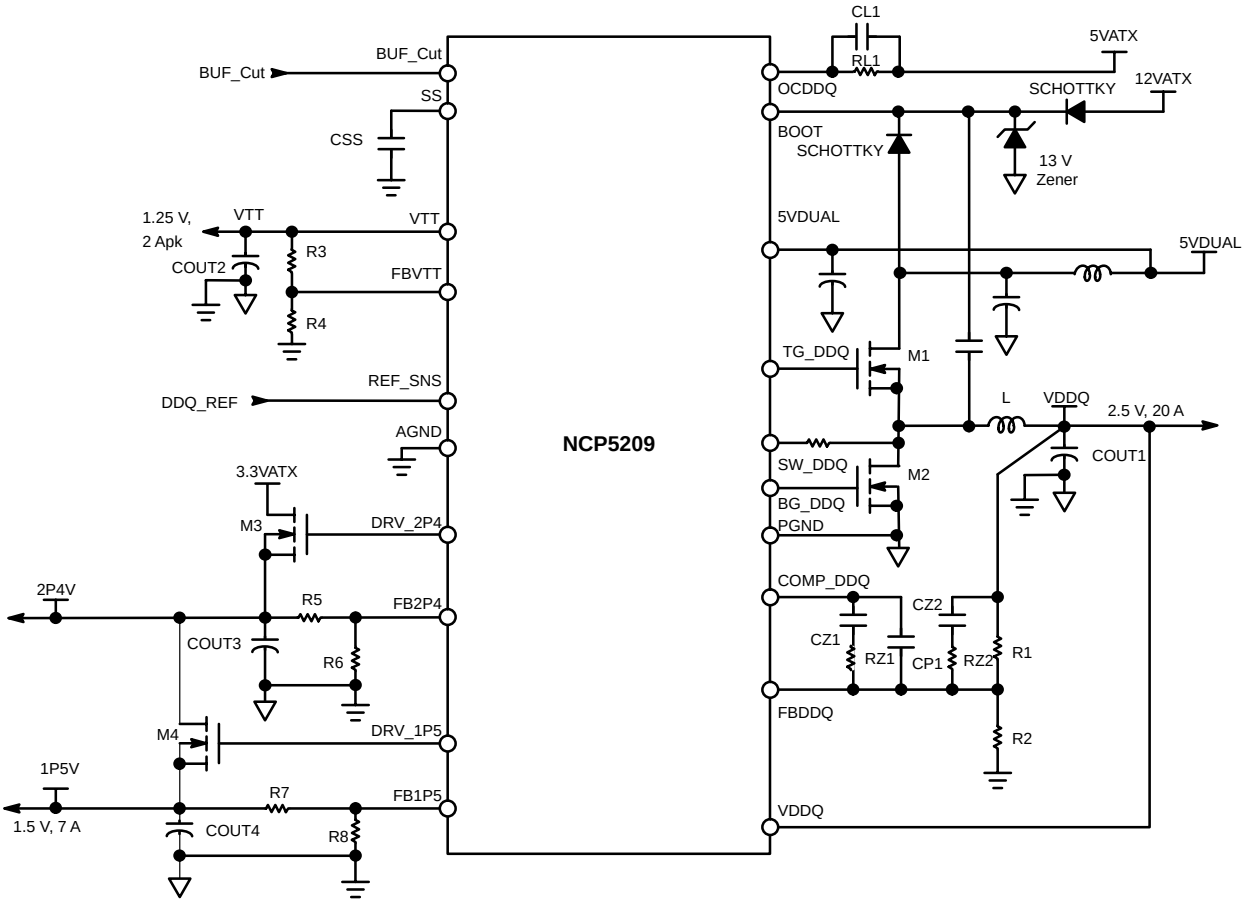


Figure 1. Application Diagram

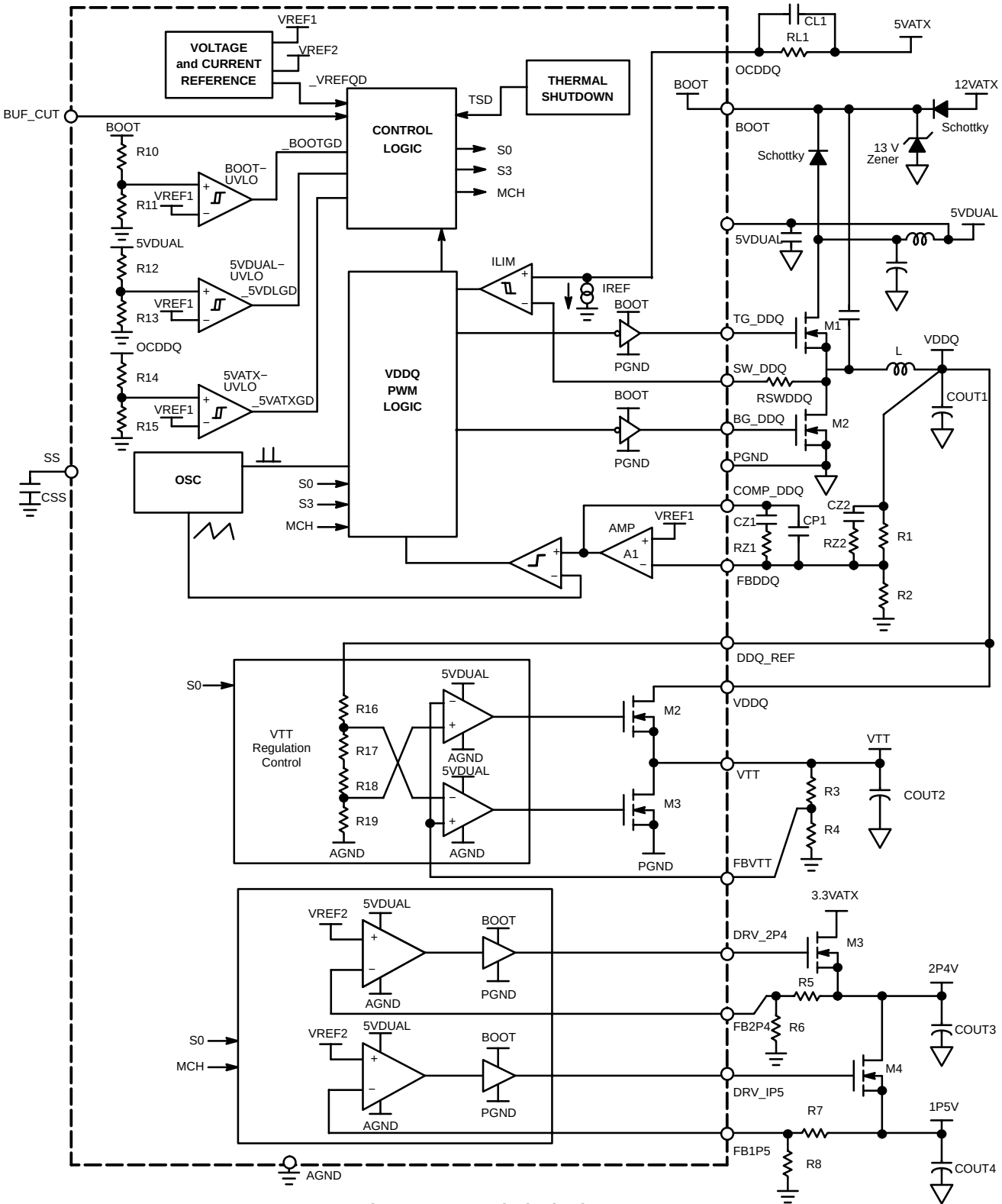


Figure 2. Internal Block Diagram

PIN DESCRIPTION

Pin	Symbol	Descriptions
1	COMP	VDDQ error amplifier compensation node.
2	FBDDQ	DDQ regulator feedback pin.
3	SS	Soft−start pin of DDQ.
4	PGND	Power ground.
5	VTT	VTT regulator output.
6	VDDQ	Power input for VTT linear regulator.
7	AGND	Analog ground connection and remote ground sense.
8	FBVTT	VTT linear regulator pin for closed loop regulation.
9	DDQ_REF	Reference voltage input of VTT regulator.
10	FB1P5	2nd linear regulator pin for closed loop regulation.
11	DRV_1P5	2nd linear regulator gate driver output for N−channel power FET.
12	FB2P4	1st linear regulator pin for closed loop regulation.
13	DRV_2P4	1st linear regulator gate driver output for N−channel power FET.
14	BUF_CUT	Active high control signal to activate S3 sleep state.
15	OCDDQ	Dual function I/O pin for overcurrent sensing as well as programming input of the high side FET of DDQ regulator, which is also monitored by undervoltage lock out circuitry.
16	5VDUAL	5.0 V dual supply input, which is monitored by undervoltage lock out circuitry.
17	BOOT	Gate drivers input supply, which is monitored by undervoltage lock out circuitry, and a boost capacitor is connected between SWDDQ and this pin.
18	TG_DDQ	Gate driver output for DDQ regulator high side N−channel power FET.
19	BG_DDQ	Gate driver output for DDQ regulator low side N−channel power FET.
20	SW_DDQ	DDQ regulator switch node and current limit sense input.
21	TH_PAD	Copper pad on bottom of IC used for heatsinking. This pin should be connected to the ground plane under the IC.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 16) to AGND (Pin 7)	5VDUAL	−0.3, 6.0	V
Gate Drive (Pins 11, 13), BOOT (Pin 17) to AGND (Pin 7)	Vs	−0.3, 14	V
Gate Drive (Pins 18, 19) to AGND (Pin 7)	Vg	−0.3 DC, −4.0 for $<$100 ns; 14	V
Input/Output Pins to AGND (Pin 7) Pins 1−3, 5−6, 8−10, 12, 14−15, 20	V_{IO}	−0.3, 6.0	V
PGND (Pin 4) to AGND (Pin 7)	V_{GND}	−0.3, 0.3	V
Thermal Characteristics QFN−20 Plastic Package Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	35	°C/W
Operating Junction Temperature Range	T_J	0 to +150	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	− 55 to +150	°C
Moisture Sensitivity Level	MSL	2.0	

1. This device series contains ESD protection and exceeds the following tests: Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22–A114. Machine Model (MM) ±200 V per JEDEC standard: JESD22–A115. Except 11 and 13 pins, which are ±150 V.
2. Latch–up Current Maximum Rating: ±150 mA per JEDEC standard: JESD78.

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS (5VDUAL = 5.0 V, BOOT = 12 V, 5VATX = 5.0 V, DDQ_REF = 2.5 V, T_A = 0 to 70°C, L = 1.7 μH, COUT1 = 3770 μF, COUT2 = 470 μF, COUT3 = 680 μF, COUT4 = 3300 μF, CSS = 33 nF, RL1 = 50 kΩ, R1 = 2.2 kΩ, R2 = 2.0 kΩ, R3 = 0 Ω, R4 = 1.0 kΩ, R5 = 10 kΩ, R6 = 5.0 kΩ, R7 = 6.8 kΩ, R8 = 7.5 kΩ, RSWDDQ = 1.0 kΩ, RZ1 = 20 kΩ, RZ2 = 8.0 Ω, CP1 = 10 nF, CZ1 = 6.8 nF, CZ2 = 100 nF, for min/max values unless otherwise noted.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
SUPPLY VOLTAGE						
5VDUAL Operating Voltage	V5VDUAL	(Note 3)	4.5	5.0	5.5	V
OCDDQ Operating Voltage	VOCDDQ	(Note 3)	−	5.0	5.5	V
BOOT Operating Voltage	VBOOT	(Note 3)	−	12	13.2	V
SUPPLY CURRENT						
S0 Mode Supply Current from 5VDUAL	I5VDL_S0	BUF_CUT = LOW, BOOT = 12 V, 5VATX = 5.0 V	−	−	8.0	mA
S3 Mode Supply Current from 5VDUAL	I5VDL_S3	BUF_CUT = HIGH, 5VATX = 0 V	−	−	5.0	mA
S5 Mode Supply Current from 5VDUAL	I5VDL_S5	BUF_CUT = LOW, 5VATX = 0 V	−	−	1.0	mA
S0 Mode Supply Current from BOOT	IBOOT_S0	BUF_CUT = LOW, BOOT = 12 V, 5VATX = 5.0 V	−	−	50	mA
S3 Mode Supply Current from BOOT	IBOOT_S3	BUF_CUT = HIGH, 5VATX = 0 V	−	−	25	mA
UNDERVOLTAGE MONITOR						
5VDUAL UVLO Upper Threshold	V5VDLUV+	−	−	−	4.4	V
5VDUAL UVLO Hysteresis	V5VDLhys	−	−	300	−	mV
BOOT UVLO Upper Threshold	VBOOTUV+	−	−	−	10.3	V
BOOT UVLO Hysteresis	VBOOThys	−	−	1.0	−	V
OCDDQ UVLO Upper Threshold	OCDDQUV+	−	−	−	1.5	V
OCDDQ UVLO Hysteresis	OCDDQhys	−	−	200	−	mV
THERMAL SHUTDOWN						
Thermal Shutdown	Tsd	(Note 3)	−	145	−	°C
Thermal Shutdown Hysteresis	Tsdhys	(Note 3)	−	25	−	°C
DDQ SWITCHING REGULATOR						
FBDDQ Feedback Voltage, Control Loop in Regulation	VFBQ	T_A = 25°C T_A = 0 to 70°C	1.178 1.166	1.190	1.202 1.214	V
Feedback Input Current	IDDQfb	V(FBDDQ) = 1.3 V	−	−	1.0	μA
Oscillator Frequency in S0 Mode	FDDQS0	−	217	250	283	kHz
Oscillator Frequency in S3 Mode	FDDQS3	−	434	500	566	kHz
Oscillator Ramp Amplitude	dVOSC	(Note 3)	−	1.3	−	Vp−p
OCDDQ Pin Current Sink	IOCDDQ	V(OCDDQ) = 3.0 V	28	40	52	μA
Current Limit Blanking Time in S0 Mode	TDDQbk	(Note 3)	400	−	−	ns
Minimum Duty Cycle in S0 Mode	DS0min	(Note 3)	0	−	−	%
Maximum Duty Cycle in S0 Mode	DS0max	(Note 3)	−	−	100	%
Minimum Duty Cycle in S3 Mode	DS3min	(Note 3)	0	−	−	%
Maximum Duty Cycle in S3 Mode	DS3max	−	−	−	90	%
Soft−Start Pin Current for DDQ	Iss1	V(SS) = 0 V		2.0		μA

3. Guarantee by design, not tested in production.

ELECTRICAL CHARACTERISTICS (5VDUAL = 5.0 V, BOOT = 12 V, 5VATX = 5.0 V, DDQ_REF = 2.5 V, T_A = 0 to 70°C, L = 1.7 μH, COUT1 = 3770 μF, COUT2 = 470 μF, COUT3 = 680 μF, COUT4 = 3300 μF, CSS = 33 nF, RL1 = 50 kΩ, R1 = 2.2 kΩ, R2 = 2.0 kΩ, R3 = 0 Ω, R4 = 1.0 kΩ, R5 = 10 kΩ, R6 = 5.0 kΩ, R7 = 6.8 kΩ, R8 = 7.5 kΩ, RSWDDQ = 1.0 kΩ, RZ1 = 20 kΩ, RZ2 = 8.0 Ω, CP1 = 10 nF, CZ1 = 6.8 nF, CZ2 = 100 nF, for min/max values unless otherwise noted.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
DDQ ERROR AMPLIFIER						
DC Gain	GAINDDQ	(Note 4)	−	70	−	dB
Gain−Bandwidth Product	GBWDDQ	COMP PIN to GND = 220 nF, 1.0 Ω in Series (Note 4)	−	12	−	MHz
Slew Rate	SRDDQ	COMP_DDQ = 10 pF	−	8.0	−	V/μs
VTT ACTIVE TERMINATION REGULATOR						
VTT Tracking REF_SNS/2 at S0 Mode	dVTTS0	IOUT= 0 to 2.0 A (Sink Current) IOUT= 0 to –2.0 A (Source Current)	−30	−	30	mV
VTT Source Current Limit	ILIMVTsrc	−	2.0	−	−	A
VTT Sink Current Limit	ILIMVTsnk	−	2.0	−	−	A
DDQ_REF Input Resistance	RDDQ_REF	−	−	50	−	kΩ
DUAL LINEAR REGULATOR CONTROLLER						
1st Regulator Feedback Voltage, Control Loop in Regulation	VFB2P4	T_A = 0°C to 70°C	0.784	0.800	0.816	V
1st Regulator Feedback Input Current	IFB2P4	−	−	−	1.0	μA
1st Regulator DC Gain	GAIN2P4	(Note 4)	−	66	−	dB
2nd Regulator Feedback Voltage, Control Loop in Regulation	VFB1P5	T_A = 0°C to 70°C	0.784	0.800	0.816	V
2nd Regulator Feedback Input Current	IFB1P5	−	−	−	1.0	μA
2nd Regulator DC Gain	GAIN1P5	(Note 4)	−	66	−	dB
Internal Soft−Start Timing	Tss2	−	−	1.5	−	ms
CONTROL SECTION						
BUF_CUT Input Logic HIGH	Logic_H	−	2.0	−	−	V
BUF_CUT Input Logic LOW	Logic_L	−	−	−	0.8	V
BUF_CUT Input Current	ILogic	−	−	−	1.0	μA
GATE DRIVERS						
TGDDQ Gate Pull−HIGH Resistance	RH_TG	BOOT = 12 V, V(TGDDQ) = 11.9 V	−	3.0	−	Ω
TGDDQ Gate Pull−LOW Resistance	RL_TG	BOOT = 12 V, V(TGDDQ) = 0.1 V	−	2.5	−	Ω
BGDDQ Gate Pull−HIGH Resistance	RH_BG	BOOT = 12 V, V(BGDDQ) = 11.9 V	−	3.0	−	Ω
BGDDQ Gate Pull−LOW Resistance	RL_BG	BOOT = 12 V, V(BGDDQ) = 0.1 V	−	1.3	−	Ω
DRV_2P4 Gate Pull−HIGH Voltage	VH2P4	BOOT = 12 V	−	9.0	−	V
DRV_2P4 Gate Pull−LOW Voltage	VL2P4	BOOT = 12 V	−	0.8	−	V
DRV_2P4 Gate Source Current	IH2P4	BOOT = 12 V	−	10	−	mA
DRV_2P4 Gate Sink Current	IL2P4	BOOT = 12 V	−	10	−	mA
DRV_1P5 Gate Pull−HIGH Voltage	VH1P5	BOOT = 12 V	−	9.0	−	V
DRV_1P5 Gate Pull−LOW Voltage	VL1P5	BOOT = 12 V	−	0.8	−	V
DRV_1P5 Gate Source Current	IH1P5	BOOT = 12 V	−	10	−	mA
DRV_1P5 Gate Sink Current	IL1P5	BOOT = 12 V	−	10	−	mA

4. Guarantee by design, not tested in production.

TYPICAL OPERATING CHARACTERISTICS

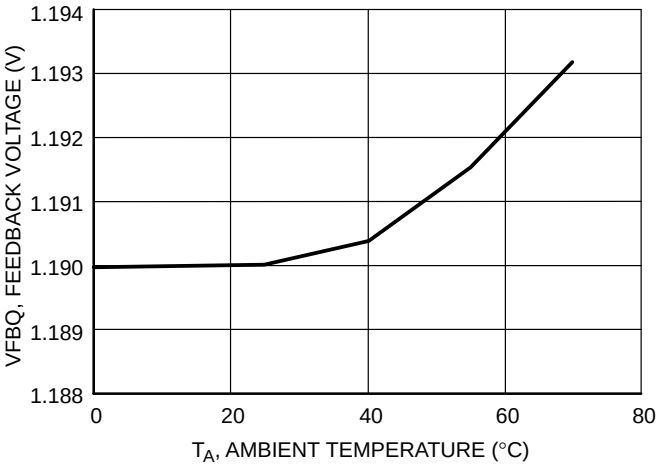


Figure 3. VFBQ Feedback Voltage vs. Ambient Temperature

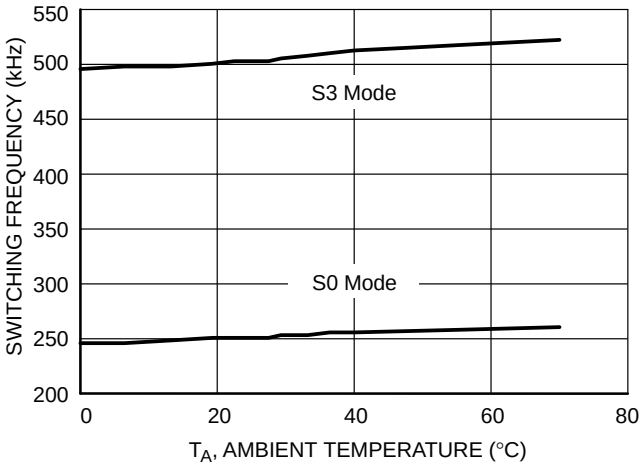


Figure 4. Oscillation Frequency in S0/S3 vs. Ambient Temperature

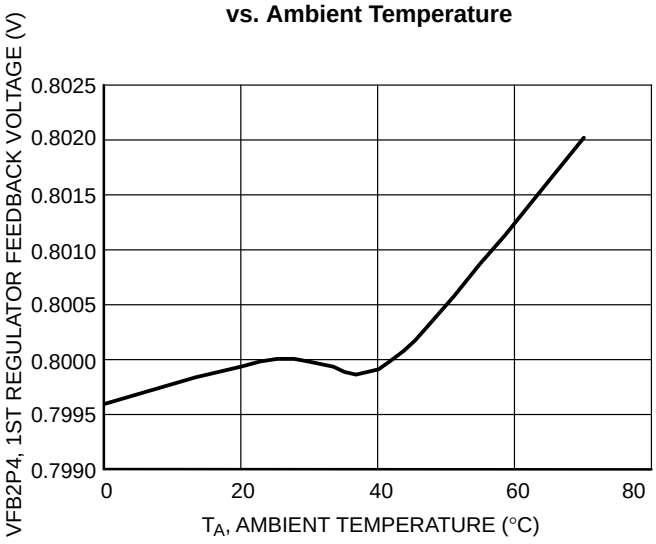


Figure 5. VFB2P4 1st Regulator Feedback Voltage vs. Ambient Temperature

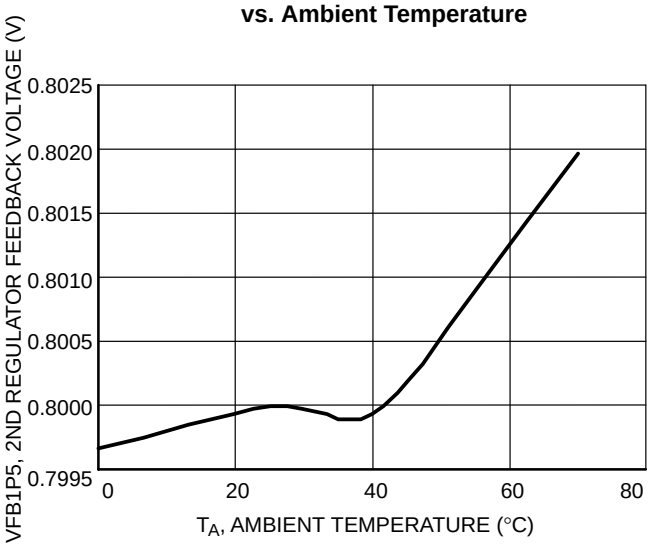


Figure 6. VFB1P5 2nd Regulator Feedback Voltage vs. Ambient Temperature

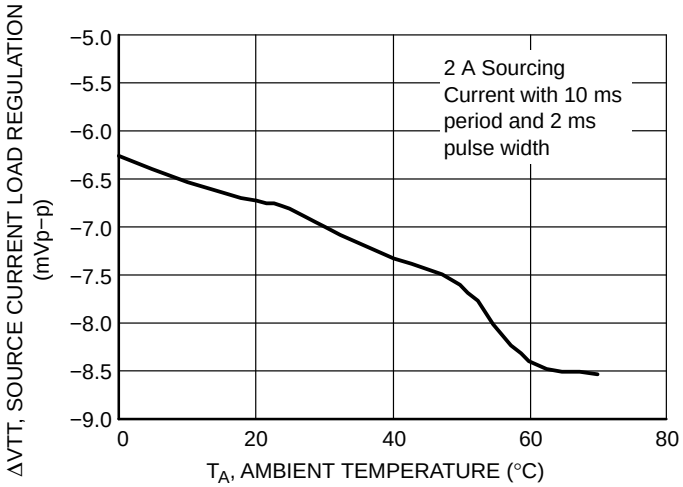


Figure 7. VTT Source Current Load Regulation vs. Ambient Temperature

TYPICAL OPERATING CHARACTERISTICS

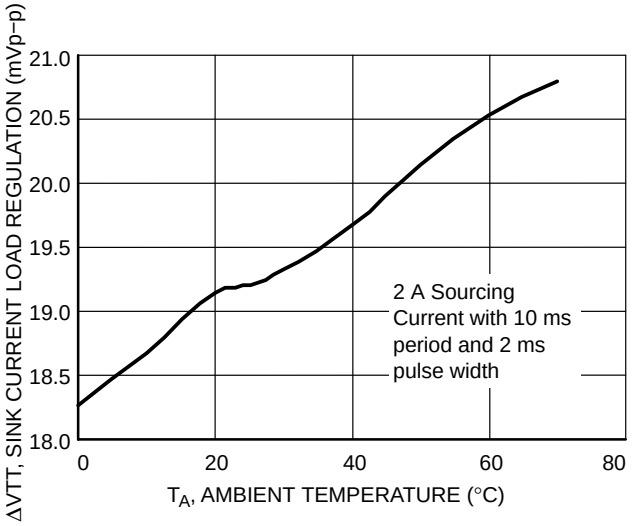


Figure 8. VTT Sink Current Load Regulation vs. Ambient Temperature

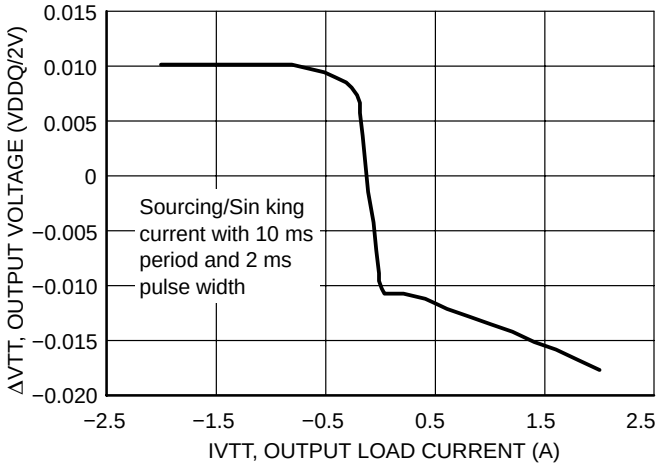
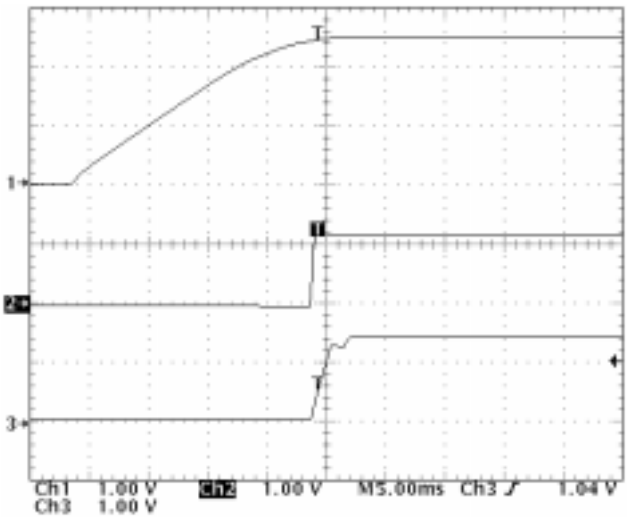


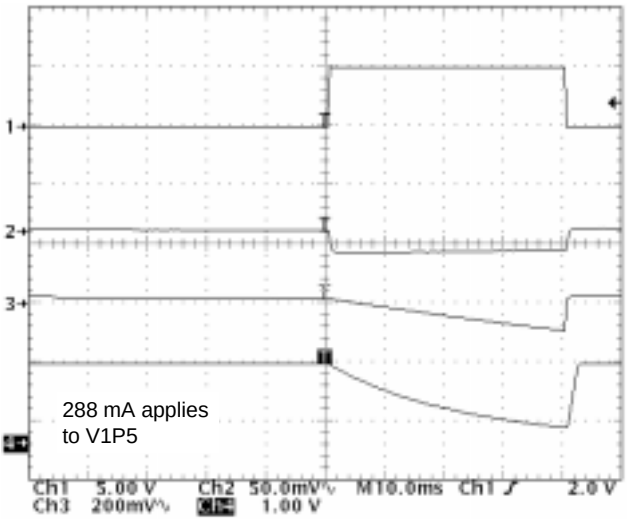
Figure 9. VTT Output Voltage vs. Load Current

TYPICAL OPERATING WAVEFORMS



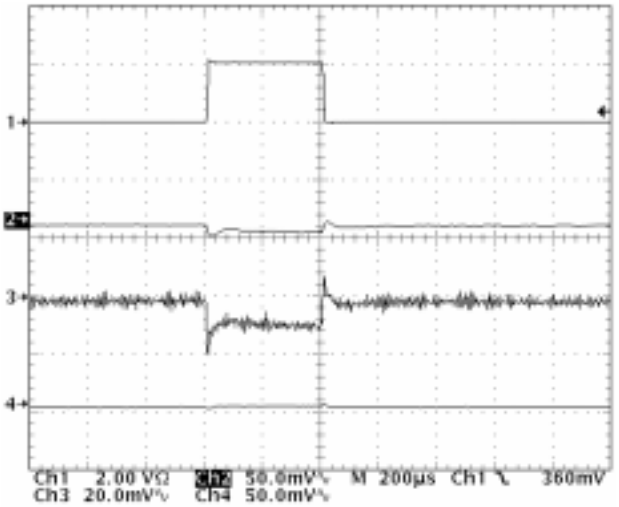
Channel 1: VDDQ output voltage, 1.0 V/div
Channel 2: VTT output voltage, 1.0 V/div
Channel 3: V1P5 output voltage, 1.0 V/div
Time base: 5.0 ms/div

Figure 10. Power Up Sequence



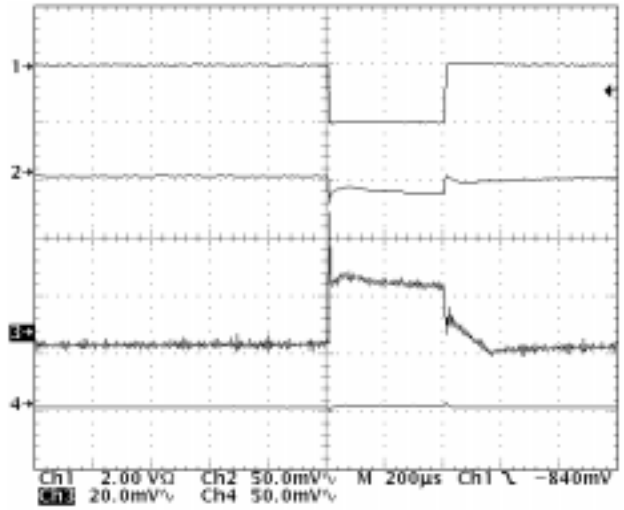
Channel 1: BUF_CUT pin voltage, 5.0 V/div
Channel 2: VDDQ output voltage, AC−coupled, 50 mV/div
Channel 3: VTT output voltage, AC−coupled, 200 mV/div
Channel 4: V1P5 output voltage, 1.0 V/div
Time base: 10 ms/div

Figure 11. S0−S3−S0 Transition



Channel 1: Current sourced out of VTT, 2.0 A/div
Channel 2: VDDQ output voltage, AC−coupled, 50 mV/div
Channel 3: VTT output voltage, AC−coupled, 20 mV/div
Channel 4: V1P5 output voltage, AC−coupled, 50 mV/div
Time base: 200 μs/div

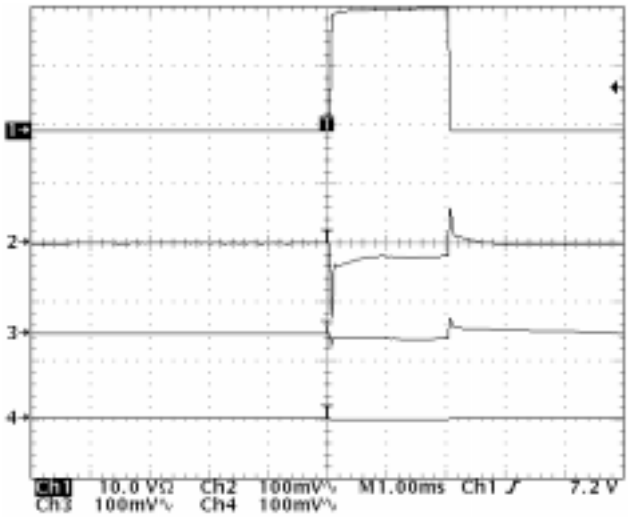
Figure 12. VTT Source Current Transient, 0A − 2A – 0A



Channel 1: Current sunk into of VTT, 2.0 A/div
Channel 2: VDDQ output voltage, AC−coupled, 50 mV/div
Channel 3: VTT output voltage, AC−coupled, 20 mV/div
Channel 4: V1P5 output voltage, AC−coupled, 50 mV/div
Time base: 200 μs/div

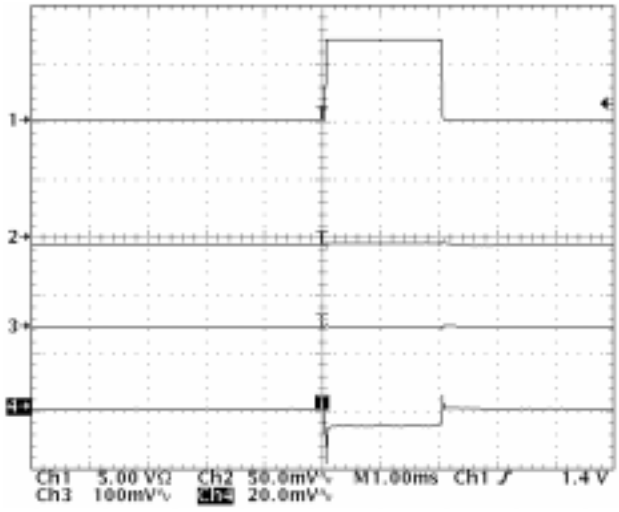
Figure 13. VTT Sink Current Transient, 0A − 2A − 0A

TYPICAL OPERATING WAVEFORMS



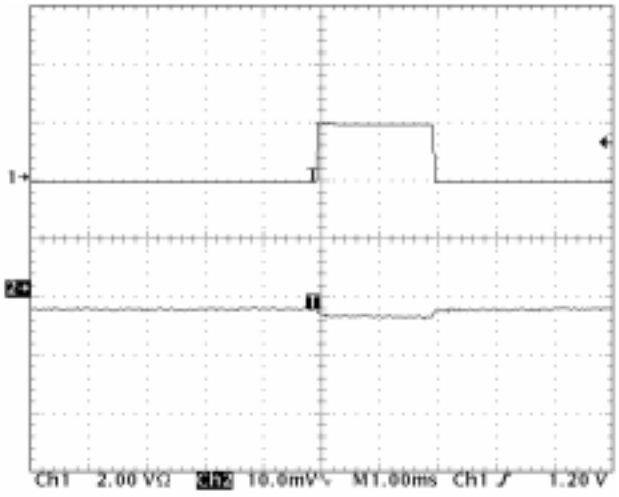
Channel 1: Current sourced into of VDDQ, 10 A/div
Channel 2: VDDQ output voltage, AC−coupled, 100 mV/div
Channel 3: VTT output voltage, AC−coupled, 100 mV/div
Channel 4: V1P5 output voltage, AC−coupled, 100 mV/div
Time base: 1.0 ms/div

Figure 14. VDDQ Source Current Transient, 0A – 20A – 0A



Channel 1: Current sourced into of V1P5, 5.0 A/div
Channel 2: VDDQ output voltage, AC−coupled, 50 mV/div
Channel 3: VTT output voltage, AC−coupled, 100 mV/div
Channel 4: V1P5 output voltage, AC−coupled, 20 mV/div
Time base: 1.0 ms/div

Figure 15. V1P5 Source Current Transient, 0A – 7A – 0A



Channel 1: Current sourced into of VDDQ, 2.0 A/div
Channel 2: VDDQ output voltage, AC−coupled, 10 mV/div
Time base: 1.0 ms/div

Figure 16. S3 Mode without 12VATX, 0A – 2A – 0A

DETAILED OPERATION DESCRIPTIONS

General

The NCP5209 4−In−1 PWM Buck and Tri−Linear DDR Power Controller contains a high efficiency PWM controller, an integrated two−quadrant linear regulator and two linear regulator controllers.

The VDDQ supply is generated by a PWM controller driving two external N−Ch FETs. The VTT termination voltage is tracked by an integrated linear regulator with sourcing and sinking current capability which tracks at 1/2 VDDQ. The dual linear controllers driving two external N−Ch FETs can either be cascaded to create the MCH core voltage or work independently to produced two regulated output voltages. All regulator outputs are adjustable.

The inclusion of soft−start, supply undervoltage monitors, overcurrent protection and thermal shutdown, makes this device a complete power solution for the MCH and DDR memory system. This device is housed in thermal enhanced space−saving QFN−20 package.

ACPI Control Logic

The ACPI control logic powered by the 5VDUAL supply input. External control is applied to the high impedance CMOS input labeled BUF_CUT. This signal and three internal undervoltage detectors are used to determine the operating mode according to the state diagram in Figure 19. The 5VDUAL supply must be come up before the other supplies.

The UVLOs monitor the motherboard supplies 5VDUAL, 12VATX and 5VATX through 5VDUAL, BOOT and OCDDQ pins respectively. Three control signals, _5VDUALGD, _BOOTGD and _OCDDQGD, are asserted when the supply voltages are in good condition.

The device is powered up initially in the S5 shutdown mode to minimize the power consumption. When all three supplies are good with BUF_CUT is LOW, the device enters S0 normal operating mode.

Transition of BUF_CUT from LOW to HIGH in S0 mode triggers the device into S3 sleep mode. In S3 mode, external 12VATX and 5VATX supplies collapse and only DDQ regulator is working. Both BOOT_UVLO and 5VATX_UVLO work specially. Two control signals, _BOOTGD and _OCDDQGD go low and the IC remains in the S3 mode.

During S3 mode, the transition of BUF_CUT from HIGH to LOW triggers the device back to S0 mode providing 12VATX and 5VATX are good. The IC can re−enter S5 mode from S0 mode by removing one of the supplies. Transitions from S3 to S5 or vice versa are not allowed. A timing diagram is shown in Figure 18. Table 1 summarizes the operating states of all regulators and the conditions of output pins.

Internal Bandgap Voltage Reference

An internal bandgap reference is generated whenever 5VDUAL exceeds 2.7 V. Once this bandgap reference is in regulation, an internal signal _VREFGD is asserted to wake up the ACPI logic.

S5−To−S0 Mode Power Up Sequence

The ACPI control logic is enabled by the assertion of VREFGD. Once the ACPI control is activated, the power−up sequence starts by waking up the 5VDUAL voltage monitor block and reference current generator first. If the 5VDUAL is within the preset level, the BOOT and OCDDQ undervoltage monitor blocks are enabled to detect the presence of 12VATX and 5VATX supplies. When the three supplies are in regulation and BUFCUT is LOW the device enters S0 mode by activating the soft−start of DDQ switching regulator.

Once the DDQ regulator is in regulation and the soft−start interval is completed, the _INREGDDQ signal is asserted HIGH to enable the VTT regulator as well as the dual linear controllers.

DDQ Switching Regulator

The DDQ regulator in S0 mode is a synchronous buck controller that drives two external power N−Ch FETs to supply up to 20 A. It employs the voltage mode fixed frequency PWM control scheme with external compensation switching at 250 kHz ± 13.2%. As shown in Figure 2, the VDDQ output voltage is divided down and fed back to the inverting input of an amplifier through FBDDQ pin to close the loop at $VDDQ = VFBQ \times (1 + R1/R2)$. This amplifier compares the feedback voltage with an internal reference voltage VREF1 (= 1.190 V) to generate an error signal for the PWM comparator. This error signal is further compared with a fixed frequency RAMP waveform to generate a PWM signal. This PWM signal drives the external N−Ch FETs via the TG_DDQ and BG_DDQ pins. External inductor L and capacitor COUT1 filter the output voltage. When the NCP5209 leaves S5 mode, the VDDQ output voltage ramps up at a rate controlled by the capacitor at SS pin. When the regulation of VDDQ is regulating in S0 mode, a signal _INREGDDQ goes HIGH.

In S3 standby mode, the switching frequency is doubled to reduce the conduction loss in the external N−Ch FETs.

Table 1. Mode, Operation and Output Pin Condition

	Operating Conditions			Output Pin Conditions			
	DDQ	VTT	Dual Linear	TGDDQ	BGDDQ	DRV_2P4	DRV_1P5
S0	Normal	Normal	Normal	Normal	Normal	Normal	Normal
S3	Standby	H−Z	H−Z	Standby	Standby	Low	Low
S5	OFF	H−Z	H−Z	Low	Low	Low	Low

Tolerance of VDDQ

Both the tolerance of VFBDDQ and the ratio of external resistor divider R1/R2 impact the precision of VDDQ. With the control loop in regulation, VDDQ = VFBQ × (1 + R1/R2). With a worst case (for all valid operating conditions) VFBDDQ tolerance of ±1.5%, a worst case range of ±2% for VDDQ can be assured if the ratio R1/R2 is specified as 1.100 ±1%.

Fault Protection of VDDQ Regulator

In S0 mode, an external resistor (RL1) connecting the 5VATX supply to the OCDDQ pin sets the current limit for the high−side switch. An internal 40 μA current sink at the OCDDQ pin establishes a voltage drop across this resistor. The inductor node voltage is sensed at the SWDDQ pin through a protective resistor (RSWDDQ). The voltage at OCDDQ pin is compared to the voltage at SWDDQ pin when the high−side FET is turned on after a fixed period of blanking time thus avoiding false current limit triggering. If the voltage at SW_DDQ is lower than that at OCDDQ, an overcurrent condition occurs, during which, all regulators are latched off to protect against overcurrent. The IC can be powered up again only if any one of supply voltages (5VDUAL, 12VATX or 5VATX) is recycled or the SS−pin is discharged to ground externally.

Since the OCDDQ pin is also used for detecting 5VATX power supply, the upper threshold of the 5VATX UVLO is set to 1.25 V. Therefore, RL1 must be selected in such a way that the voltage at the OCDDQ pin must be higher than this threshold to avoid false triggering of UVLO.

In S3 mode, this overcurrent protection feature is disabled.

Feedback Compensation of VDDQ Regulator

The compensation network is shown in Figure 2.

VTT Active Terminator

The VTT active terminator is a two quadrant linear regulator with two internal N−Ch FETs to provide current sink and source capability up to 2.0 A. It is activated only when the VDDQ regulator is in regulation in S0 mode. It draws power from VDDQ with the internal gate drive power derived from 5VDUAL. While the VTT output is directly connected to the FBVTT pin, the VTT voltage is designed to automatically track at the half of the DDQ_REF voltage. This VTT voltage can be adjusted by using an external resistor divider in the feedback loop. This regulator is stable with any value of output capacitor greater than 470 μF, and is insensitive to ESR ranging from 1.0 mΩ to 400 mΩ.

Fault Protection of VTT Active Terminator

To provide protection for the internal FETs, a bidirectional current limit set to 2.4 A is implemented. The VTT current limit provides a soft−start function during startup.

Dual Linear Regulator Controllers

The dual linear regulators are formed by two high−gain controllers driving external N−Ch FETs. They are activated after the DDQ regulator is in regulation in S0 mode. The output voltage of each regulator is fed back through an external resistor divider. The feedback voltage is compared to an internal reference voltage VREF2 (= 0.800 V) to achieve voltage regulation.

Both linear regulators use a common soft−start ramping voltage set to 1.5 ms. Once they are activated, hiccup mode is employed during the soft−start period to protect them against short circuit or power failure conditions. In the soft−start interval, the feedback voltages of both regulators are compared with the soft−start ramping voltage. If either one of feedback voltages is 100 mV below the SS ramping voltage, a short circuit or power failure condition is detected, causing both regulators to be reset and initiate the soft−start sequence again, as depicted in Figure 17. This hiccup mode feature is disabled once after both outputs are in regulation.

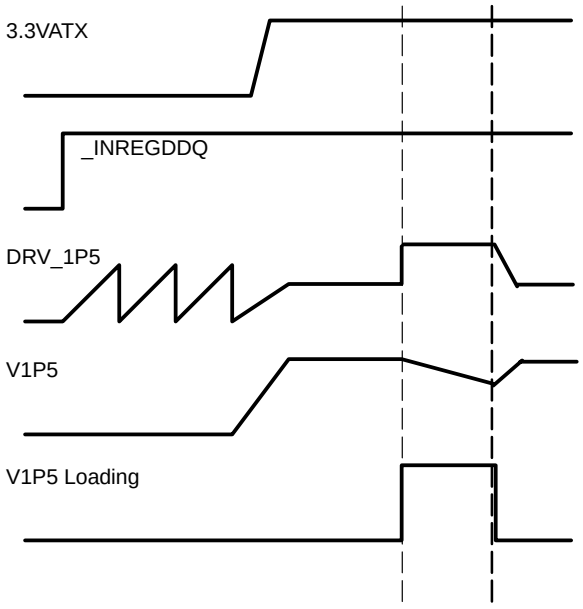


Figure 17. Hiccup Mode Soft−Start of Dual Linear Regulators

These two linear regulators can be cascaded to generate the 1.5 V MCH core voltage with 2.4 V as the intermediate voltage. By using 3.3 VATX as the power supply of external N−Ch FETs, up to 7.0 A can be delivered.

If only one linear regulator is used, it is recommended to pull the feedback pin of the unused regulator to 5VDUAL to reduce the internal power consumption as well as to avoid soft−start issue.

Fault Protection of Dual Linear Regulator

Internal soft−start is built−in to limit the in−rush current.

BOOT Pin Supply Voltage

In a typical application, a flying capacitor is connected between the inductor LX node and the BOOT pin. In S0 mode, the 12VATX supply is tied to the BOOT pin through a Schottky diode. A 13 V Zener diode must be put as close to the BOOT pin as possible to clamp the boot strapping voltage produced by the flying capacitor.

In S3 mode the 12VATX supply is collapsed. The BOOT voltage is created by the Schottky diode between 5VDUAL and BOOT pins and the flying capacitor. The BOOT_UVLO works in the special case. The _BOOTGD goes low and the IC remains in S3 mode.

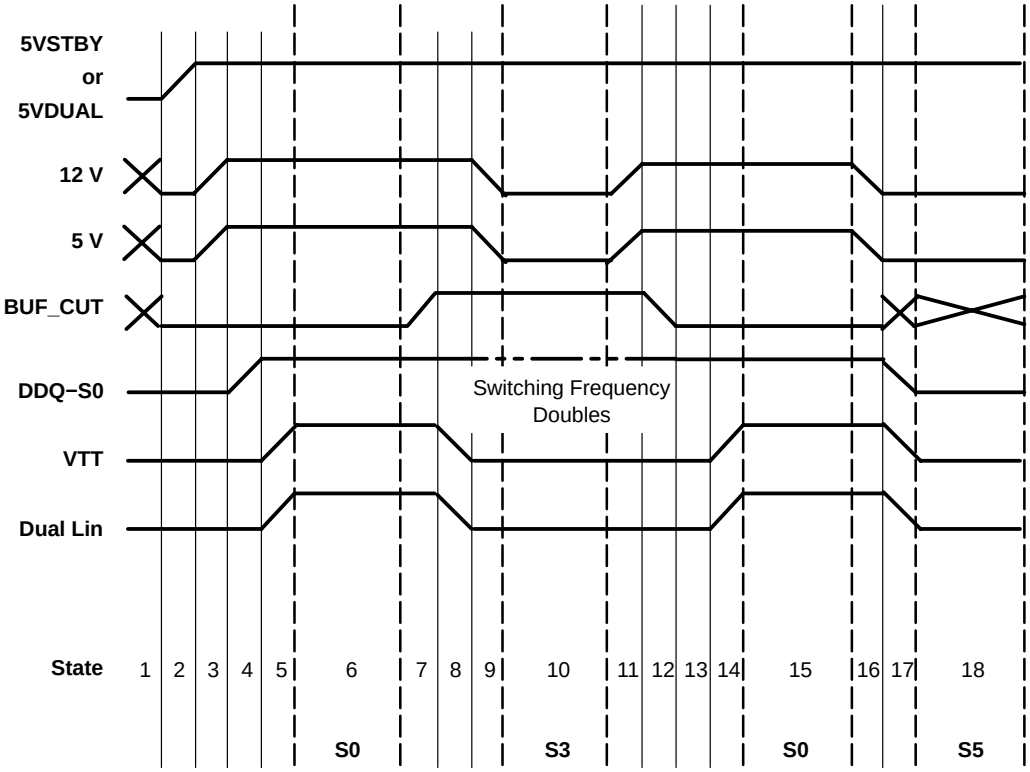
Thermal Consideration

Assuming an ambient temperature of 50°C, the maximum allowed dissipated power of the QFN−20 package is 2.8 W, which is enough to handle the internal power dissipation in S0 mode. **To take full advantage of the thermal capability of this package, the exposed pad underneath must be soldered directly onto a PCB metal substrate to allow good thermal contact.**

Thermal Shutdown

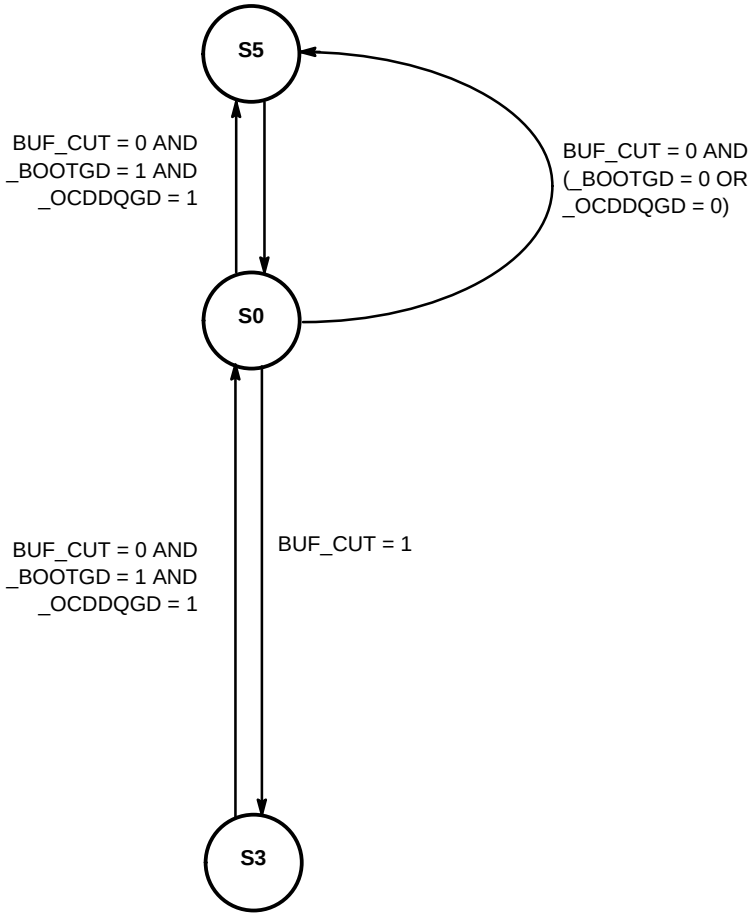
When the junction temperature of the IC exceeds 145°C, the entire IC is shutdown. When the junction temperature drops below 120°C, the chip resumes normal operation.

POWER UP AND POWER DOWN TIMING



2 5VSTBY or 5VSTB is ultimate chip enable. This supply has to be up first to ensure gates are in known state.
3 12 and 5.0 V supplies can ramp in either order.
4 DDQ ramps up with timing set by the SS pin.
5 MCH and VTT both ramp once DDQ SS is completed and DDQ is within 90% of regulated value.
6 S0 mode.
7 Prepare S3 Mode −− BUF_CUT goes HIGH.
8 VTT and MCH turn off.
9 12 V and 5.0 V ramp down.
10 Standard S3 mode.
11 12 V and 5.0 V ramp back to regulation.
12 BUF_CUT goes LOW.
13 DDQ switches back to 250 kHz.
14 MCH and VTT ramp up again.
15 S0 mode.
16 Prepare S5 mode −− 12VUVLO = H OR 5VUVLO = H.
17 DDQ, VTT and MCH turn off.
18 S5 mode.

Figure 18. Timing Diagram



Note: 5VDUAL is assumed to be in good condition in any mode.
All possible state transitions are shown.
All unspecified inputs do not cause any state change.

Figure 19. State Transitions Diagram of NCP5209

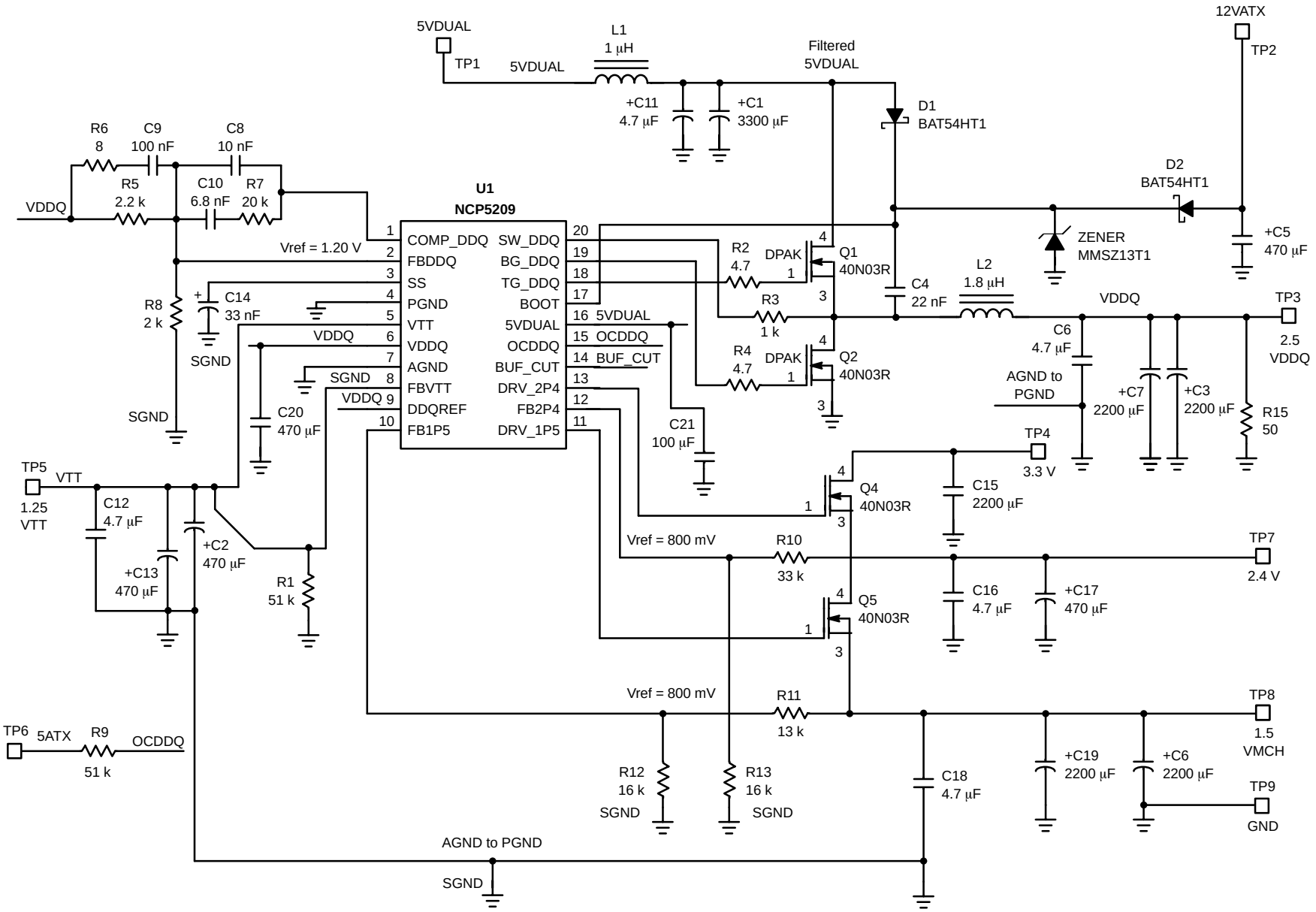


Figure 20. NCP5209 Typical Application Circuit

Application Circuit

Figure 20 shows the typical application circuit for NCP5209. NCP5209 is specifically designed as a total power solution for the MCH and DDR memory system. This diagram contains NCP5209 for driving two external N−Ch FETs to form the DDR memory supply voltage (VDDQ) and two external N−Ch FETs to form the MCH regulator.

Output Inductor Selection

The value of the output inductor is chosen by balancing ripple current with transient response capability. A value of 1.7 μH will yield about 3.0 A peak−to−peak ripple current when converting from 5.0 V to 2.5 V at 250 KHz. It is important that the rated inductor current is not exceeded during full load, and that the saturation current is not less than the expected peak current. Low ESR inductors may be required to minimize DC losses and temperature rise.

Input Capacitor Selection

Input capacitors for PWM power supplies are required to provide a stable, low impedance source node for the buck regulator to convert from. The usual practice is to use a combination of electrolytic capacitors and multi−layer ceramic capacitors to provide bulk capacitance and high frequency noise suppression. It is important that the capacitors are rated to handle the AC ripple current at the input of the buck regulators, as well as the input voltage.

Output Capacitor Selection

Output capacitors are chosen by balancing the cost with the requirements for low output ripple voltage and transient voltage. Low ESR electrolytic capacitors can be effective at reducing ripple voltage at 250 KHz. Low ESR ceramic capacitors are most effective at reducing output voltage excursions caused by fast load steps of system memory and the memory controller.

Switcher Power MOSFET Selection

Power MOSFETs are chosen by balancing the cost with the requirements for the current load of the memory system and the efficiency of the converter provided. The selections criteria can be based on drain−source voltage, drain current, on−resistance $R_{DS(on)}$ and input gate capacitance. Low $R_{DS(on)}$ and high drain current power MOSFETs are usually preferred to achieve the high current requirement of the DDR memory system, as well as the high efficiency of the converter. The tradeoff is a corresponding increase in the input gate capacitor of the power MOSFET.

PCB Layout Considerations

With careful PCB layout the NCP5209 can supply 20 A or more of current. It is very important to use wide traces or large copper shapes to carry current from the input node through the MOSFET switches, inductor and the output filters and load. Reducing the length of high current nodes will reduce losses and reduce parasitic inductance. It is usually best to locate the input capacitors the MOSFET switches and the output inductor in close proximity to reduce DC losses, parasitic inductance losses and radiated EMI.

The sensitive voltage feedback and compensation networks should be placed near the NCP5209 and away from the switch nodes and other noisy circuit elements. Placing compensation components near each other will minimize the loop area and further reduce noise susceptibility.

Optional Boost Voltage Configuration

The charge pump circuit in Figure 21 can be used instead of boost voltage scheme of Figure 20. The advantage in Figure 21 is the elimination of the requirement for the Zener clamp. The tradeoff is slightly less boost voltage and a corresponding increase in MOSFET conduction losses.

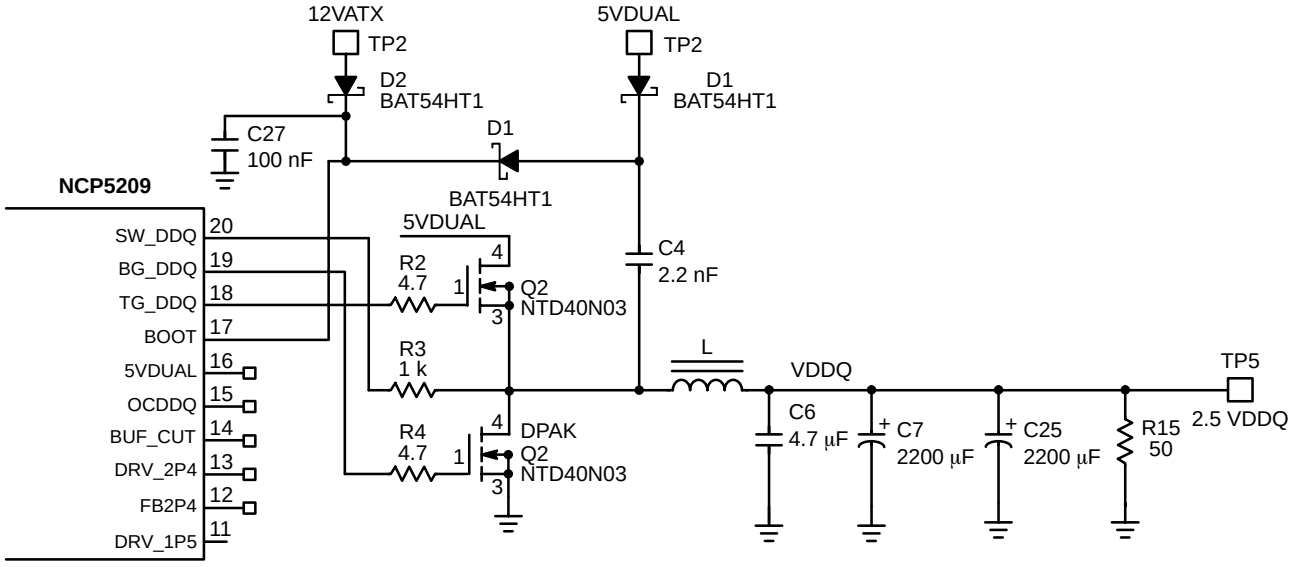


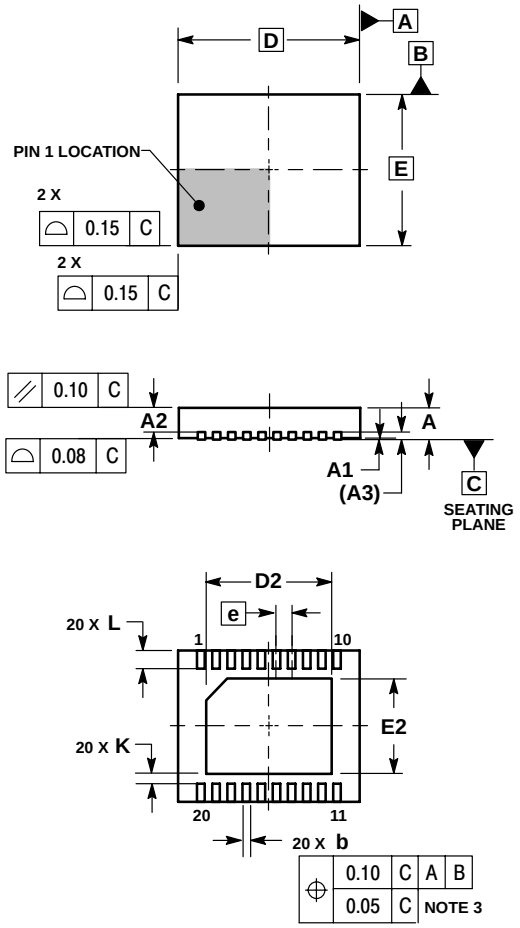
Figure 21. Charge Pump Circuit at Boot Pin

Table 2. Bill of Material of NCP5209 Application Circuit

Ref Design	Description	Value	Qty	Part #	Manufacturer
Q1, Q2, Q3, Q4	Power MOSFET N−Channel	25 V, 12.6 mΩ, 40 A	4	NTD40N03R	ON Semiconductor
D1, D2	Rectifier Schottky Diode	30 V	2	BAT54HT1	ON Semiconductor
U1	Controller	4−In−1 PWM Buck & Tri−Linear Power Controller	1	NCP5209	ON Semiconductor
Zener	Zener Diode	13 V, 0.5 W	1	MMSZ13T1	ON Semiconductor
L1	Toroidal Choke	1.0 μH, 25 A	1	T60−26(6T)	−
L2	Toroidal Choke	1.8 μH, 25 A	1	T50−26B(6T)	−
C1	Aluminum Electrolytic Capacitor	3300 μF, 6.3 V	1	EEUFJ0J332U	Panasonic
C5	Aluminum Electrolytic Capacitor	470 μF, 35 V	1	EEUFC1V471	Panasonic
C21	Aluminum Electrolytic Capacitor	100 μF, 50 V	1	EEUFC1H101	Panasonic
C15	Aluminum Electrolytic Capacitor	2200 μF, 10 V	1	EEUFC1A222L	Panasonic
C17, C20	Aluminum Electrolytic Capacitor	470 μF, 16 V	2	EEUFC1C471	Panasonic
C13, C2	Aluminum Electrolytic Capacitor	470 μF, 10 V	2	EEUFC1A471	Panasonic
C7, C3, C19, C6	Aluminum Electrolytic Capacitor	2200 μF, 6.3 V	4	EEUFC0J222SL	Panasonic
C11, C6, C16, C18, C12	Ceramic Capacitor	4.7 μF, 6.3 V	5	ECJHVB0J475M	Panasonic
C4	Ceramic Capacitor	22 nF, 25 V	1	ECJ1VB1E223K	Panasonic
C10	Ceramic Capacitor	6.8 nF, 50 V	1	ECJ1VB1H682K	Panasonic
C9	Ceramic Capacitor	100 nF, 16 V	1	ECJ1VB1C104K	Panasonic
C8	Ceramic Capacitor	10 nF, 50 V	1	ECJ1VB1H103K	Panasonic
C14	Ceramic Capacitor	33 nF, 25 V	1	ECJ1VB1E333K	Panasonic
R2, R4	Resistor	4.7 Ω	2	−	−
R3	Resistor	1.0 kΩ	1	−	−
R7	Resistor	20 kΩ	1	−	−
R6	Resistor	8.2 Ω	1	−	−
R8	Resistor	2.0 kΩ	1	−	−
R5	Resistor	2.2 kΩ	1	−	−
R10	Resistor	33 kΩ	1	−	−
R13, R12	Resistor	16 kΩ	2	−	−
R11	Resistor	13 kΩ	1	−	−
R15	Resistor	50 Ω	1	−	−
R1, R9	Resistor	51 kΩ	2	−	−

PACKAGE DIMENSIONS

QFN−20, DUAL−SIDED, 6x5 mm
MN SUFFIX
CASE 505AB−01
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A2	0.65	0.75
A3	0.20 REF	
b	0.23	0.28
D	6.00 BSC	
D2	3.98	4.28
E	5.00 BSC	
E2	2.98	3.28
e	0.50 BSC	
K	0.20	−−−
L	0.50	0.60

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