28 V, 2-Channel Power Monitor

NCP45496

The NCP45496 is a high−performance monolithic IC which can be used to monitor the power on two high−voltage power supplies simultaneously. The voltage and current on each bus are measured and converted to a power signal that is output as a current. The power of multiple busses may be summed by connecting the power current signals (IPWRx). The power signal for each channel is also sampled by an internal ADC and made available over an SVID bus. It also includes a low−latency open−drain ALARM signal that is produced by comparing the power of each bus to its individually programmable threshold level. If either bus exceeds the programmed power threshold the low−latency ALARM signal will be pulled low. The SVID bus is used to program the ALARM levels.

Features

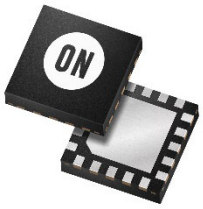
- Represents Power from each of two Channels as a Scaled Output Current
- Single Device monitors two Supplies
- Current Outputs from multiple Devices can be connected to obtain the Summed Power
- Individually programmable Low−latency ALARM to Signal High Channel Power
- Provides Digitized Power Measurements over an SVID Bus
- RoHS/REACH Compliant Device

Typical Applications

- Power Management
- Power Control Loops

End Products

- Computers / Notebooks / Tablets / Graphics Cards
- Servers / Data Centers
- Battery Chargers

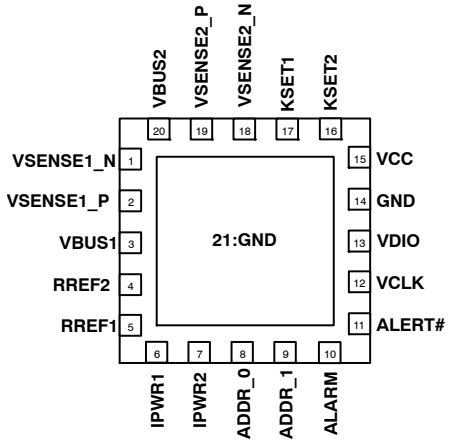


QFN20 3x3, 0.4P
CASE 485BC

MARKING DIAGRAM

NCP45496 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP45496XMNWTWG	QFN20 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

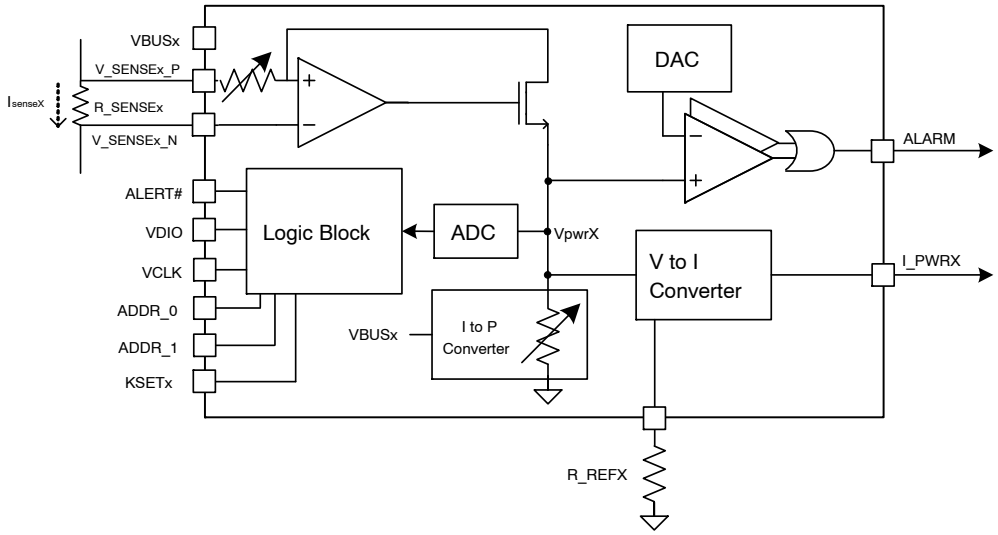


Figure 1. Block Diagram

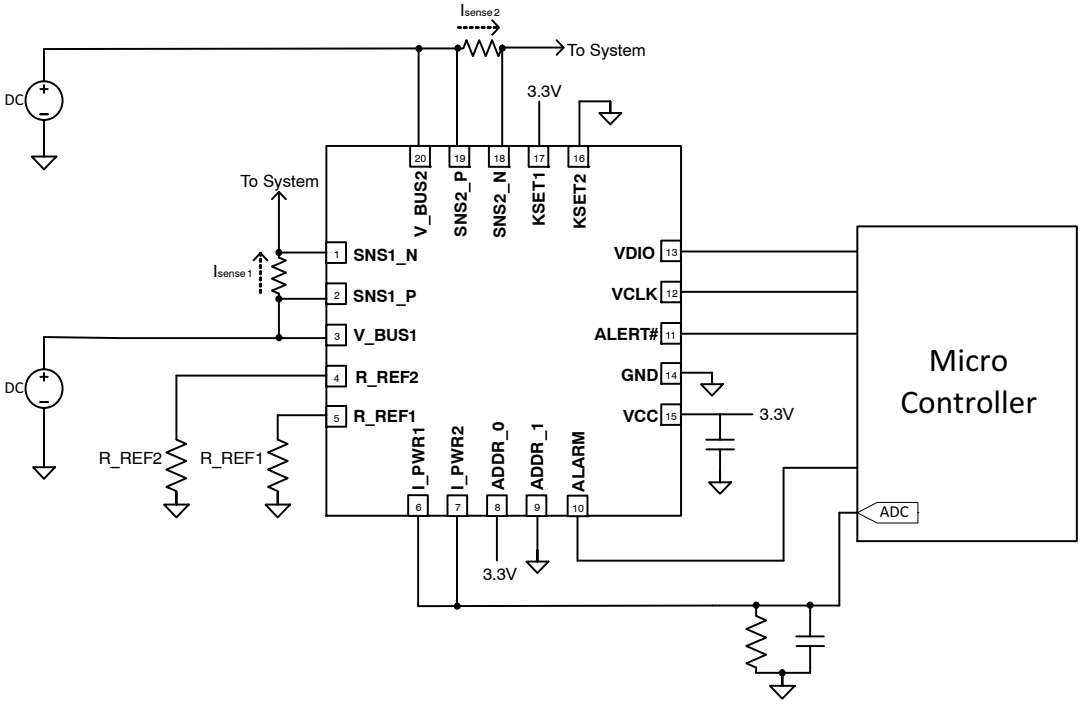


Figure 2. Application Schematic

Table 1. PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
1, 18	VSENSEx_N	AI	Sense Resistor Low−side Voltage, High−voltage
2, 19	VSENSEx_P	AI	Sense Resistor High−side Voltage, High−voltage
3, 20	VBUSx	AI	Bus Voltage Input, High−voltage
4, 5	RREFx	AIO	Reference Resistor to generate IPWRx
6, 7	IPWRx	AO	Scaled Current Output proportional to measured power
8, 9	ADDR_x	DI	SVID Address Select. (Note 1)
10	ALARM	DO	Low−latency Alarm Signal
11	ALERT#	DO	SVID interface signal
12	VCLK	DI	SVID interface signal
13	VDIO	DIO	SVID interface signal
14	GND	GND	Device Ground
15	VCC	PWR	Device Power (Note 2)
16, 17	KSETx	DI	Power Signal Gain Select (Note 3)

1. Internal Pull−down to GND of typical 70 μA
2. Place a >100 nF decoupling capacitor from this pin to GND
3. Internal Pull−up to VCC of typical 70 μA

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Pins	Symbol	Value	Unit
Supply Voltage Range (Note 4)	VCC	V_{CC}	−0.3 to 6	V
Bus Input Voltage Range (Note 4)	VBUSx, VSENSEx_P, VSENSEx_N	V_{BV}	−0.3 to 30	V
Digital Input Voltage Range (Note 4)	ALERT#, ALARM, VCLK, VDIO, ADDR_x	V_{LV}	−0.3 to 6	V
Low Voltage I/O Range (Note 4)	RREFx, IPWRx	V_{LV}	−0.3 to 6	V
Storage Temperature Range		TSTG	−40 to 150	°C
ESD Capability, Human Body Model (Note 5)		ESD_{HBM}	>2.0	kV
ESD Capability, Charged Device Model (Note 5)		ESD_{CDM}	>0.5	kV
Lead Temperature, Soldering (Note 6)		T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
5. This device series incorporates ESD protection and is tested by the following methods:
   a. ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   b. ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   c. Latchup Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78
6. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

Table 3. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, QFN20, 3x3 mm (Note 7) Thermal Resistance, Junction−to−Air (Note 8)	$R_{\theta JA}$	50	°C/W

7. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
8. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

Table 4. RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Supply Voltage Range	V_{CC}	2.97	5.5	V
Bus Voltage Input Range	V_{BV}	2.97	28	V
VSENSE_N, VSENSE_P	V_{SENSE_N}, V_{SENSE_P}	2.97	28	V
Current Sense Differential Voltage Range (VSENSE_P – VSENSE_N)	V_{SENSE}	10	300	mV
RREFx Resistance	R_{REFx}	1.8	60	kΩ
I_{PWRx} Output Current	I_{PWRx}	0	1	mA
I_{PWRx} Output Voltage	V_{IPWRx}	0	V_{CC} – 1	V
Low Voltage I/O Range	V_{LV}	0	V_{CC}	V
Ambient Temperature	T_A	–40	105	°C
Junction Temperature	T_J	–40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 5. ELECTRICAL CHARACTERISTICS
VBUS = 12 V, VCC = 3.3 V, unless indicated otherwise. (Note 9)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
AC CHARACTERISTICS						
Power−up Time		T_{PWR_UP}			80	μs
ALARM Signal Latency (Notes 10)	12 kΩ pull−up to 3.3 V, 20 pF capacitive loading	T_{ALARM}		0.9	2	μs
Voltage Measurement Bandwidth		B_{VOL}	50	100		kHz
Current Measurement Bandwidth		B_{CUR}	100	200		kHz
V to I Conversion Bandwidth		B_{Vtol}		500		kHz
Step Current Response Latency (Notes 11, 15)		T_{DELAY_I}		1.5	3	μs
Step Voltage Response Latency (Notes 12, 15)		T_{DELAY_V}		2	3	μs
ADC Sample Rate (Note 13)		f_{ADC}	25	115		kHz
Power Measurement Update Period (Note 13)		T_{UPDATE}		17.4	80	μs
DC CHARACTERISTICS						
Digital Input Pins High Value		V_{IH}	0.65			V
Digital Input Pins Low Value		V_{IL}			0.45	V
Digital Output Pins Low Value	I_{SINK} = 4 mA	V_{OL}			0.4	V
Maximum Current Consumption VCC (Note 14)		I_{VCC}		9.25	12	mA
Maximum Current Consumption VBUS	V_{CC} > 2 V	I_{VBUS}		570	700	μA
	V_{CC} < 2 V	I_{VBUS}		0.7	5	μA
Maximum Current Consumption VSENSEx_N, VSENSEx_P	V_{CC} > 2 V	I_{VSENSE}		52	125	μA
	V_{CC} < 2 V	I_{VSENSE}		0.007	1	uA
MEASUREMENT ACCURACY						
IPWR Current Accuracy (Note 15)	2.97 V < VCC < 5.5 0.4 V < V_{PWR} < 1.8 V; 100 μA < IPWR < 1 mA			1.9	3.75	%
	2.97 V < VCC < 5.5 0.4 V < V_{PWR} < 1.8 V; IPWR < 100 μA		−3.5		3.5	μA
	VBUS = 12 V, VCC = 5 V, K = 8 0.4 V < V_{PWR} < 1.8 V; 100 μA < IPWR < 1 mA			0.5	2.75	%
Digitized Measurement Accuracy	0.8 V < V_{PWR} < 1.8 V			2.2	5	%
ALARM Threshold Accuracy	V_{CC} < 4.5 V; 0.8 V < $V_{THRESHOLD}$ < 1.8 V			1	5	%
	V_{CC} > 4.5 V; 0.8 V < $V_{THRESHOLD}$ < 2 V			1	5	%

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

9. Min and Max values are valid for temperature range −40°C ≤ T_J ≤ +105°C unless noted otherwise and are guaranteed by test, design, characterization, or statistical correlation. Typical values are referenced to T_J = 25°C.
10. Measured with a current step from 33% below the ALARM threshold to 33% above the ALARM threshold. The ALARM Signal is based on V_{PWRx}. V_{PWRx} responds to changes in bus voltage and current according to the Voltage Measurement Bandwidth and Current Measurement Bandwidth listed above. Rapid changes in voltage may respond slower.
11. Measured by quickly increasing voltage differential across VSENSEx_P and VSENSEx_N from 16 mV to 68 mV. The amount of time from when the voltage differential steps to when IPWRx settles within 10% of the DC value.
12. Measured by quickly increasing bus voltage by at least 10%. The amount of time from when the bus voltage steps to when IPWRx settles within 10% of the DC value.
13. V_{PWR} from each channel is muxed into single ADC for measurement. Each channel is guaranteed to be sampled at least once within the Power Measurement Update Period.
14. Each current output is sourced from V_{CC}. The expected I_VCC is (IPWR1 + IPWR2)*2 + 6 mA
15. With an external 500 kHz RC filter.

Table 6. ADC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Full Scale Voltage	V_{FS}	1.764	1.8	1.836	V
Resolution			8		Bits
Integral Nonlinearity	INL	−2	0	2	LSB
Differential Nonlinearity	DNL	−2	0	2	LSB
Offset Error	E_O	−1.5	0	1.5	LSB
Effective Number of Bits	ENOB		7.5		
Gain Error	E_G	−1	0.3	1	$\%V_{FS}$
Missing Codes			0		Codes

APPLICATIONS INFORMATION

Power Scaled Current Output

An internal current source supplies a current to each IPWRx pin that is scaled by the measured power on the respective bus according to the following equation:

$$I_{PWRx} = \frac{K \times R_{SENSEx} \times I_{SENSEx} \times V_{BUSx}}{R_{REFx}}$$

The accuracy of the output current is not guaranteed if the resulting I_{PWRx} is greater than 1 mA. The two current output pins can be connected together to generate a sum power current. The power current can be supplied across a resistor to generate a voltage proportional to the measured power.

Digitized Power Output

An internal ADC samples an internally generated voltage that follows the following equation,

$$V_{PWRx} = K \times R_{SENSEx} \times I_{SENSEx} \times V_{BUSx}$$

where K is a gain constant with two options that can be individually set for each channel as described in the Adjustable Shunt Amplifier Gain section.

The ADC full scale input is defined in Table 6. R_{SENSEx} and K should be selected such that the maximum expected power on the given channel will result in V_{PWRx} to be less than or equal to V_{FS}.

Adjustable Shunt Amplifier Gain

The gain of the current shunt amplifier (K) can be adjusted to accommodate a wide range of expected bus powers. The gain can be set to either 2 or 8 by setting the respective PIN_GAIN_CHx register to 0x3 or 0xF respectively. If the value in the PIN_GAIN_CHx register is 0, the gain of the channel will be defined by the connection to the KSETx pin according to the table below.

KSETx	K (V/ΩW)
GND	8
VCC	2

Low−Latency Alarm

The ALARM signal is used to signal when the measured power on either bus is greater than a given threshold. The threshold and hysteresis is individually programmable for each channel.

ALARM Threshold

Setting the PIN_ALARM_TH_CHx register will adjust the ALARM threshold for the respective channel. The power threshold corresponding with the register value is calculated using the following formula:

$$P_{ALARM} = \frac{PIN\_ALARM\_TH\_CHx + 1}{R_{SENSEx} \times K \times 128}$$

where PIN_ALARM_TH_CHx is the decimal value in the respective ALARM threshold register and K is the same constant described in the Adjustable Shunt Amplifier Gain section above. For example, with K = 8 and R_{SENSE} = 5 mΩ, a register setting of 199 corresponds to 39.0625 W.

ALARM Hysteresis

Setting the two least significant bits of the PIN_ALARM_CFG_CHx register will configure the ALARM hysteresis for the respective channel. The hysteresis for the ALARM is set according to the following table.

PIN_ALARM_CFG_CHx bits [1:0]	ALARM Signal Hysteresis
0x02	10%
0x03	15%

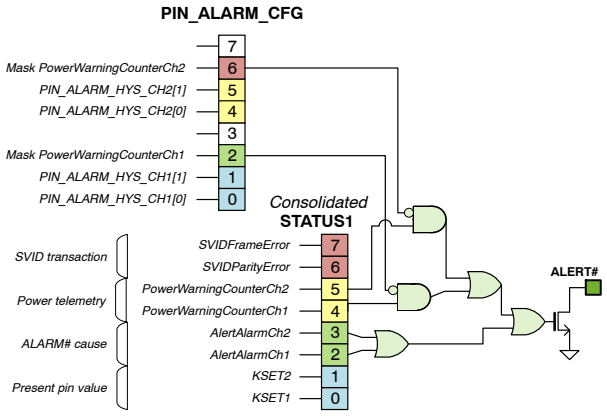


Figure 3. ALERT# Logic

Masking the ALERT# signal

By default, the ALERT# signal will be asserted when PIN_W_CNT_CHx reaches its maximum value as defined in Intel Document 456098. This behavior can be masked to prevent this assertion. If the third−least significant bit [2] of this register is set then the ALERT# Signal will not assert due to PIN_W_CNT_CHx reaching its maximum value.

Measuring Total Power with Scaled Current Outputs

Because the signals on IPWR1 and IPWR2 are scaled current outputs, they can be connected together to produce a current that is the sum of the two signals. If both current signals have the same gain, the sum of the two signals will be proportional to the total power measured on both channels.

The equation for IPWRx in the Power Scaled Current Output section above can be rewritten as,

$$I_{PWRx} = \frac{K \times R_{SENSEx}}{R_{REFx}} P_x$$

where P_x is the power measured on the channel. The gain of the current signal is equal to the ratio between K^*R_{SENSEx} and R_{REFx}. If the ratio between $K^* R_{SENSEx}$ and R_{REFx} is equal for both channels then the current produced when IPWR1 is connected to IPWR2 will be:

$$I_{PWR\_Total} = \frac{K \times R_{SENSE}}{R_{REF}} P_{Total}$$

The IPWRx signals from multiple NCP45496 devices can be connected together. If the ratio of K* R_{SENSEx} and R_{REFx} is equal for all channels the resulting current when connecting all these channels will follow the same equation above.

Low Pass Filter for IPWRx

To achieve the IPWR Current Accuracy listed in Table 5, an external low−pass RC filter with a corner frequency of at most 500 kHz is required. If multiple IPWR signals are connected together, only one filter is required. Place a capacitor in parallel with the resistor the current output is sourced over for measurement. The capacitor value to produce a 500 kHz low−pass filter can be determined with the following equation:

$$500\ kHz = \frac{1}{2 \times \pi \times RC}$$

For example, if the resistor that the current output is sourced over is 500 Ω, it is recommended that a greater than 636 pF capacitor be connected in parallel.

Unused Channels

If one channel is not needed, utilize Channel 1 and use the following connections for the unused Channel 2.

Pin Name	Recommended Connection
VBUS2	GND
VSENSE2_P	GND
VSENSE2_N	GND
RREF2	Float
IPWR2	Float

Power−up Process

There are no power−up sequencing requirements. As V_{CC} rises, the power−on−reset circuitry will ensure that the ALERT# and ALARM thresholds for each channel will be set at the default value. Once V_{CC} rises above 2.8 V and after the Power−up time listed in Table 5, the current driven on the IPWRx output will be proportional to the power measured on the bus. Digitized power measurements will be available over SVID following one Power Measurement Update Period after the Power−up time.

SVID Interface

The NCP45496 utilizes an SVID Interface as described in Intel Document 456098 Revision 1.93, and the DG PSYS Device Protocol Document TBD. The NCP45496 implements the functionalities of registers listed in Table 7 below as defined in the SVID documentation.

The address which the NCP45496 responds to is configurable by connecting the ADDR_x pins to VCC or GND. The resulting addresses are represented in the table below.

ADDR_1	ADDR_0	SVID Address
GND	GND	0x08
GND	VCC	0x09
VCC	GND	0x0A
VCC	VCC	0x0B

Layout Considerations

Sensitive signals that require special attention in board layout include the channel inputs (VSENSEx_P, VSENSEx_N, and VBUSx) and the scaled current output signals (IPWRx). The VSENSEx_P and VSENSEx_N signals require a direct kelvin connection to the leads of the sense resistor to avoid parasitic trace resistance affecting the shunt current measurement. This direct connection is shown in Figure 4 below. The sense resistors and connections from source to load for each channel need to be large enough to accommodate the expected high load current.

Care should be taken to keep IPWRx lines isolated from dynamically changing signals such as clocks and power supplies. If IPWRx must cross a dynamically changing signal, it is best practice to cross the signal at a right angle with as many board layers as possible between the signals. It is recommended that the required RC filter be placed as close as possible to where the signal will be measured.

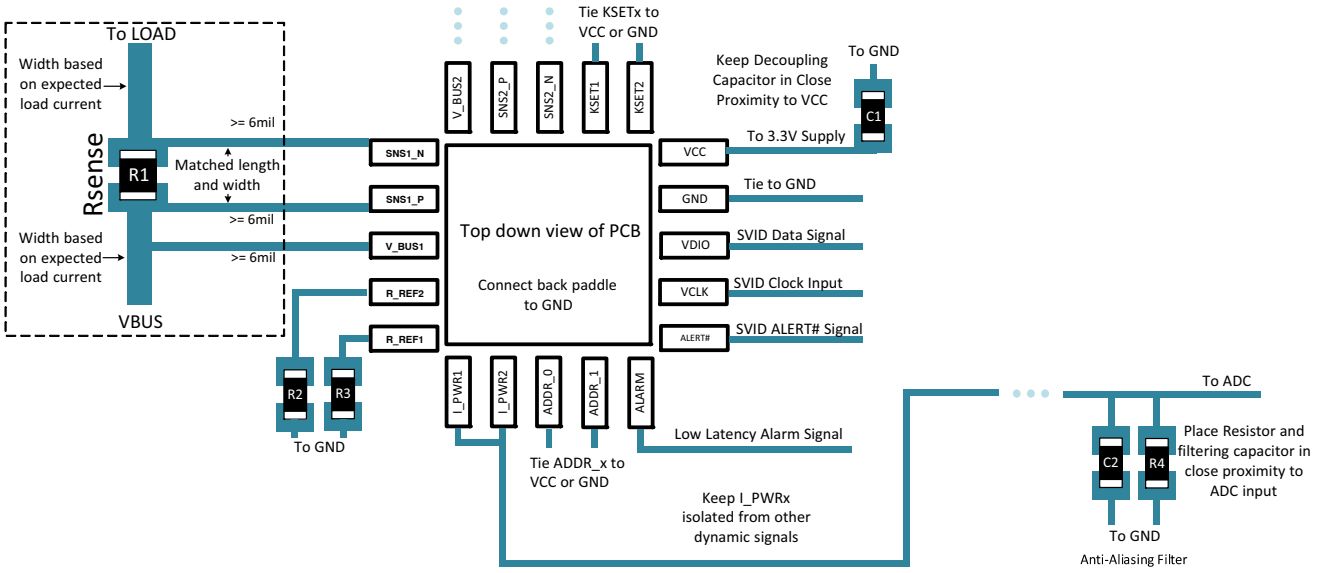


Figure 4. Layout Recommendations

Table 7. REGISTER MAP

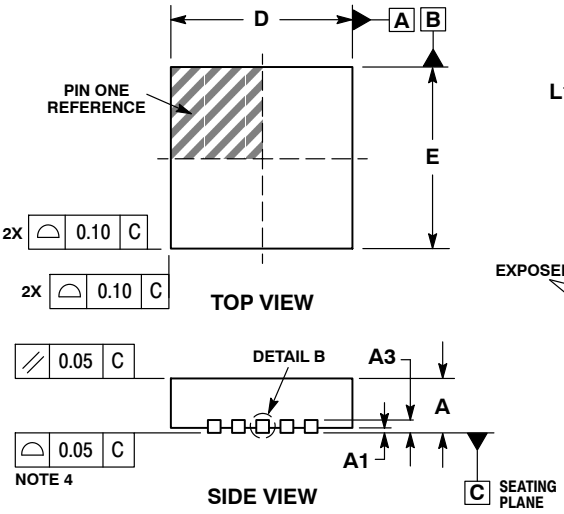
Group	Addr. (hex)	Name	Description	Reference to [1]		Type	Default (hex)
				Section	Comply (Note 16)		
Product Info	00	VENDOR_ID	Uniquely identifies the VR vendor.	7.2.1	YES	RO	1A
	01	PROD_ID	Uniquely identifies the VR product.	7.2.2	YES	RO	2E
	02	PROD_REV	Uniquely identifies the revision	7.2.3	YES	RO	A2
	05	PROTOCOL_ID	Identifies version of the SVID protocol the controller supports	7.2.6	YES	RO	12
	06	CAPABILITY	Identifies which telemetry registers are supported	7.2.7	YES	RO	20
Power Measurement (5.3)	07	PIN_GAIN_CH1	Channel 1 Power Gain		NEW (Note 18)	RW	0[7]
	08	PIN_GAIN_CH2	Channel 2 Power Gain		NEW (Note 18)	RW	0[7]
	C0	PIN_GAIN (Note 20)	Combined access to PIN_GAIN_CH1 and PIN_GAIN_CH2		NEW (Note 18)	RW	0[7]
	09	POWER_CH1	Channel 1 Power Measurement	7.4.7	PAR (Notes 17, 18)	RO	–
	0A	POWER_CH2	Channel 2 Power Measurement	7.4.7	PAR (Notes 17, 18)	RO	–
Event Notifications (5.4)	0B	PIN_ALARM_TH_CH1	Channel 1 Input power ALARM Threshold		PAR (Notes 17, 18)	RW	E6
	0C	PIN_ALARM_TH_CH2	Channel 2 Input power ALARM Threshold		PAR (Notes 17, 18)	RW	E6
	0D	PIN_ALARM_CFG_CH1	Channel 1 Input Power ALARM Configuration		NEW (Note 18)	RW	03
	0E	PIN_ALARM_CFG_CH2	Channel 2 Input Power ALARM Configuration		NO (Note 18)	RW	03
	C1	PIN_ALARM_CFG (Note 20)	Combined access to PIN_ALARM_CFG_CH1 and PIN_ALARM_CFG_CH2		NO (Note 18)	RW	33
Status Reporting (5.5)	10	STATUS1	Consolidated status	7.3.1	PAR (Note 17)	RO/RC	00
	14	LASTREAD	Contains last value read by get family command	7.3.4	PAR (Note 17)	RO	–
	1C	STATUS1_LASTREAD	Copy of last read status register	7.3.5	PAR (Note 17)	RO	–
Power Telemetry (5.6)	4B	PIN_W_LVL_CH1	Channel 1 Power−In Warning Level, High Byte (Note 19)	7.8.4	PAR (Note 17)	RO	¾ E6 (Note 21)
	4C	PIN_W_LVL_CH2	Channel 2 Power−In Warning Level, High Byte (Note 19)	7.8.4	PAR (Note 17)	RO	¾ E6 (Note 21)
	4D	PIN_W_CNT_CH1	Channel 1 Power−In Warning counter	7.8.5.2	PAR (Note 17)	RC	00
	4E	PIN_W_CNT_CH2	Channel 2 Power−In Warning counter	7.8.5.2	PAR (Note 17)	RC	00

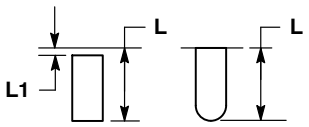
16. The register definition fully complies with the SVID specification: address, type, and purpose match the original definition.
17. Partially complying definition, the new definition can be found in the accompanying SVID proposal document or the DG PSYS Device Protocol Document TBD.
18. The custom register occupies SVID VENDOR_* slot.
19. The Technical Publications Template provides SVID normal precision 8−bit telemetry, i.e. it does not need the completing low byte register.
20. Combined access allows to write and read values belonging to both channels at once.
21. 3/4 of the respective register PIN_ALARM_TH_CHx.
22. When PIN_GAIN_CHx is set to 0 the gain is defined by the connections to KSETx pin.

QFN20 3x3, 0.4P
CASE 485BC
ISSUE O

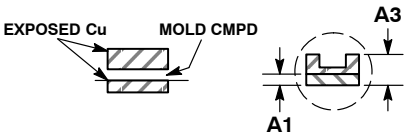
DATE 15 OCT 2009

SCALE 2:1





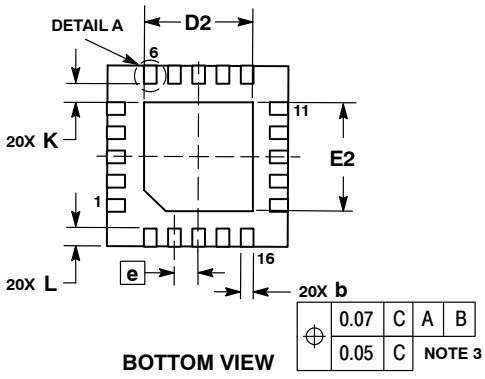
DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



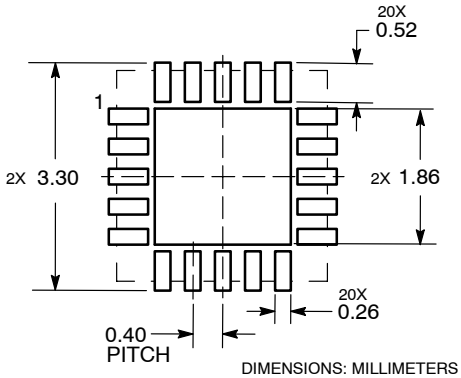
DETAIL B
ALTERNATE CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.15	0.25
D	3.00 BSC	
D2	1.70	1.90
E	3.00 BSC	
E2	1.70	1.90
e	0.40 BSC	
K	0.30 REF	
L	0.20	0.40
L1	0.00	0.15



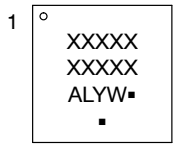
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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