## Fixed/Adjustable Current-Limiting Power-Distribution Switches

## NCP380, NCV380

The NCP380 is a high side power-distribution switch designed for applications where heavy capacitive loads and short-circuits are likely to be encountered. The device includes an integrated $55 \mathrm{~m} \Omega$ (DFN package), P-channel MOSFET. The device limits the output current to a desired level by switching into a constant-current regulation mode when the output load exceeds the current-limit threshold or a short is present. The current-limit threshold is either user adjustable between 500 mA and 2.1 A via an external resistor or internally fixed. The power-switch rise and fall times are controlled to minimize current ringing during switching.

An internal reverse-voltage detection comparator disables the power-switch if the output voltage is higher than the input voltage to protect devices on the input side of the switch.

The $\overline{\text { FLAG }}$ logic output asserts low during over current, reverse-voltage or over temperature conditions. The switch is controlled by a logic enable input active high or low.

## Features

- $2.5 \mathrm{~V}-5.5 \mathrm{~V}$ Operating Range
- $70 \mathrm{~m} \Omega$ High-side MOSFET
- Current Limit:
- User adjustable from 500 mA to 2.1 A
- Fixed $500 \mathrm{~mA}, 1 \mathrm{~A}, 1.5 \mathrm{~A}, 2 \mathrm{~A}$ and 2.1 A
- Under Voltage Lock-out (UVLO)
- Built-in Soft-start
- Thermal Protection
- Soft Turn-off
- Reverse Voltage Protection
- Junction Temperature Range: $-40^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$
- Enable Active High or Low (EN or $\overline{\mathrm{EN}}$ )
- Compliance to IEC61000-4-2 (Level 4)
- 8.0 kV (Contact)
- 15 kV (Air)
- UL Listed - File No. E343275 (NCP Versions Only)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These are Pb -Free Devices


## Typical Applications

- Laptops
- USB Ports/Hubs
- TVs


MARKING DIAGRAMS


UDFN6


TSOP-5


TSOP-6
XXX = Specific Device Code
A =Assembly Location
M = Date Code
$Y=$ Year
W = Work Week

- = Pb-Free Package
(Note: Microdot may be in either location)


## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 20 of this data sheet.

## NCP380, NCV380


*For Adjustable Version Only.
Figure 1. Typical Application Circuit

*For adjustable version only, otherwise not connected.
Figure 2. Pin Connections

Table 1. PIN FUNCTION DESCRIPTION

| Pin Name | Type |  |
| :---: | :---: | :--- |
| EN | INPUT | Enable input, logic low/high (i.e. EN or EN) turns on power switch |
| GND | POWER | Ground connection; |
| IN | POWER | Power-switch input voltage; connect a $1 \mu \mathrm{~F}$ or greater ceramic capacitor from IN to GND as close as pos- <br> sible to the IC. |
| FLAG | OUTPUT | Active-low open-drain output, asserted during overcurrent, overtemperature or reverse-voltage conditions. <br> Connect a 10 $\mathrm{k} \Omega$ or greater resistor pull-up, otherwise leave unconnected. |
| OUT | OUTPUT | Power-switch output; connect a $1 \mu \mathrm{~F}$ ceramic capacitor from OUT to GND as close as possible to the IC <br> is recommended. A $1 \mu \mathrm{~F}$ or greater ceramic capacitor from OUT to GND must be connected if the USB <br> requirement (i.e.120 $\mu \mathrm{F}$ capacitor minimum) is not met. |
| ILIM $^{*}$ | INPUT | External resistor used to set current-limit threshold; recommended $5 \mathrm{k} \Omega$ < R R ILIM $<250 \mathrm{k} \Omega$. |
| PAD1** | THERMAL | Exposed Thermal Pad: Must be soldered to PCB Ground plane |

[^0]Table 2. MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| From IN to OUT Pins: Input/Output (Note 1) | $\mathrm{V}_{\text {IN }}$, $\mathrm{V}_{\text {OUT }}$ | -7.0 to +7.0 | V |
| IN, OUT, EN, ILIM, FLAG, Pins: Input/Output (Note 1) | $\mathrm{V}_{\text {EN }}, \mathrm{V}_{\text {ILIM }}, \mathrm{V}_{\text {FLAG, }} \mathrm{V}_{\text {IN }}, \mathrm{V}_{\text {OUT }}$ | -0.3 to +7.0 | V |
| FLAG Sink Current | ISINK | 1 | mA |
| ILIM Source Current | ILIM | 1 | mA |
| ESD Withstand Voltage (IEC 61000-4-2) <br> (Output Only, when Bypassed with $1.0 \mu$ F Capacitor Minimum) | ESD IEC | 15 Air, 8 Contact | kV |
| Human Body Model (HBM) ESD Rating (Note 2) | ESD HBM | 2,000 | V |
| Machine Model (MM) ESD Rating (Notes 2 and 3) | ESD MM | 200 | V |
| Latch-up Protection (Note 4) Pins IN, OUT, EN, ILIM, FLAG | LU | 100 | mA |
| Maximum Junction Temperature Range (Note 6) | TJ | -40 to +TSD | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | TSTG | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Moisture Sensitivity (Note 5) | MSL | Level 1 |  |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. According to JEDEC standard JESD22-A108.
2. This device series contains ESD protection and passes the following tests: Human Body Model (HBM) $\pm 2.0 \mathrm{kV}$ per JEDEC standard: JESD22-A114 for all pins. Machine Model (MM) $\pm 200$ V per JEDEC standard: JESD22-A115 for all pins.
3. Except EN pin, 150 V .
4. Latch up Current Maximum Rating: $\pm 100 \mathrm{~mA}$ per JEDEC standard: JESD78 class II.
5. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J-STD-020.
6. A thermal shutdown protection avoids irreversible damage on the device due to power dissipation.

Table 3. OPERATING CONDITIONS

| Symbol | Parameter | Conditions |  | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IN }}$ | Operational Power Supply |  |  | 2.5 | - | 5.5 | V |
| $\mathrm{V}_{\mathrm{EN}}$ | Enable Voltage |  |  | 0 | - | 5.5 |  |
| $\mathrm{T}_{\mathrm{A}}$ | Ambient Temperature Range |  |  | -40 | 25 | +85 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{J}$ | Junction Temperature Range |  |  | -40 | 25 | +125 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{R}_{\text {ILIM }}$ | Resistor from ILIM to GND Pin |  |  | 5.0 | - | 250 | $\mathrm{k} \Omega$ |
| $\mathrm{I}_{\text {SINK }}$ | FLAG Sink Current |  |  | - | - | 1.0 | mA |
| $\mathrm{C}_{\text {IN }}$ | Decoupling Input Capacitor |  |  | 1.0 | - | - | $\mu \mathrm{F}$ |
| Cout | Decoupling Output Capacitor |  | rt per Hub | 120 | - | - | $\mu \mathrm{F}$ |
| $\mathrm{R}_{\text {өJA }}$ | Thermal Resistance Junction-to-Air | UDFN-6 P | ge (Notes 7 and 8) | - | 120 | - | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
|  |  | TSOP-5 P | ge (Notes 7 and 8) | - | 305 | - | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
|  |  | TSOP-6 | ge (Notes 7 and 8) | - | 280 | - | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| IOUT | Maximum DC Current |  | 6 Package | - | - | 2.1 | A |
|  |  | TSOP- | OP-6 Package | - | - | 1.0 | A |
| $\mathrm{P}_{\mathrm{D}}$ | Power Dissipation Rating (Note 9) | $\mathrm{T}_{\mathrm{A}} \leq 25^{\circ} \mathrm{C}$ | UDFN-6 Package | - | 830 | - | mW |
|  |  |  | TSOP-5 Package | - | 325 | - | mW |
|  |  |  | TSOP-6 Package | - | 350 | - | mW |
|  |  | $\mathrm{T}_{\mathrm{A}}=85^{\circ} \mathrm{C}$ | UDFN-6 Package | - | 325 | - | mW |
|  |  |  | TSOP-5 Package | - | 130 | - | mW |
|  |  |  | TSOP-6 Package | - | 145 | - | mW |

7. A thermal shutdown protection avoids irreversible damage on the device due to power dissipation.
8. The $R_{\text {日JA }}$ is dependent of the PCB heat dissipation. Board used to drive this data was a 2 " $\times 2$ " NCP380EVB board. It is a 2 layers board with 2-once copper traces on top and bottom of the board. Exposed pad is connected to ground plane for UDFN-6 version only.
9. The maximum power dissipation ( $P_{D}$ ) is given by the following formula:

$$
P_{D}=\frac{T_{J M A X}-T_{A}}{R_{\theta J A}}
$$

## NCP380, NCV380

Table 4. ELECTRICAL CHARACTERISTICS
(Min \& Max Limits apply for $\mathrm{T}_{\mathrm{A}}$ between $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ and $\mathrm{T}_{J}$ up to $+125^{\circ} \mathrm{C}$ for $\mathrm{V}_{\mathrm{IN}}$ between 2.5 V to 5.5 V (Unless otherwise noted). Typical values are referenced to $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{IN}}=5 \mathrm{~V}$.)

| Symbol | Parameter | Conditions |  | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| POWER SWITCH |  |  |  |  |  |  |  |
| $\mathrm{R}_{\mathrm{DS} \text { (on) }}$ | Static Drain-source On-state <br> Resistance <br> DFN Package | $\mathrm{V}_{\text {IN }}=5 \mathrm{~V}$ | $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}$ | - | 55 | 75 | $\mathrm{m} \Omega$ |
|  |  | $2.5 \mathrm{~V}<\mathrm{V}_{\text {IN }}<5.5 \mathrm{~V}$ | $-40^{\circ} \mathrm{C}<\mathrm{T}_{J}<125^{\circ} \mathrm{C}$ | - | - | 110 |  |
|  |  | $\mathrm{V}_{\text {IN }}=5 \mathrm{~V}$ | $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}$ | - | 70 | 95 | $\mathrm{m} \Omega$ |
|  |  | $2.5 \mathrm{~V}<\mathrm{V}_{\text {IN }}<5.5 \mathrm{~V}$ | $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}$ | - | - | 135 |  |
| $\mathrm{T}_{\mathrm{R}}$ | Output Rise Time | $\mathrm{V}_{\text {IN }}=5 \mathrm{~V}$ | $\begin{gathered} C_{\text {LOAD }}=1 \mu \mathrm{~F}, \\ \mathrm{R}_{\text {LOAD }}=100 \Omega(\text { Note 10 }) \end{gathered}$ | 0.3 | 1.0 | 1.5 | ms |
|  |  | $\mathrm{V}_{\text {IN }}=2.5 \mathrm{~V}$ |  | 0.2 | 0.65 | 1.0 |  |
| $\mathrm{T}_{\mathrm{F}}$ | Output Fall Time | $\mathrm{V}_{\text {IN }}=5 \mathrm{~V}$ |  | 0.1 | - | 0.5 |  |
|  |  | $\mathrm{V}_{\text {IN }}=2.5 \mathrm{~V}$ |  | 0.1 | - | 0.5 |  |

ENABLE INPUT EN OR EN

| $\mathrm{V}_{1 \mathrm{H}}$ | High-level Input Voltage |  | 1.2 | - | - | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Low-level Input Voltage |  | - | - | 0.4 | V |
| $\mathrm{I}_{\text {EN }}$ | Input Current | $\mathrm{V}_{\mathrm{EN}}=0 \mathrm{~V}, \mathrm{~V}_{\overline{\mathrm{EN}}}=5 \mathrm{~V}$ | -0.5 | - | 0.5 | $\mu \mathrm{A}$ |
| Ton | Turn On Time | $\mathrm{C}_{\text {LOAD }}=1 \mu \mathrm{~F}, \mathrm{R}_{\text {LOAD }}=100 \Omega$ (Note 11) | 2.0 | 3.0 | 4.0 | ms |
| T ${ }_{\text {OFF }}$ | Turn Off Time |  | 1.0 | - | 3.0 | ms |

CURRENT LIMIT

| IOCP | Current-limit Threshold (Maximum DC Output Current IOUT Delivered to Load) | $\mathrm{V}_{\mathrm{IN}}=5 \mathrm{~V}$ | $\mathrm{R}_{\text {ILIM }}=20 \mathrm{k} \Omega$ (Note 11) | 1.02 | 1.20 | 1.38 | A |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $\mathrm{R}_{\text {ILIM }}=40 \mathrm{k} \Omega$ <br> (Notes 11 and 13) | 0.595 | 0.700 | 0.805 |  |
|  |  |  | Fixed 0.5 A (Note 12) | 0.5 | 0.58 | 0.65 | A |
|  |  |  | Fixed 1.0 A (Note 12) | 1.0 | 1.15 | 1.3 |  |
|  |  |  | Fixed 1.5 A (Note 12) | 1.5 | 1.75 | 1.9 |  |
|  |  |  | Fixed 2.0 A (Note 12) | 2.0 | 2.25 | 2.5 |  |
|  |  |  | Fixed 2.1 A (Note 12) | 2.1 | 2.25 | 2.5 |  |
| T ${ }_{\text {DET }}$ | Response Time to Short Circuit |  | 5 V | - | 2.0 | - | $\mu \mathrm{s}$ |
| $\mathrm{T}_{\text {REG }}$ | Regulation Time |  |  | 1.8 | 3.0 | 4.0 | ms |
| TOCP | Overcurrent Protection Time |  |  | 14 | 20 | 26 | ms |

REVERSE-VOLTAGE PROTECTION

| $\mathrm{V}_{\text {REV }}$ | Reverse-voltage Comparator <br> Trip Point (VOUT $\left.-\mathrm{V}_{\text {IN }}\right)$ | $-\mathrm{V}_{\mathrm{IN}}=5 \mathrm{~V}$ | 100 | - | mV |  |
| :---: | :--- | :--- | :--- | :---: | :---: | :---: |
| $\mathrm{T}_{\text {REV }}$ | Time from Reverse-voltage <br> Condition to MOSFET Switch Off <br> \& FLAG Low | 4.0 | 6.0 | 9.0 | ms |  |
| $\mathrm{~T}_{\text {RREV }}$ | Re-arming Time |  | 7.0 | 10 | 15 | ms |

UNDERVOLTAGE LOCKOUT

| $V_{\text {UVLO }}$ | IN Pin Low-level Input Voltage | $\mathrm{V}_{\text {IN }}$ Rising | 2.0 | 2.3 | 2.4 | V |
| :---: | :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{~V}_{\text {HYST }}$ | IN Pin Hysteresis | $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ | 25 | - | 60 | mV |
| $\mathrm{T}_{\text {RUVLO }}$ | Re-arming Time |  | 7.0 | 10 | 15 | ms |

SUPPLY CURRENT

| $\mathrm{I}_{\text {INOFF }}$ | Low-level Output Supply Current | $\mathrm{V}_{\text {IN }}=5 \mathrm{~V}$, No Load on OUT, Device OFF |  |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {EN }}=0 \mathrm{~V}$ or $V_{\text {EN }}=5 \mathrm{~V}$ |  |  |  |$)$

Table 4. ELECTRICAL CHARACTERISTICS (continued)
(Min \& Max Limits apply for $\mathrm{T}_{\mathrm{A}}$ between $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ and $\mathrm{T}_{J}$ up to $+125^{\circ} \mathrm{C}$ for $\mathrm{V}_{\text {IN }}$ between 2.5 V to 5.5 V (Unless otherwise noted).
Typical values are referenced to $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{IN}}=5 \mathrm{~V}$.)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| FLAG PIN |  |  |  |  |  |  |
| $\mathrm{V}_{\text {OL }}$ | FLAG Output Low Voltage | $l_{\text {FLAG }}=1 \mathrm{~mA}$ |  |  | 400 | mV |
| ILEAK | Off-state Leakage | $V_{\text {FLAG }}=5 \mathrm{~V}$ |  |  | 1.0 | $\mu \mathrm{A}$ |
| $\mathrm{T}_{\text {FLG }}$ | FLAG Deglitch | FLAG De-assertion Time due to Overcurrent or Reverse Voltage Condition | 4.0 | 6.0 | 9.0 | ms |
| $\mathrm{T}_{\text {FOCP }}$ | FLAG Deglitch | FLAG Assertion due to Overcurrent | 6.0 | 8.0 | 12 | ms |

THERMAL SHUTDOWN

| $\mathrm{T}_{\text {SD }}$ | Thermal Shutdown Threshold |  |  | 140 |  |
| :---: | :--- | :--- | :--- | :---: | :---: |
| $\mathrm{~T}_{\text {SDOCP }}$ | Thermal Regulation Threshold |  | ${ }^{\circ} \mathrm{C}$ |  |  |
| $\mathrm{T}_{\text {RSD }}$ | Thermal Shutdown Rearming <br> Threshold |  | 125 |  | ${ }^{\circ} \mathrm{C}$ |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
10. Parameters are guaranteed for CLOAD and R ROAD connected to the OUT pin with respect to the ground, See Figure 3.
11. Adjustable current version, $\mathrm{R}_{\text {IIIM }}$ tolerance $\pm 1 \%$.
12. Fixed current version.
13. Not production test, guaranteed by characterization.


Figure 3. Test Configuration


Figure 4. Voltage Waveform

## BLOCK DIAGRAM


*For adjustable version only, otherwise not connected.

Figure 5. Block Diagram

## NCP380, NCV380



Figure 6. $T_{o n}$ Delay and $T_{\text {rise }}$ Time


Figure 7. $\mathrm{T}_{\text {off }}$ Delay and $\mathrm{T}_{\text {fall }}$


Figure 8. Turn On a Short


Figure 9. $2 \Omega$ Short on Output. Complete Regulation Sequence


Figure 10. OCP Regulation and TSD Warning Event


Figure 11. Timer Regulation Sequence During $2 \Omega$ Overload


Figure 12. Direct Short on OUT Pin


Figure 13. From Timer Regulation to Load Removal Sequence


Figure 14. From No Load to Direct Short Circuit


Figure 15. Reverse Voltage Detection


Figure 16. Reverse Voltage Removal


Figure 17. Undervoltage Threshold (Falling) and Hysteresis


Figure 18. Standby Current vs Vin

High-Level Output Supply Current vs Vin


Figure 19. Quiescent Current vs Vin

TSOP Package


Figure 20. R $_{\text {DS(on) }}$ vs Temperature, TSOP Package


Figure 21. R $_{\text {DS(on) }}$ vs Temperature, $\mu \mathrm{DFN}$ Package

## FUNCTIONAL DESCRIPTION

## Overview

The NCP380 is a high side $P$ channel MOSFET power distribution switch designed to protect the input supply voltage in case of heavy capacitive loads, short circuit or over current. In addition, the high side MOSFET is turned off during under voltage, thermal shutdown or reverse voltage condition. Adjustable version allows the user to program the current limit threshold using an external resistor. Thanks to the soft start circuitry, NCP380 is able to limit large current and voltage surges.

## Overcurrent Protection

NCP380 switches into a constant current regulation mode when the output current is above the $\mathrm{I}_{\mathrm{OCP}}$ threshold. Depending on the load, the output voltage is decreased accordingly.

- In case of hot plug with heavy capacitive load, the output voltage is brought down to the capacitor voltage. The NCP380 will limit the current to the $\mathrm{I}_{\mathrm{OCP}}$ threshold value until the charge of the capacitor is completed.



Figure 22. Heavy capacitive load

- In case of overload, the current is limited to the $\mathrm{I}_{\mathrm{OCP}}$ value and the voltage value is reduced according to the load by the following relation:

$$
\begin{equation*}
V_{O U T}=R_{\text {LOAD }} \times I_{O C P} \tag{eq.1}
\end{equation*}
$$



Figure 23. Overload

- In case of short circuit or huge load, the current is limited to the $\mathrm{I}_{\mathrm{OCP}}$ value within $\mathrm{T}_{\mathrm{DET}}$ time until the short condition is removed. If the output remains shorted or tied to a very low voltage, the junction temperature of the chip exceeds $\mathrm{T}_{\text {SDOCP }}$ value and the
device enters in thermal shutdown (MOSFET is turned-off).


Figure 24. Short circuit

Then, the device enters in timer regulation mode, described in 2 phases:

- Off-phase: Power MOSFET is off during $\mathrm{T}_{\mathrm{OCP}}$ to allow the die temperature to drop.
- On-phase: regulation current mode during $\mathrm{T}_{\text {REG. }}$. The current is regulated to the $\mathrm{I}_{\mathrm{OCP}}$ level.
The timer regulation mode allows the device to handle high thermal dissipation (in case of short circuit for example) within temperature operating condition.

NCP380 stays in on-phase/off-phase loop until the over current condition is removed or enable pin is toggled.

Remark: Other regulation modes can be available for different applications. Please contact our onsemi representative for availability.

## FLAG Indicator

The $\overline{\text { FLAG }}$ pin is an open-drain MOSFET asserted low during over current, reverse-voltage or over temperature conditions. When an over current or a reverse voltage fault is detected on the power path, FLAG pin is asserted low at the end of the associate deglitch time (see electrical characteristics). Thanks to this feature, the FLAG pin is not tied low during the charge of a heavy capacitive load or a voltage transient on output. Deglitch time is $\mathrm{T}_{\mathrm{FOCP}}$ for over current fault and $\mathrm{T}_{\text {REV }}$ for reverse voltage. The $\overline{\text { FLAG }}$ pin remains low until the fault is removed. Then, the $\overline{\text { FLAG }}$ pin goes high at the end of $\mathrm{T}_{\mathrm{FGL}}$.

## Undervoltage Lock-out

Thanks to a built-in under voltage lockout (UVLO) circuitry, the output remains disconnected from input until $\mathrm{V}_{\text {IN }}$ voltage is below $\mathrm{V}_{\text {UVLO }}$. When $\mathrm{V}_{\text {IN }}$ voltage is above $\mathrm{V}_{\text {UVLO }}$, the system try to reconnect the output after a rearming time. $\mathrm{T}_{\text {RUVLO }}$. This circuit has a $\mathrm{V}_{\text {HYST }}$ hysteresis witch provides noise immunity to transient.

## Thermal Sense

Thermal shutdown turns off the power MOSFET if the die temperature exceeds $\mathrm{T}_{\mathrm{SD}}$. A Hysteresis prevents the part from turning on until the die temperature cools at $\mathrm{T}_{\mathrm{RSD}}$.

## Reverse Voltage Protection

When the output voltage exceeds the input voltage by $\mathrm{V}_{\text {REV }}$ voltage during $\mathrm{T}_{\text {REV }}$, the reverse voltage circuitry disconnects the output in order to protect the power supply. The same time $\mathrm{T}_{\mathrm{REV}}$ is needed to turn on again the power MOS plus a rearming time $\mathrm{T}_{\text {RREV }}$.

## Enable Input

Enable pin must be driven by a logic signal (CMOS or TTL compatible) or connected to the GND. $\mathrm{V}_{\text {IN }}$ and EN should not be connected together directly. $\mathrm{V}_{\text {IN }}$ should be
well established and stablized prior to enabling the IC. If no separate EN signal is available, a $10 \mathrm{k} \Omega / 100 \mathrm{nF}$ RC network can be added between $\mathrm{V}_{\text {IN }}$ and EN to delay the EN signal. A logic low on $\overline{\mathrm{EN}}$ or high on EN turns-on the device. A logic high on $\overline{\mathrm{EN}}$ or low on EN turns off device and reduces the current consumption down to $\mathrm{I}_{\text {INOFF }}$.

## Blocking Control

The blocking control circuitry switches the bulk of the power MOS. When the part is off, the body diode limits the leakage current $\mathrm{I}_{\mathrm{REV}}$ from OUT to IN. In this mode, anode of the body diode is connected to IN pin and cathode is connected to OUT pin. In operating condition, anode of the body diode is connected to OUT pin and cathode is connected to IN pin preventing the discharge of the power supply.

## APPLICATION INFORMATION

## Power Dissipation

The junction temperature of the device depends on different contributing factors such as board layout, ambient temperature, device environment, etc... Yet, the main contributor in terms of junction temperature is the power dissipation of the power MOSFET. Assuming this, the power dissipation and the junction temperature in normal mode can be calculated with the following equations:

$$
\begin{equation*}
R_{D}=R_{D S(\text { on })} \times\left(I_{\text {OUT }}\right)^{2} \tag{eq.2}
\end{equation*}
$$

Where:

| $\mathrm{P}_{\mathrm{D}}$ | $=$ Power dissipation (W) |
| :--- | :--- |
| $\mathrm{R}_{\mathrm{DS}(\text { on })}$ | $=\operatorname{Power} \operatorname{MOSFET}$ on resistance $(\Omega)$ |
| $\mathrm{I}_{\mathrm{OUT}}$ | $=$ Output current (A) |
|  | $T_{J}=P_{D} \times R_{\theta J A}+T_{A}$ |

Where:

| $\mathrm{T}_{\mathrm{J}}$ | $=$ Junction temperature $\left({ }^{\circ} \mathrm{C}\right)$ |
| :--- | :--- |
| $\mathrm{R}_{\theta \mathrm{JA}}$ | $=$ Package thermal resistance $\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$ |
| $\mathrm{T}_{\mathrm{A}}$ | $=$ Ambient temperature $\left({ }^{\circ} \mathrm{C}\right)$ |

Power dissipation in regulation mode can be calculated by taking into account the drop $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}$ link to the load by the following relation:

$$
P_{D}=\left(V_{I N}-R_{L O A D} \times I_{O C P}\right) \times I_{O C P}
$$

Where:
$\mathrm{P}_{\mathrm{D}} \quad=$ Power dissipation (W)
$\mathrm{V}_{\text {IN }} \quad=$ Input Voltage $(\mathrm{V})$
$\mathrm{R}_{\text {LOAD }} \quad=$ Load Resistance $(\Omega)$
$\mathrm{I}_{\mathrm{OCP}} \quad=$ Output regulated current (A)

## Adjustable Current-Limit Programming (for adjustable version only)

The NCP380xMUAJAA and NCP380xSNAJAA, respectively $\mu \mathrm{DFN}$ and TSOP6 packages, are proposed to have current limit flexibility for end Customer. Indeed, Ilim pin is available to connect pull down resistor to ground, which participate to the current threshold adjustment. It's strongly recommended to use 0.1 or $1 \%$ resistor tolerance to keep the over current accuracy.

For this resistance selection, Customer should define first of all, the USB current to sustain, without the device enters in the protection sequence. Main rule is to select this pull down resistor in order to make sure min current limit is above the USB current to provide continuously to the upstream accessory.

Following, the main table selection contains the USB current port for the accessory, the standard resistor selection and typical/max over current threshold.

Table 5. RESISTOR SELECTION FOR ADJUSTABLE CURRENT LIMIT VERSION

| Min Current Limit Value (A) | Theoric Resistor Value ( $\mathrm{k} \Omega$ ) | Selected Resistor Value $\begin{gathered} \text { (kS) } \\ 1 \% \text { or 0.1\% } \end{gathered}$ | Typical OCP Target Value <br> (A) | Maximum Current Value <br> (A) |
| :---: | :---: | :---: | :---: | :---: |
| 0.5 | 44.2 | 44.2 | 0.59 | 0.67 |
| 0.6 | 37.5 | 37.4 | 0.71 | 0.81 |
| 0.7 | 32.2 | 31.6 | 0.825 | 0.95 |
| 0.8 | 27.7 | 27.4 | 0.94 | 1.08 |
| 0.9 | 24.0 | 23.7 | 1.06 | 1.22 |
| 1.0 | 21.0 | 21 | 1.18 | 1.35 |
| 1.1 | 18.5 | 18.2 | 1.3 | 1.49 |
| 1.2 | 16.6 | 16.5 | 1.41 | 1.62 |
| 1.3 | 14.6 | 14.3 | 1.53 | 1.76 |
| 1.4 | 13.0 | 13 | 1.65 | 1.9 |
| 1.5 | 11.4 | 11.3 | 1.78 | 2.05 |
| 1.6 | 10.4 | 10.2 | 1.88 | 2.17 |
| 1.7 | 9.2 | 9.09 | 2.01 | 2.31 |
| 1.8 | 8.3 | 8.25 | 2.12 | 2.438 |
| 1.9 | 7.4 | 7.32 | 2.23 | 2.56 |
| 2.0 | 6.5 | 6.49 | 2.36 | 2.7 |
| 2.1 | 5.6 | 5.49 | 2.48 | 2.85 |

The "Min current limit Value" column, represents the DC current to provide to the accessory without over current activation.

$$
\begin{equation*}
R \lim =-5.2959 \times I L I M^{5}+45.256 \times I L I M^{4}-155.25 \times I L I M^{3}+274.39 \times I L I M^{2}-267.6 \times I L I M+134.21 \tag{eq.5}
\end{equation*}
$$



Figure 25. R LIM Curve vs. Current Limit

## NCP380, NCV380

When the resistor is choosing to fit with the Customer application, the limits of the over current threshold can be calculated with the following formula:

$$
\begin{align*}
\text { IOCP min } & =1.6915129-0.0330328 \times \text { Rlim }+0.0011207(\text { Rlim }-22.375)^{2}-0.0000451 \times(\text { Rlim }-22.375)^{3}+\quad(\mathrm{eq.6})  \tag{eq.6}\\
& +0.0000009 \times(\text { Rlim }-22.375)^{4} \\
\text { IOCP max } & =2.2885175-0.0446914 \times \text { Rlim }+0.0015163(\text { Rlim }-22.375)^{2}-0.000061 \times(\text { Rlim }-22.375)^{3}+\quad(\mathrm{eq.} 7)  \tag{eq.7}\\
& +0.0000012 \times(\text { Rlim }-22.375)^{4} \\
\text { IOCPtyp } & =1.9900152-0.0388621 \times \text { Rlim }+0.0013185(\text { Rlim }-22.375)^{2}-0.0000531 \times(\text { Rlim }-22.375)^{3}+\quad \text { (eq. 8) } \\
& +0.0000011 \times(\text { Rlim }-22.375)^{4}
\end{align*}
$$

The minimum, typical and maximum current curves are described in the following graph:


Figure 26. Current Threshold vs. Rlim Resistor

That is recommended to respect $6 \mathrm{k} \Omega-47 \mathrm{k} \Omega$ resistor range for two reasons.

For the low resistor values, the current limit is pushed up to high current level. Due to internal power dissipation capability, a maximum of 2.4 A typical can be set for the $\mu$ DFN package if thermal consideration are respected. For the TSOP6 version 1.2 A is the maximum recommended value because the part could enter in thermal shutdown mode before constant current regulation mode.

In the other side, if we want to keep $15 \%$ of accuracy, high resistor values can be used up to $50 \mathrm{k} \Omega$. With higher value, the current threshold is lower than 500 mA , so in this case degraded accuracy can be observed.

## PCB Recommendations

The NCP380 integrates a PMOS FET rated up to 2 A , and the PCB design rules must be respected to properly evacuate the heat out of the silicon. The UDFN6 PAD1 must be connected to ground plane to increase the heat transfer if necessary. This pad must be connected to ground plane. By increasing PCB area, the $\mathrm{R}_{\theta \mathrm{JA}}$ of the package can be decreased, allowing higher power dissipation.


Figure 27. USB Host Typical Application

Table 6. ORDERING INFORMATION

| Device | Marking | Active <br> Enable Level | Over Current Limit | Evaluation Board | UL Listed | CB <br> Scheme | Package | Shipping ${ }^{\dagger}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| NCP380LSNAJAAT1G | AAC | Low | Adj. | NCP380LSNAJAGEVB | Y | Y | $\begin{gathered} \text { TSOP-6 } \\ \text { (Pb-Free) } \end{gathered}$ | $\begin{gathered} 3,000 \\ \text { Tape / Reel } \end{gathered}$ |
| NCP380LSN05AAT1G | AC5 |  | 0.5 A | NCP380LSN05AGEVB | Y | Y | TSOP 5 |  |
| NCP380LSN10AAT1G | AC6 |  | 1.0 A | NCP380LSN10AGEVB | Y | Y | (Pb-Free) |  |
| NCP380LMUAJAATBG | AA |  | Adj. | NCP380LMUAJAGEVB | Y | Y | UDFN6 (Pb-Free) |  |
| NCV380LMUAJAATBG* | AN |  | Adj. | NCP380LMUAJAGEVB | N | N |  |  |
| NCP380LMU05AATBG | AE |  | 0.5 A | NCP380LMU05AGEVB | Y | Y |  |  |
| NCP380HSNAJAAT1G | AAD | High | Adj. | NCP380HSNAJAGEVB | Y | Y | $\begin{aligned} & \hline \text { TSOP-6 } \\ & \text { (Pb-Free) } \end{aligned}$ |  |
| NCP380HSN05AAT1G | AC7 |  | 0.5 A | NCP380HSN05AGEVB | Y | Y | $\begin{gathered} \text { TSOP-5 } \\ \text { (Pb-Free) } \end{gathered}$ |  |
| NCP380HSN10AAT1G | ADA |  | 1.0 A | NCP380HSN10AGEVB | Y | Y |  |  |
| NCP380HMUAJAATBG | AC |  | Adj. | NCP380HMUAJAGEVB | Y | Y | UDFN6 (Pb-Free) |  |
| NCV380HMUAJAATBG* | AP |  | Adj. | NCP380HMUAJAGEVB | N | N |  |  |
| NCP380HMU05AATBG | AH |  | 0.5 A | NCP380HMU05AGEVB | Y | Y |  |  |
| NCP380HMU10AATBG | AJ |  | 1.0 A | NCP380HMU10AGEVB | Y | Y |  |  |
| NCP380HMU15AATBG | AK |  | 1.5 A | NCP380HMU15AGEVB | Y | Y |  |  |
| NCP380HMU20AATBG | AM |  | 2.0 A | NCP380HMU20AGEVB | Y | Y |  |  |
| NCP380HMU21AATBG | AU |  | 2.1 A | NCP380HMU21AGEVB | Y | Y |  |  |

$\dagger$ For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable


TSOP-6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W
DATE 26 FEB 2024


NDTES:

1. DIMENSIDNING AND TULERANCING PER ASME Y14.5M, 2018.
2. CINTRILLING DIMENSIUN: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS $\square F$ BASE MATERIAL,
4. DIMENSIUNS D AND E1 DI NDT INCLUDE MILD FLASH,

PRZTRUSIINS, $\square R$ GATE BURRS. MILD FLASH, PRUTRUSIDNS, $\quad$ RR GATE BURRS SHALL NDT EXCEED 0.15 PER SIDE, DIMENSIDNS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN 1 INDICATQR MUST BE LDCATED IN THE INDICATED ZENE


| MILLIMETERS |  |  |  |
| :---: | :---: | :---: | :---: |
| DIM | MIN | NLM | MAX |
| A | 0.90 | 1.00 | 1.10 |
| A1 | 0.01 | 0.06 | 0.10 |
| A己 | 0.80 | 0.90 | 1.00 |
| b | 0.25 | 0.38 | 0.50 |
| C | 0.10 | 0.18 | 0.26 |
| D | 2.90 | 3.00 | 3.10 |
| E | 2.50 | 2.75 | 3.00 |
| E1 | 1.30 | 1.50 | 1.70 |
| e | 0.85 | 0.95 | 1.05 |
| L | 0.20 | 0.40 | 0.60 |
| L2 | 0.25 BSC |  |  |
| M | $0^{\circ}$ | --- | $10^{\circ}$ |



RECDMMENDED MLUNTING FEDTPRINT
*For additional information on our Pb-Free strategy and soldering details, please download th e ZN Semiconductor Soldering and Mounting Techniques Reference manual, SLLDERRM/D.

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TSOP-6 $3.00 \times 1.50 \times 0.90,0.95 \mathrm{P}$
CASE 318 G
ISSUE $W$
DATE 26 FEB 2024

GENERIC
MARKING DIAGRAM*


IC
XXX = Specific Device Code
A =Assembly Location
Y = Year
W = Work Week

- = Pb-Free Package
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " $\mathrm{\square}$ ", may or may not be present. Some products may not follow the Generic Marking.
STYLE 1:
PIN 1. DRAIN

2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN
STYLE 2:
PIN 1. EMITTER 2
7. BASE 1
8. COLLECTOR 1
9. EMITTER 1
10. BASE 2
11. COLLECTOR 2
STYLE 3:
PIN 1. ENABLE
12. N/C
13. R BOOST
14. Vz
15. V in
16. V out
STYLE 4:
PIN 1. N/C
17. V in
18. NOT USED
19. GROUND
20. ENABLE
21. LOAD
STYLE 5:
PIN 1. EMITTER 2
22. BASE 2
23. COLLECTOR 1
24. EMITTER 1
25. BASE 1
26. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
2. COLLE
3. BASE
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

## STYLE 7:

PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

STYLE 9
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10
PIN 1. D(OUT)+
2. GND
3. D(OUT)-
4. D(IN)-
5. VBUS
6. $\mathrm{D}(\mathrm{IN})+$

STYLE 16:
STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. $\mathrm{I} / \mathrm{O}$
4. I/O
5. VCC
6. I/O

STYLE 15:
PIN 1. ANODE/CATHODE
PIN 1. ANODE 2. SOURCE 3. GATE 4. DRAIN
5. N/C 6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

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| ---: | :--- | :--- | :--- |
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[^2]

TSOP-5
CASE 483
ISSUE N
SCALE 2:1
DATE 12 AUG 2020
*For additional information on our Pb -Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.


- H

C seating
SIDE VIEW

END VIEW

NOTES

1. DIMENSIONING AND TOLERANCING PER ASME

Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH

THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD

FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

| DIM | MILLIMETERS |  |
| :---: | :---: | :---: |
|  | MIN | MAX |
| A | 2.85 | 3.15 |
| B | 1.35 | 1.65 |
| $\mathbf{C}$ | 0.90 | 1.10 |
| $\mathbf{D}$ | 0.25 | 0.50 |
| $\mathbf{G}$ | 0.95 | BSC |
| $\mathbf{H}$ | 0.01 | 0.10 |
| $\mathbf{J}$ | 0.10 | 0.26 |
| $\mathbf{K}$ | 0.20 | 0.60 |
| $\mathbf{M}$ | $0^{\circ}$ | $10^{\circ}$ |
| $\mathbf{S}$ | 2.50 | 3.00 |

GENERIC MARKING DIAGRAM*

Analog

XXX = Specific Device Code
A = Assembly Location
X = Specific Device Code
M = Date Code

- = Pb-Free Package

W = Work Week

- = Pb-Free Package
(Note: Microdot may be in either location)
*This information is generic. Please refer to device data sheet for actual part marking. $\mathrm{Pb}-$ Free indicator, " $G$ " or microdot " $-{ }^{-}$", may or may not be present. Some products may not follow the Generic Marking.

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[^3]

UDFN6 2x2, 0.65P
CASE 517AB
ISSUE C
DATE 10 APR 2013
SCALE 4:1

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 2. CONTROLLING DIMENSION: MILLIMETERS.
2. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
3. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
4. TIE BARS MAY BE VIIIBLE IN THIS VIEW AND ARE CONNECTED TO THE THERMAL PAD

|  | MILLIMETERS |  |
| :---: | :---: | :---: |
| DIM | MIN | MAX |
| A | 0.45 | 0.55 |
| A1 | 0.00 | 0.05 |
| A3 | 0.127 |  |
| R REF |  |  |
| b | 0.25 |  |
| D | 0.35 |  |
| D2 | 1.50 |  |
| E | BSC |  |
| E | 2.00 |  |
| E2 | 0.80 |  |
| BSC | 1.00 |  |
| L | 0.65 BSC |  |
| L | 0.25 | 0.35 |
| L1 | --- | 0.15 |

GENERIC
DETAIL B
ALTERNATE CONSTRUCTIONS



DETAILA ALTERNATE TERMINAL CONSTRUCTIONS

MARKING DIAGRAM*


XX = Specific Device Code
M = Date Code

- = Pb-Free Package
(Note: Microdot may be in either location)
*This information is generic. Please refer to device data sheet for actual part marking. $\mathrm{Pb}-$ Free indicator, "G" or microdot " $\stackrel{\text { ", }}{ }$ may or may not be present.


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