NCP361, NCV361

USB Positive Overvoltage Protection Controller with Internal PMOS FET and Overcurrent Protection

The NCP361 disconnects systems at its output when wrong VBUS operating conditions are detected at its input. The system is positive over-voltage protected up to +20 V.

Thanks to an integrated PMOS FET, no external device is necessary, reducing the system cost and the PCB area of the application board.

The NCP361 is able to instantaneously disconnect the output from the input if the input voltage exceeds the overvoltage threshold (5.675 V). Thanks to an overcurrent protection, the integrated PMOS is turning off when the charge current exceeds current limit (see options in ordering information).

The NCP361 provides a negative going flag (FLAG) output, which alerts the system that voltage, current or overtemperature faults have occurred.

In addition, the device has ESD-protected input (15 kV Air) when bypassed with a 1 µF or larger capacitor.

Features
• Overvoltage Protection up to 20 V
• On-chip PMOS Transistor
• Overvoltage Lockout (OVLO)
• Undervoltage Lockout (UVLO)
• Overcurrent Protection
• Alert FLAG Output
• EN Enable Pin
• Thermal Shutdown
• Compliance to IEC61000–4–2 (Level 4)
  8 kV (Contact)
  15 kV (Air)
• ESD Ratings:
  Machine Model = B
  Human Body Model = 2
• UDFN6 2x2 mm and TSOP–5 3x3 mm Packages
• NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
• This is a Pb–Free Device

Applications
• USB Devices
• Mobile Phones
• Peripheral
• Personal Digital Applications
• MP3 Players
• Set Top Boxes

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.
NCP361, NCV361

Figure 1. Typical Application Circuit (UDFN Pinout)

Figure 2. Functional Block Diagram

PIN FUNCTION DESCRIPTION (UDFN Package)

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>EN</td>
<td>INPUT</td>
<td>Enable Pin. The device enters in shutdown mode when this pin is tied to a high level. In this case the output is disconnected from the input. To allow normal functionality, the EN pin shall be connected to GND or to a I/O pin. This pin does not have an impact on the fault detection.</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>POWER</td>
<td>Ground</td>
</tr>
<tr>
<td>3</td>
<td>IN</td>
<td>POWER</td>
<td>Input Voltage Pin. This pin is connected to the VBUS. A 1 μF low ESR ceramic capacitor, or larger, must be connected between this pin and GND.</td>
</tr>
<tr>
<td>4, 5</td>
<td>OUT</td>
<td>OUTPUT</td>
<td>Output Voltage Pin. The output is disconnected from the VBUS power supply when the input voltage is above OVLO threshold or below UVLO threshold. A 1 μF capacitor must be connected to these pins. The two OUT pins must be hardwired to common supply.</td>
</tr>
<tr>
<td>6</td>
<td>FLAG</td>
<td>OUTPUT</td>
<td>Fault Indication Pin. This pin allows an external system to detect a fault on VBUS pin. The FLAG pin goes low when input voltage exceeds OVLO threshold. Since the FLAG pin is open drain functionality, an external pull up resistor to VCC must be added.</td>
</tr>
</tbody>
</table>

PIN FUNCTION DESCRIPTION (TSOP−5 Package)

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>IN</td>
<td>POWER</td>
<td>Input Voltage Pin. This pin is connected to the VBUS. A 1 μF low ESR ceramic capacitor, or larger, must be connected between this pin and GND.</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>POWER</td>
<td>Ground</td>
</tr>
<tr>
<td>3</td>
<td>EN</td>
<td>INPUT</td>
<td>Enable Pin. The device enters in shutdown mode when this pin is tied to a high level. In this case the output is disconnected from the input. To allow normal functionality, the EN pin shall be connected to GND or to a I/O pin. This pin does not have an impact on the fault detection.</td>
</tr>
<tr>
<td>4</td>
<td>FLAG</td>
<td>OUTPUT</td>
<td>Fault Indication Pin. This pin allows an external system to detect a fault on VBUS pin. The FLAG pin goes low when input voltage exceeds OVLO threshold. Since the FLAG pin is open drain functionality, an external pull up resistor to VCC must be added.</td>
</tr>
<tr>
<td>5</td>
<td>OUT</td>
<td>OUTPUT</td>
<td>Output Voltage Pin. The output is disconnected from the VBUS power supply when the input voltage is above OVLO threshold or below UVLO threshold. A 1 μF capacitor must be connected to this pin.</td>
</tr>
</tbody>
</table>

NOTE: Pin out provided for concept purpose only and might change in the final product.
# MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum Voltage (IN to GND)</td>
<td>Vmin</td>
<td>−0.3</td>
<td>V</td>
</tr>
<tr>
<td>Minimum Voltage (All others to GND)</td>
<td>Vmin</td>
<td>−0.3</td>
<td>V</td>
</tr>
<tr>
<td>Maximum Voltage (IN to GND)</td>
<td>Vmax</td>
<td>21</td>
<td>V</td>
</tr>
<tr>
<td>Maximum Voltage (All others to GND)</td>
<td>Vmax</td>
<td>7.0</td>
<td>V</td>
</tr>
<tr>
<td>Maximum DC Current from Vin to Vout (PMOS) (Note 1)</td>
<td>I MAX</td>
<td>600</td>
<td>mA</td>
</tr>
<tr>
<td>Thermal Resistance, Junction-to-Air</td>
<td>RthJA</td>
<td>305</td>
<td>°C/W</td>
</tr>
<tr>
<td>Operating Ambient Temperature Range</td>
<td>TAMB</td>
<td>−40 to +85</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>TSTG</td>
<td>−65 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>Junction Operating Temperature</td>
<td>TJ</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>ESD Withstand Voltage (IEC 61000–4–2)</td>
<td>Vesd</td>
<td>15 Air, 8.0 Contact</td>
<td>kV</td>
</tr>
<tr>
<td>Human Body Model (HBM), Model = 2 (Note 2)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Machine Model (MM) Model = B (Note 3)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Moisture Sensitivity</td>
<td>MSL</td>
<td>Level 1</td>
<td>–</td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. With minimum PCB area. By decreasing RthJA, the current capability increases. See PCB recommendation page 9.
2. Human Body Model, 100 pF discharged through a 1.5 kΩ resistor following specification JESD22/A114.
## ELECTRICAL CHARACTERISTICS

(Min/Max limits values (−40°C < TA < +85°C) and Vin = +5.0 V. Typical values are TA = +25°C, unless otherwise noted.)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage Range</td>
<td>VIN</td>
<td></td>
<td>1.2</td>
<td>20</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Undervoltage Lockout Threshold</td>
<td>UVLO</td>
<td>VIN falls down UVLO threshold</td>
<td>2.85</td>
<td>3.0</td>
<td>3.15</td>
<td>V</td>
</tr>
<tr>
<td>Undervoltage Lockout Hysteresis</td>
<td>UVLOHyst</td>
<td></td>
<td>50</td>
<td>70</td>
<td>90</td>
<td>mV</td>
</tr>
<tr>
<td>Overvoltage Lockout Threshold</td>
<td>OVLO</td>
<td>VIN rises up OVLO threshold</td>
<td>5.43</td>
<td>5.675</td>
<td>5.9</td>
<td>V</td>
</tr>
<tr>
<td>Overvoltage Lockout Hysteresis</td>
<td>OVLOHyst</td>
<td></td>
<td>50</td>
<td>100</td>
<td>125</td>
<td>mV</td>
</tr>
<tr>
<td>VIN versus Vout Dropout</td>
<td>VDROP</td>
<td>VIN = 5 V, I charge = 500 mA</td>
<td>150</td>
<td>200</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Overcurrent Limit</td>
<td>Ilim</td>
<td>Vout = 5 V</td>
<td>550</td>
<td>750</td>
<td>950</td>
<td>mA</td>
</tr>
<tr>
<td>Supply Quiescent Current</td>
<td>IDD</td>
<td>No Load, VIN = 5.25 V</td>
<td>20</td>
<td>35</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>Standby Current</td>
<td>ISTD</td>
<td>VIN = 5 V, EN = 1.2 V</td>
<td>26</td>
<td>37</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>Zero Gate Voltage Drain Current</td>
<td>IDSS</td>
<td>VDS = 20 V, VGS = 0 V</td>
<td>0.08</td>
<td></td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>FLAG Output Low Voltage</td>
<td>VOflag</td>
<td>VIN &gt; OVLO, sink 1 mA on FLAG pin</td>
<td>400</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FLAG Leakage Current</td>
<td>FLAGleak</td>
<td>FLAG level = 5 V</td>
<td>5.0</td>
<td>nA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN Voltage High</td>
<td>VHI</td>
<td>VIN from 3.3 V to 5.5 V</td>
<td>1.2</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN Voltage Low</td>
<td>VIL</td>
<td>VIN from 3.3 V to 5.5 V</td>
<td>0.55</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN Leakage Current</td>
<td>ENleak</td>
<td>EN = 5.5 V or GND</td>
<td>170</td>
<td>nA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### TIMINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Start Up Delay</td>
<td>tON</td>
<td>From VIN &gt; UVLO to Vout = 0.8xVIN, See Fig 3 &amp; 9</td>
<td>4.0</td>
<td></td>
<td>15</td>
<td>ms</td>
</tr>
<tr>
<td>FLAG going up Delay</td>
<td>tSTART</td>
<td>From VIN &gt; UVLO to FLAG = 1.2 V, See Fig 3 &amp; 10</td>
<td>3.0</td>
<td></td>
<td>15</td>
<td>µs</td>
</tr>
<tr>
<td>Output Turn Off Time</td>
<td>TOFF</td>
<td>From VIN &gt; OVLO to Vout ≤ 0.3 V, See Fig 4 &amp; 11</td>
<td>0.7</td>
<td></td>
<td>1.5</td>
<td>µs</td>
</tr>
<tr>
<td>Alert Delay</td>
<td>TSTOP</td>
<td>From VIN &gt; OVLO to FLAG ≤ 0.4 V, See Fig 4 &amp; 12</td>
<td>1.0</td>
<td></td>
<td>1.5</td>
<td>µs</td>
</tr>
<tr>
<td>Disable Time</td>
<td>TDIS</td>
<td>From EN 0.4 to 1.2V to Vout ≤ 0.3 V, See Fig 5 &amp; 13</td>
<td>3.0</td>
<td></td>
<td>1.5</td>
<td>µs</td>
</tr>
<tr>
<td>Thermal Shutdown Temperature</td>
<td>TSD</td>
<td>VIN = 4.75 V, No output capacitor.</td>
<td>150</td>
<td></td>
<td></td>
<td>ºC</td>
</tr>
<tr>
<td>Thermal Shutdown Hysteresis</td>
<td>TSDHyst</td>
<td>Vout ≤ 0.3 V, See Fig 4 &amp; 11</td>
<td>30</td>
<td></td>
<td></td>
<td>ºC</td>
</tr>
</tbody>
</table>
Figure 3. Start Up Sequence

Figure 4. Shutdown on Over Voltage Detection

Figure 5. Disable on \( EN = 1 \)

Figure 6. FLAG Response with \( EN = 1 \)

Figure 7.

Figure 8.

TYPICAL OPERATING CHARACTERISTICS
Figure 9. Start Up. Vin=Ch1, Vout=Ch2

Figure 10. FLAG Going Up Delay. Vin=Ch1, FL:AG=Ch3

Figure 11. Output Turn Off time. Vin=Ch1, Vout=Ch2

Figure 12. Alert Delay. Vout=Ch1, FLAG=Ch3

Figure 13. Disable Time. EN=Ch4, Vin=Ch1, Vout=Ch2

Figure 14. Thermal Shutdown. Vin=Ch1, Vout=Ch2, FLAG=Ch3
NCP361, NCV361

TYPICAL OPERATING CHARACTERISTICS

Figure 15. \( R_{DS(on)} \) vs. Temperature
(Load = 500 mA)

Figure 16. Output Short Circuit

Figure 17. Quiescent Current vs. Input Voltage

Figure 18. Overcurrent Protection Threshold
vs. Temperature

Figure 19. Overcurrent Protection Threshold
vs. Input Voltage
Operation
NCP361 provides overvoltage protection for positive voltage, up to 20 V. A PMOS FET protects the systems (i.e., VBUS) connected on the Vout pin, against positive overvoltage. The output follows the VBUS level until OVLO threshold is overtaken.

Undervoltage Lockout (UVLO)
To ensure proper operation under any conditions, the device has a built-in undervoltage lock out (UVLO) circuit. During Vin positive going slope, the output remains disconnected from input until Vin voltage is above 3.0 V nominal. The FLAGV output is pulled to low as long as Vin does not reach UVLO threshold. This circuit has a 70 mV hysteresis to provide noise immunity to transient conditions.

Overvoltage Lockout (OVLO)
To protect connected systems on Vout pin from overvoltage, the device has a built-in overvoltage lock out (OVLO) circuit. During overvoltage condition (OVLO exceeds), the output remains disabled and FLAG is tied low, as long as the input voltage is higher than OVLO – hysteresis. This circuit has a 100 mV hysteresis to provide noise immunity to transient conditions.

Overcurrent Protection (OCP)
The NCP361 integrates overcurrent protection to prevent system/battery overload or defect. The current limit threshold is internally set at 750 mA. This value can be changed from 150 mA to 750 mA by a metal tweak, please contact your ON Semiconductor representative for availability. During current fault, the internal PMOS FET is automatically turned off (5 μs) if the charge current exceeds Ilim. NCP361 goes into turn on and turn off mode as long as defect is present. The internal ton delay (4 ms typical) allows limiting thermal dissipation. The Flag pin goes to low level when an overcurrent fault appears. That allows the microcontroller to count defect events and turns off the PMOS with EN pin.

FLAG Output
NCP361 provides a FLAG output, which alerts external systems that a fault has occurred. This pin is tied to low as soon as: 1.2 V < Vin < UVLO, Vin > OVLO, Icharge > Ilimit. TJ ≥ 150°C. When NCP361 recovers normal condition, FLAG is held high. The pin is an open drain output, thus a pull up resistor (typically 1 MΩ – Minimum 10 kΩ) must be provided to VCC. FLAG pin is an open drain output.

EN Input
To enable normal operation, the EN pin shall be forced to low or connected to ground. A high level on the pin disconnects OUT pin from IN pin. EN does not overdrive an OVLO or UVLO fault.

Internal PMOS FET
The NCP361 includes an internal PMOS FET to protect the systems, connected on OUT pin, from positive overvoltage. Regarding electrical characteristics, the RDS(on) during normal operation, will create low losses on Vout pin, characterized by Vin versus Vout dropout.

ESD Tests
The NCP361 fully supports the IEC61000–4–2, level 4 (Input pin, 1 μF mounted on board). That means, in Air condition, Vin has a ±15 kV ESD protected input. In Contact condition, Vin has ±8 kV ESD protected input. Please refer to Figure 22 to see the IEC61000–4–2 electrostatic discharge waveform.
PCB Recommendations

The NCP361 integrates a 500 mA rated PMOS FET, and the PCB rules must be respected to properly evacuate the heat out of the silicon. The UDFN PAD1 must be connected to ground plane to increase the heat transfer if necessary from an application standpoint. Of course, in any case, this pad shall be not connected to any other potential.

By increasing PCB area, the \( R_{JA} \) of the package can be decreased, allowing higher charge current to fill the battery.

Taking into account that internal bondings (wires between package and silicon) can handle up to 1 A (higher than thermal capability), the following calculation shows two different example of current capability, depending on PCB area:

- With 305°C/W (without PCB area), allowing DC current is 500 mA
- With 260°C/W (200 mm²), the charge DC current allows with a 85°C ambient temperature is:

\[
I = \sqrt{\frac{(T_J-T_A)}{R_{JA} \times R_{DSON}}}
\]

\[
I = 625 \text{ mA}
\]

In every case, we recommend to make thermal measurement on final application board to make sure of the final Thermal Resistance.

---

**Figure 22.**

**Figure 23.** Thermal Resistance of UDFN 2x2 and TSOP Packages as a Function of PCB Area and Thickness
**ORDERING INFORMATION**

<table>
<thead>
<tr>
<th>Device</th>
<th>Marking</th>
<th>Package</th>
<th>Shipping†</th>
</tr>
</thead>
<tbody>
<tr>
<td>NCP361MUTBG</td>
<td>AD</td>
<td>UDFN6 (Pb-Free)</td>
<td>3000 / Tape &amp; Reel</td>
</tr>
<tr>
<td>NCP361SNT1G</td>
<td>ACD</td>
<td>TSOP−5 (Pb-Free)</td>
<td>3000 / Tape &amp; Reel</td>
</tr>
<tr>
<td>NCV361SNT1G*</td>
<td>VET</td>
<td>TSOP−5 (Pb-Free)</td>
<td>3000 / Tape &amp; Reel</td>
</tr>
</tbody>
</table>

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements

**SELECTION GUIDE**

Part number is designated as follows:

**NCP361xxxxxTxG**

- **a**
- **b**
- **c**
- **d**
- **e**

<table>
<thead>
<tr>
<th>Code</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>Overcurrent Threshold&lt;br&gt;差点: 750 mA</td>
</tr>
<tr>
<td>b</td>
<td>Package&lt;br&gt;MU: UDFN&lt;br&gt;SN: TSOP−5</td>
</tr>
<tr>
<td>c</td>
<td>UVLO Typical Threshold&lt;br&gt;差点: 3.00 V</td>
</tr>
<tr>
<td>d</td>
<td>OVLO Typical Threshold&lt;br&gt;差点: 5.675 V</td>
</tr>
<tr>
<td>e</td>
<td>Tape &amp; Reel Type&lt;br&gt;B: = 3000&lt;br&gt;1: = 3000</td>
</tr>
</tbody>
</table>
NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

<table>
<thead>
<tr>
<th>DIM</th>
<th>MIN</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.90</td>
<td>1.10</td>
</tr>
<tr>
<td>B</td>
<td>0.01</td>
<td>0.10</td>
</tr>
<tr>
<td>C</td>
<td>0.01</td>
<td>0.10</td>
</tr>
<tr>
<td>D</td>
<td>0.025</td>
<td>0.50</td>
</tr>
<tr>
<td>G</td>
<td>0.95</td>
<td>BSC</td>
</tr>
<tr>
<td>H</td>
<td>0.10</td>
<td>0.26</td>
</tr>
<tr>
<td>J</td>
<td>0.20</td>
<td>0.60</td>
</tr>
<tr>
<td>K</td>
<td>0.20</td>
<td>0.60</td>
</tr>
<tr>
<td>M</td>
<td>0.95</td>
<td>1.10</td>
</tr>
<tr>
<td>S</td>
<td>2.50</td>
<td>3.00</td>
</tr>
</tbody>
</table>

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “•”, may or may not be present. Some products may not follow the Generic Marking.
NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TIE BARS MAY BE VISIBLE IN THIS VIEW AND ARE CONNECTED TO THE THERMAL PAD.

NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TIE BARS MAY BE VISIBLE IN THIS VIEW AND ARE CONNECTED TO THE THERMAL PAD.

NOTES:
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4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
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2. CONTROLLING DIMENSION: MILLIMETERS.
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4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TIE BARS MAY BE VISIBLE IN THIS VIEW AND ARE CONNECTED TO THE THERMAL PAD.

NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TIE BARS MAY BE VISIBLE IN THIS VIEW AND ARE CONNECTED TO THE THERMAL PAD.

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