2A Ultra-Small Controlled Load Switch with Auto-Discharge Path

NCP334, NCP335

The NCP334 and NCP335 are low Ron MOSFET controlled by external logic pin, allowing optimization of battery life, and portable device autonomy.

Indeed, due to a current consumption optimization with PMOS structure, leakage currents are eliminated by isolating connected IC’s on the battery when not used.

Output discharge path is also embedded to eliminate residual voltages on the output rail in the NCP335.

Proposed in wide input voltage range from 1.2 V to 5.5 V, and a very small 0.96 x 0.96 mm WLCSP4, 0.5 mm pitch.

Features
• 1.2 V – 5.5 V Operating Range
• 47 mΩ P MOSFET at 3.3 V
• DC Current Up to 2 A
• Output Auto-discharge (NCP335)
• Active high EN pin
• WLCSP4 0.96 x 0.96 mm
• ESD Ratings: 4 kV Human Body Model, 2 kV CDM, 250 V Machine Model
• These are Pb-Free Devices

Typical Applications
• Mobile Phones
• Tablets
• Digital Cameras
• GPS
• Portable Devices

MARKING DIAGRAM

XX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week

PIN DIAGRAM

ORDERING INFORMATION
See detailed ordering, marking and shipping information on page 9 of this data sheet.
PIN FUNCTION DESCRIPTION

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN</td>
<td>A2</td>
<td>POWER</td>
<td>Load–switch input voltage; connect a 1 μF or greater ceramic capacitor from IN to GND as close as possible to the IC.</td>
</tr>
<tr>
<td>GND</td>
<td>B1</td>
<td>POWER</td>
<td>Ground connection.</td>
</tr>
<tr>
<td>EN</td>
<td>B2</td>
<td>INPUT</td>
<td>Enable input, logic high turns on power switch.</td>
</tr>
<tr>
<td>OUT</td>
<td>A1</td>
<td>OUTPUT</td>
<td>Load–switch output; connect a 1 μF ceramic capacitor from OUT to GND as close as possible to the IC is recommended.</td>
</tr>
</tbody>
</table>

BLOCK DIAGRAM

IN: Pin A2
EN: Pin B2
GND: Pin B1
OUT: Pin A1

Gate driver and soft start control
Control logic
EN block
Optional: NCP335

Figure 1. Typical Application Circuit

Figure 2. Block Diagram
# MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN, OUT, EN, Pins</td>
<td>$V_{EN}, V_{IN}, V_{OUT}$</td>
<td>0.3 to + 7.0</td>
<td>V</td>
</tr>
<tr>
<td>From IN to OUT Pins: Input/Output</td>
<td>$V_{IN}, V_{OUT}$</td>
<td>0 to + 7.0</td>
<td>V</td>
</tr>
<tr>
<td>Maximum Junction Temperature</td>
<td>$T_J$</td>
<td>−40 to + 125</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$T_{STG}$</td>
<td>−40 to + 150</td>
<td>°C</td>
</tr>
<tr>
<td>Human Body Model (HBM) ESD Rating are (Notes 1 and 2)</td>
<td>ESD HBM</td>
<td>4000</td>
<td>V</td>
</tr>
<tr>
<td>Machine Model (MM) ESD Rating are (Notes 1 and 2)</td>
<td>ESD MM</td>
<td>250</td>
<td>V</td>
</tr>
<tr>
<td>Charge Device Model (CDM) ESD Rating are (Notes 1 and 2)</td>
<td>ESD CDM</td>
<td>2000</td>
<td>V</td>
</tr>
<tr>
<td>Latch-up protection (Note 3) − Pins IN, OUT, EN</td>
<td>LU</td>
<td>100</td>
<td>mA</td>
</tr>
<tr>
<td>Moisture Sensitivity (Note 4)</td>
<td>MSL</td>
<td>Level 1</td>
<td></td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. According to JEDEC standard JESD22−A108.
2. This device series contains ESD protection and passes the following tests:
   - Human Body Model (HBM) ±4.0 kV per JEDEC standard: JESD22−A114 for all pins.
   - Machine Model (MM) ±250 V per JEDEC standard: JESD22−A115 for all pins.
   - Charge Device Model (CDM) ±2.0 kV per JEDEC standard: JESD22−C101 for all pins.
3. Latch up Current Maximum Rating: ±100 mA per JEDEC standard: JESD78 class II.

# OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>Operational Power Supply</td>
<td>1.2</td>
<td>5.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{EN}$</td>
<td>Enable Voltage</td>
<td>0</td>
<td>5.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_A$</td>
<td>Ambient Temperature Range</td>
<td>−40</td>
<td>25 to + 85</td>
<td>°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_{IN}$</td>
<td>Decoupling input capacitor</td>
<td>1</td>
<td>μF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_{OUT}$</td>
<td>Decoupling output capacitor</td>
<td>1</td>
<td>μF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{JUA}$</td>
<td>Thermal Resistance Junction to Air</td>
<td>WLCSP package (Note 5)</td>
<td>100</td>
<td>°C/W</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{OUT}$</td>
<td>Maximum DC current</td>
<td>2</td>
<td>A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$P_D$</td>
<td>Power Dissipation Rating (Note 6)</td>
<td>$T_A \leq 25 ^\circ C$</td>
<td>WLCSP package</td>
<td>0.5</td>
<td>W</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_A = 85 ^\circ C$</td>
<td>WLCSP package</td>
<td>0.2</td>
<td>W</td>
<td></td>
</tr>
</tbody>
</table>

5. The $R_{JUA}$ is dependent of the PCB heat dissipation and thermal via.
6. The maximum power dissipation ($P_D$) is given by the following formula:

$$P_D = \frac{T_{J\text{MAX}} - T_A}{R_{JUA}}$$
ELECTRICAL CHARACTERISTICS

Min and Max Limits apply for $T_A$ between $-40^\circ\text{C}$ to $+85^\circ\text{C}$ for $V_{IN}$ between 1.2 V to 5.5 V (Unless otherwise noted). Typical values are referenced to $T_A = +25^\circ\text{C}$ and $V_{IN} = 4$ V (Unless otherwise noted).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{DS(on)}$</td>
<td>Static drain–source on–state resistance</td>
<td>$V_{IN} = 5.5$ V $T_A = 25^\circ\text{C}$, $I = 200$ mA (Note 8)</td>
<td>38</td>
<td>40</td>
<td>m$\Omega$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IN} = 4.2$ V $T_A = 25^\circ\text{C}$, $I = 200$ mA</td>
<td>42</td>
<td>46</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IN} = 3.3$ V $T_A = 25^\circ\text{C}$, $I = 200$ mA</td>
<td>47</td>
<td>52</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IN} = 1.8$ V $T_A = 25^\circ\text{C}$, $I = 200$ mA</td>
<td>76</td>
<td>87</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Full</td>
<td>100</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{DIS}$</td>
<td>Output discharge path</td>
<td>$V_{IN} = 1.2$ V $T_A = 25^\circ\text{C}$, $I = 200$ mA</td>
<td>211</td>
<td>420</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_R$</td>
<td>Output rise time</td>
<td>$V_{IN} = 3.6$ V $C_{LOAD} = 1$ $\mu$F, $R_{LOAD} = 25$ $\Omega$ (Note 7)</td>
<td>71</td>
<td>$\mu$s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_F$</td>
<td>Output fall time</td>
<td>$V_{IN} = 3.6$ V $C_{LOAD} = 1$ $\mu$F, $R_{LOAD} = 25$ $\Omega$ (Note 7)</td>
<td>42</td>
<td>$\mu$s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_{\text{on}}$</td>
<td>Gate turn on</td>
<td>$V_{IN} = 3.6$ V Gate turn on + Output rise time</td>
<td>116</td>
<td>$\mu$s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_{\text{en}}$</td>
<td>Enable time</td>
<td>$V_{IN} = 3.6$ V From EN low to high to $V_{OUT} = 10%$ of fully on</td>
<td>45</td>
<td>$\mu$s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>High–level input voltage</td>
<td></td>
<td>0.9</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Low–level input voltage</td>
<td></td>
<td>0.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{EN}$</td>
<td>Pull down resistor</td>
<td></td>
<td>5</td>
<td>M$\Omega$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

7. Parameters are guaranteed for $C_{LOAD}$ and $R_{LOAD}$ connected to the OUT pin with respect to the ground
8. Guaranteed by design and characterization, not production tested.

TIMINGS

Figure 3. Enable, Rise and fall time
NCP334, NCP335

TYPICAL CHARACTERISTICS

Figure 4. $R_{DS(on)}$ (mΩ) vs. $V_{IN}$ (V)

Figure 5. $R_{DS(on)}$ (mΩ) vs. $I_{OUT}$ (mA) at 3.6 V

Figure 6. $R_{DS(on)}$ (mΩ) vs. Temperature (°C) at 3.3 V, $I_{load}$ 100 mA

Figure 7. $R_{DS(on)}$ (mΩ) vs. Temperature (°C), $I_{load}$ 2 A

Figure 8. Standby Current ($\mu$A) versus $V_{IN}$ (V), No Load

Figure 9. Standby Current ($\mu$A) versus $V_{IN}$ (V), $V_{out}$ Short to GND.

VIN = 5.5 V
VIN = 4.2 V
VIN = 3.6 V
VIN = 3.3 V

Temperature = 0°C
Temperature = 25°C
Temperature = 50°C
Temperature = 85°C
Temperature = 125°C

IN ($\mu$A)
VIN (V)

IN ($\mu$A)
VIN (V)
Figure 10. Quiescent Current (μA) versus $V_{\text{IN}}$ (V), No load.

Figure 11. Enable Time, Rise Time, and Ton Time
FUNCTIONAL DESCRIPTION

Overview
The NCP334 – NCP335 are high side P channel MOSFET power distribution switch designed to isolate ICs connected on the battery in order to save energy. The part can be turned on, with a range of battery from 1.2 V to 5.5 V.

Enable Input
Enable pin is an active high. The path is opened when EN pin is tied low (disable), forcing P MOS switch off. The IN/OUT path is activated with a minimum of Vin of 1.2V and EN forced to high level.

Auto Discharge (NCP335 Only)
NMOS FET is placed between the output pin and GND, in order to discharge the application capacitor connected on OUT pin.

The auto-discharge is activated when EN pin is set to low level (disable state).

The discharge path (Pull down NMOS) stays activated as long as EN pin is set at low level and V_IN > 1.2 V.
In order to limit the current across the internal discharge N-MOSFET, the typical value is set at 65 Ω.

Cin and Cout Capacitors
IN and OUT, 1 μF, at least, capacitors must be placed as close as possible the part for stability improvement.
APPLICATION INFORMATION

Power Dissipation
Main contributor in term of junction temperature is the power dissipation of the power MOSFET. Assuming this, the power dissipation and the junction temperature in normal mode can be calculated with the following equations:

\[ P_D = R_{DS(on)} \times (I_{OUT})^2 \]

- \( P_D \) = Power dissipation (W)
- \( R_{DS(on)} \) = Power MOSFET on resistance (Ω)
- \( I_{OUT} \) = Output current (A)

\[ T_J = P_D \times R_{JA} + T_A \]

- \( T_J \) = Junction temperature (°C)
- \( R_{JA} \) = Package thermal resistance (°C/W)
- \( T_A \) = Ambient temperature (°C)

PCB Recommendations
The NCP334 – NCP335 integrate an up to 2 A rated PMOS FET, and the PCB design rules must be respected to properly evacuate the heat out of the silicon. By increasing PCB area, especially around IN and OUT pins, the \( R_{JA} \) of the package can be decreased, allowing higher power dissipation.

Figure 13. Routing Example 1 oz, 2 Layers, 100°C/W
Example of application definition.

\[ T_J - T_A = R_{iJA} \times Pd = R_{iJA} \times R_{DS(on)} \times I^2 \]

\( T_J \): Junction Temperature.
\( T_A \): Ambient Temperature.
\( R_0 \): Thermal resistance between IC and air, through PCB.
\( R_{DS(on)} \): Intrinsic resistance of the IC MOSFET.
\( I \): load DC current.

Taking into account of \( R_{\theta} \) obtain with:

1 oz, 2 layers: 100°C/W.

At 2 A, 25°C ambient temperature, \( R_{DS(on)} \) 42 mΩ @ \( V_{IN} \) 4.2 V, the junction temperature will be:

\[ T_J = T_A + R_0 \times Pd = 25 + (0.042 \times 2^2) \times 100 = 41.8°C/W \]

Taking into account of \( R_{\theta} \) obtain with:

2 oz, 4 layers: 60°C/W.

At 2 A, 25°C ambient temperature, \( R_{DS(on)} \) 42 mΩ @ \( V_{IN} \) 4.2 V, the junction temperature will be:

\[ T_J = T_A + R_0 \times Pd = 25 + (0.042 \times 2^2) \times 60 = 35°C \]

**ORDERING INFORMATION**

<table>
<thead>
<tr>
<th>Device</th>
<th>Marking</th>
<th>Package</th>
<th>Shipping†</th>
</tr>
</thead>
<tbody>
<tr>
<td>NCP334FCT2G</td>
<td>AD</td>
<td>WLCSP 0.96 x 0.96 mm (Pb–Free)</td>
<td>3000 / Tape &amp; Reel</td>
</tr>
<tr>
<td>NCP335FCT2G</td>
<td>AA</td>
<td>WLCSP 0.96 x 0.96 mm (Pb–Free)</td>
<td>3000 / Tape &amp; Reel</td>
</tr>
</tbody>
</table>

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

**WLCSP4 0.96x0.96x0.609**
CASE 567FG
ISSUE A

**DATE 01 JUL 2022**

**NOTES:**
2. CONTROLLING DIMENSIONS: MILLIMETERS
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.

<table>
<thead>
<tr>
<th>DIM</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>MIN.</td>
</tr>
<tr>
<td>A1</td>
<td>0.219</td>
</tr>
<tr>
<td>A2</td>
<td>0.335</td>
</tr>
<tr>
<td>b</td>
<td>0.282</td>
</tr>
<tr>
<td>D</td>
<td>0.96</td>
</tr>
<tr>
<td>E</td>
<td>0.96</td>
</tr>
<tr>
<td>e</td>
<td>0.56</td>
</tr>
</tbody>
</table>

**DOCUMENT NUMBER:** 98AON79917E
**DESCRIPTION:** WLCSP4 0.96x0.96x0.609

Electronic versions are uncontrolled except when accessed directly from the Document Repository.
Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.

© Semiconductor Components Industries, LLC, 2019
www.onsemi.com

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.