2A Ultra-Small Controlled Load Switch with Auto-Discharge Path

NCP334, NCP335

The NCP334 and NCP335 are low Ron MOSFET controlled by external logic pin, allowing optimization of battery life, and portable device autonomy.

Indeed, due to a current consumption optimization with PMOS structure, leakage currents are eliminated by isolating connected IC's on the battery when not used.

Output discharge path is also embedded to eliminate residual voltages on the output rail in the NCP335.

Proposed in wide input voltage range from 1.2 V to 5.5 V, and a very small 0.96 x 0.96 mm WLCSP4, 0.5 mm pitch.

Features

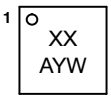
- 1.2 V – 5.5 V Operating Range
- 47 mΩ P MOSFET at 3.3 V
- DC Current Up to 2 A
- Output Auto−discharge (NCP335)
- Active high EN pin
- WLCSP4 0.96 x 0.96 mm
- ESD Ratings: 4 kV Human Body Model, 2 kV CDM,
- 250 V Machine Model
- These are Pb−Free Devices

Typical Applications

- Mobile Phones
- Tablets
- Digital Cameras
- GPS
- Portable Devices

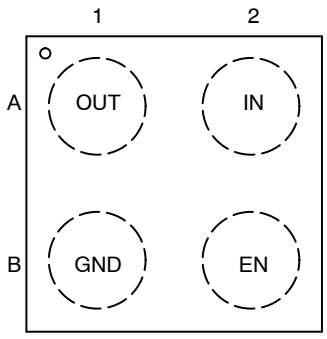
WLCSP4
CASE 567FG

MARKING DIAGRAM



XX	= Specific Device Code
A	= Assembly Location
Y	= Year
W	= Work Week

PIN DIAGRAM



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 9 of this data sheet.

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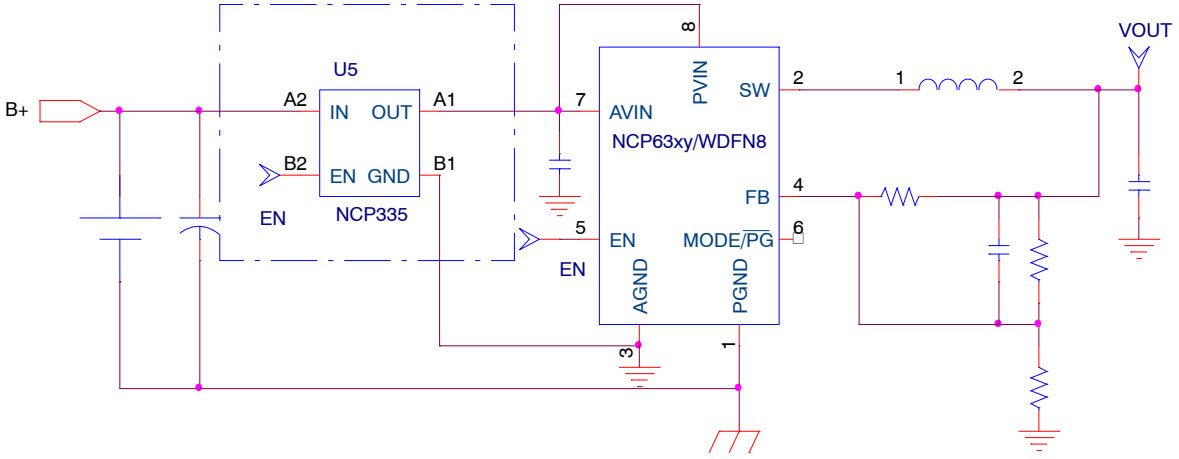


Figure 1. Typical Application Circuit

PIN FUNCTION DESCRIPTION

Pin Name	Pin Number	Type	Description
IN	A2	POWER	Load−switch input voltage; connect a 1 μF or greater ceramic capacitor from IN to GND as close as possible to the IC.
GND	B1	POWER	Ground connection.
EN	B2	INPUT	Enable input, logic high turns on power switch.
OUT	A1	OUTPUT	Load−switch output; connect a 1 μF ceramic capacitor from OUT to GND as close as possible to the IC is recommended.

BLOCK DIAGRAM

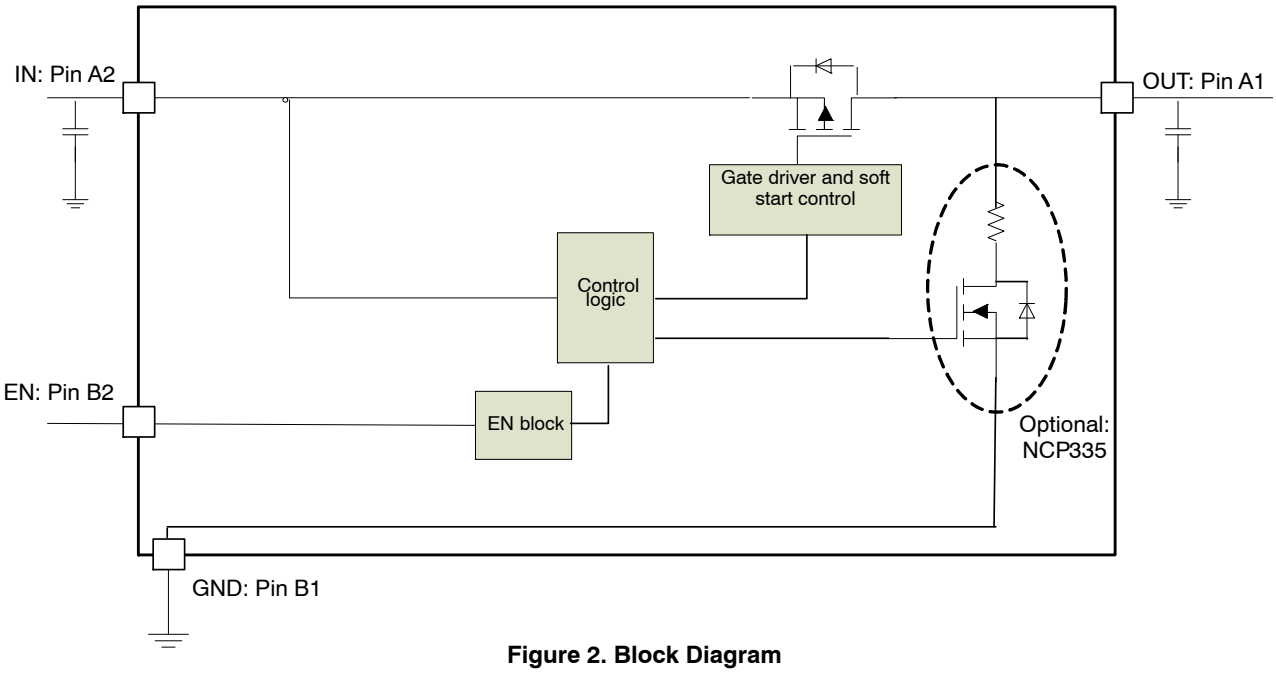


Figure 2. Block Diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IN, OUT, EN, Pins	V_{EN} , V_{IN}, V_{OUT}	0.3 to + 7.0	V
From IN to OUT Pins: Input/Output	V_{IN}, V_{OUT}	0 to + 7.0	V
Maximum Junction Temperature	T_J	−40 to + 125	°C
Storage Temperature Range	T_{STG}	−40 to + 150	°C
Human Body Model (HBM) ESD Rating are (Notes 1 and 2)	ESD HBM	4000	V
Machine Model (MM) ESD Rating are (Notes 1 and 2)	ESD MM	250	V
Charge Device Model (CDM) ESD Rating are (Notes 1 and 2)	ESD CDM	2000	V
Latch−up protection (Note 3) − Pins IN, OUT, EN	LU	100	mA
Moisture Sensitivity (Note 4)	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. According to JEDEC standard JESD22−A108.
2. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ±4.0 kV per JEDEC standard: JESD22−A114 for all pins.
   Machine Model (MM) ±250 V per JEDEC standard: JESD22−A115 for all pins.
   Charge Device Model (CDM) ±2.0 kV per JEDEC standard: JESD22−C101 for all pins.
3. Latch up Current Maximum Rating: ±100 mA per JEDEC standard: JESD78 class II.
4. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020.

OPERATING CONDITIONS

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IN}	Operational Power Supply			1.2		5.5	V
V_{EN}	Enable Voltage			0		5.5	
T_A	Ambient Temperature Range			−40	25	+ 85	°C
C_{IN}	Decoupling input capacitor			1			μF
C_{OUT}	Decoupling output capacitor			1			μF
$R_{\theta JA}$	Thermal Resistance Junction to Air	WLCSP package (Note 5)			100		°C/W
I_{OUT}	Maximum DC current					2	A
P_D	Power Dissipation Rating (Note 6)	$T_A \le 25$ °C	WLCSP package		0.5		W
		T_A = 85°C	WLCSP package		0.2		W

5. The $R_{\theta JA}$ is dependent of the PCB heat dissipation and thermal via.
6. The maximum power dissipation (P_D) is given by the following formula:

$$P_D = \frac{T_{JMAX} - T_A}{R_{\theta JA}}$$

ELECTRICAL CHARACTERISTICS Min and Max Limits apply for $_{TA}$ between −40°C to +85°C for $_{VIN}$ between 1.2 V to 5.5 V (Unless otherwise noted). Typical values are referenced to T_A = + 25 °C and V_{IN} = 4 V (Unless otherwise noted).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
POWER SWITCH							
$R_{DS(on)}$	Static drain−source on−state resistance	V_{IN} = 5.5 V	T_A = 25°C, I = 200 mA (Note 8)		38	40	mΩ
		V_{IN} = 4.2 V	T_A = 25°C, I = 200 mA		42	46	
		V_{IN} = 3.3 V	T_A = 25°C, I = 200 mA		47	52	
		V_{IN} = 1.8 V	T_A = 25°C, I = 200 mA		76	87	
			Full			100	
		V_{IN} = 1.2 V	T_A = 25°C, I = 200 mA		211	420	
R_{DIS}	Output discharge path	EN = low	V_{IN} = 3.3 V, NCP335 only		65	110	Ω
T_R	Output rise time	V_{IN} = 3.6 V	C_{LOAD} = 1 μF, R_{LOAD} = 25 Ω (Note 7)		71		μs
T_F	Output fall time	V_{IN} = 3.6 V	C_{LOAD} = 1 μF, R_{LOAD} = 25 Ω (Note 7)		42		μs
T_{on}	Gate turn on	V_{IN} = 3.6 V	Gate turn on + Output rise time		116		μs
T_{en}	Enable time	V_{IN} = 3.6 V	From EN low to high to V_{OUT} = 10% of fully on		45		μs
V_{IH}	High−level input voltage			0.9			V
V_{IL}	Low−level input voltage					0.5	V
R_{EN}	Pull down resistor				5		MΩ
QUIESCENT CURRENT							
I_Q	Current consumption	V_{IN} = 3.3 V, EN = low, No load				1	μA
		V_{IN} = 3.3 V, EN= high, No load				1	μA

7. Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground
8. Guaranteed by design and characterization, not production tested.

TIMINGS

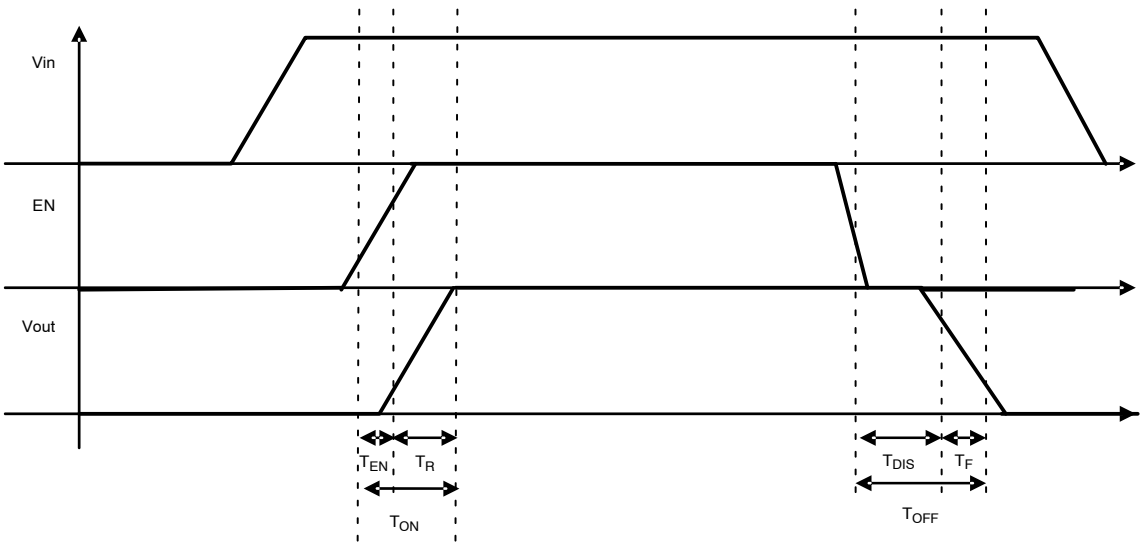


Figure 3. Enable, Rise and fall time

TYPICAL CHARACTERISTICS

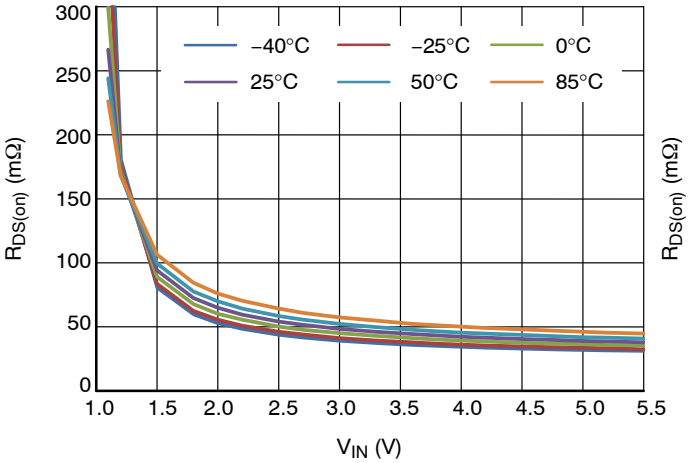


Figure 4. $R_{DS(on)}$ (mΩ) vs. Vin (V)

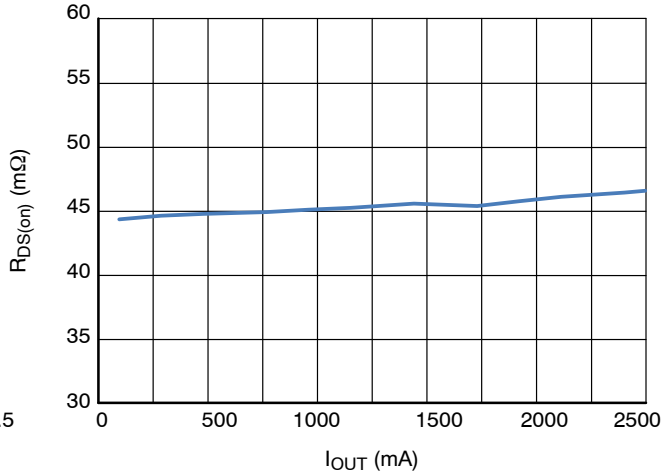


Figure 5. $R_{DS(on)}$ (mΩ) vs. Iload (mA) at 3.6 V

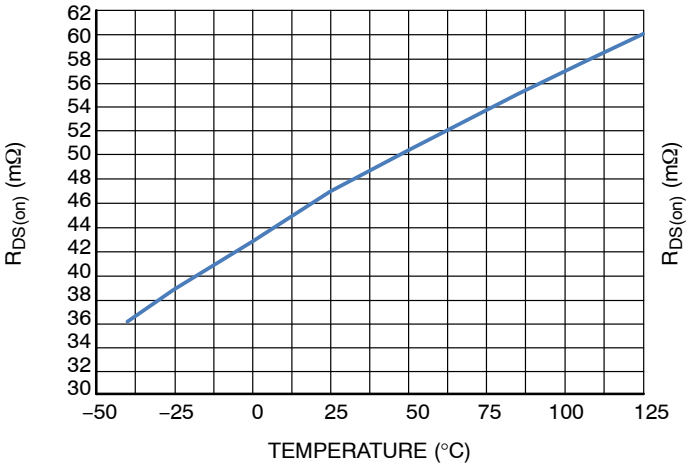


Figure 6. $R_{DS(on)}$ (mΩ) vs. Temperature (°C) at 3.3 V, Iload 100 mA

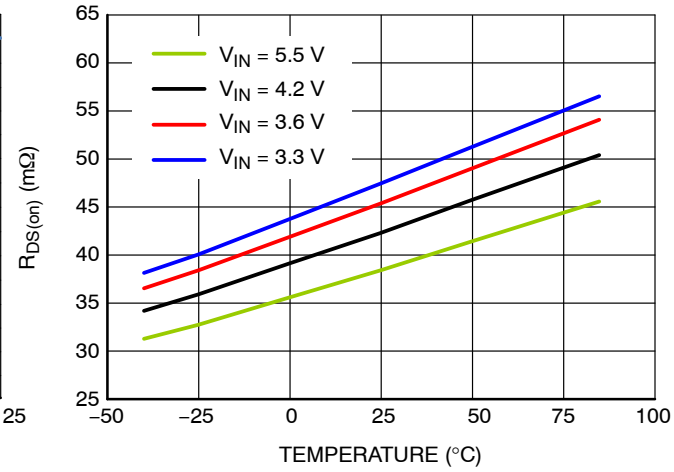


Figure 7. $RD_{S(on)}$ (mΩ) vs. Temperature (°C), Iload 2 A

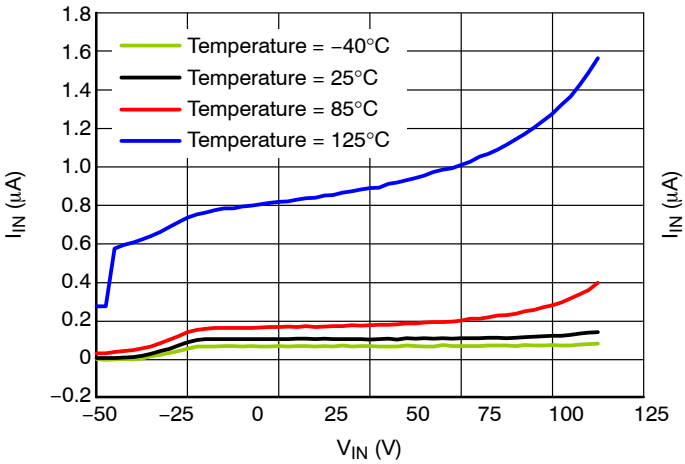


Figure 8. Standby Current (μA) versus V_{IN} (V), No Load

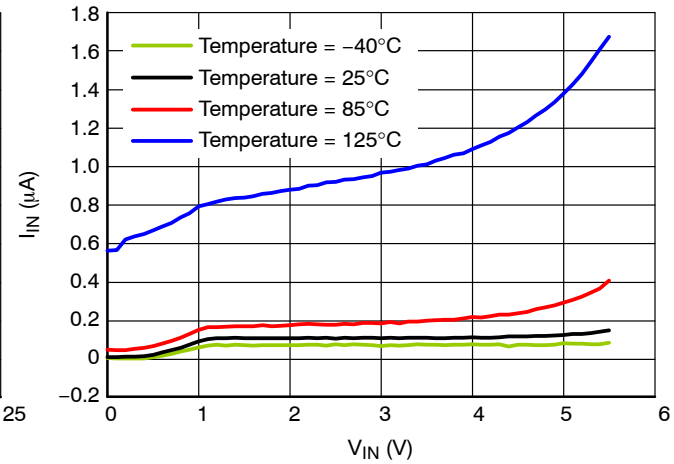


Figure 9. Standby Current (μA) versus V_{IN} (V), V_{out} Short to GND.

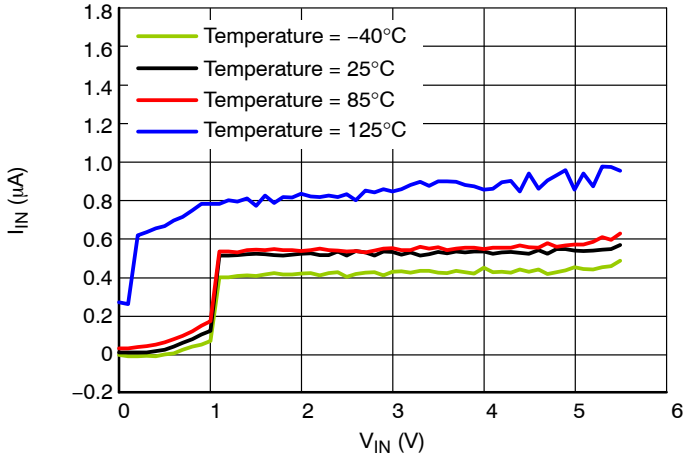


Figure 10. Quiescent Current (μA) versus V_{IN} (V), No load.

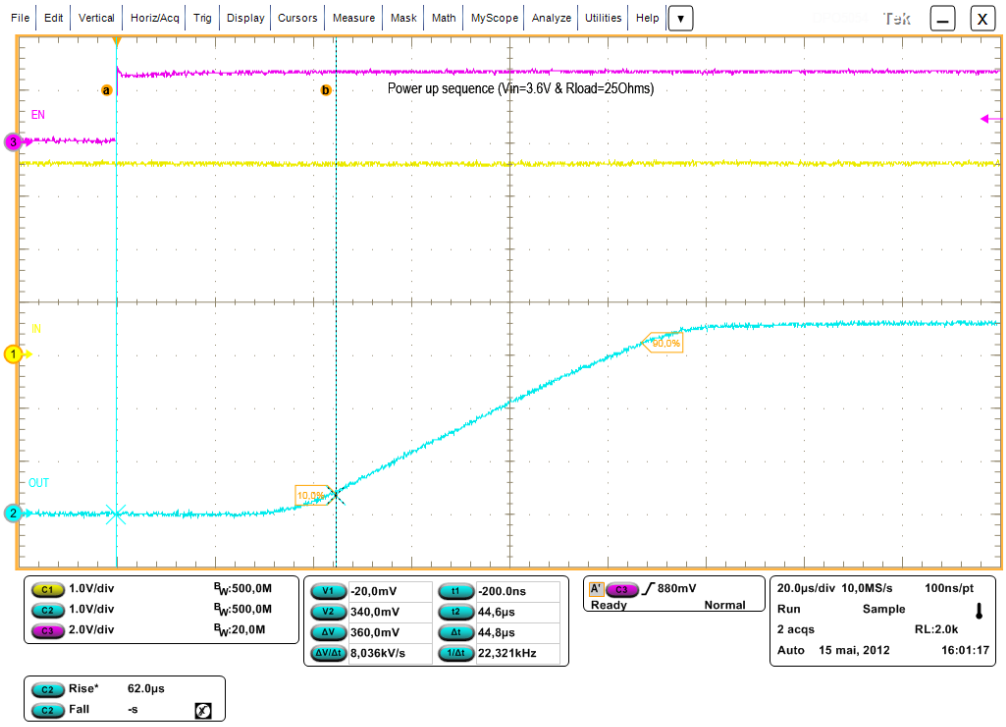


Figure 11. Enable Time, Rise Time, and Ton Time

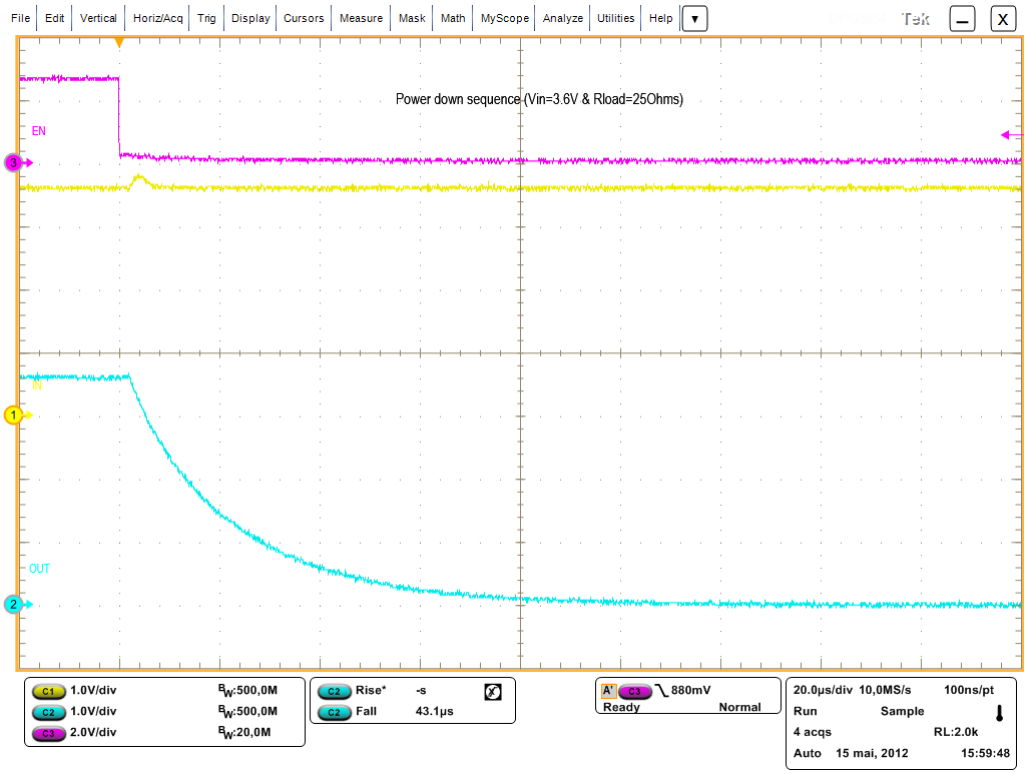


Figure 12. Disable Time, Fall Time and Toff Time

FUNCTIONAL DESCRIPTION

Overview

The NCP334 – NCP335 are high side P channel MOSFET power distribution switch designed to isolate ICs connected on the battery in order to save energy. The part can be turned on, with a range of battery from 1.2 V to 5.5 V.

Enable Input

Enable pin is an active high. The path is opened when EN pin is tied low (disable), forcing P MOS switch off.

The IN/OUT path is activated with a minimum of Vin of 1.2V and EN forced to high level.

Auto Discharge (NCP335 Only)

NMOS FET is placed between the output pin and GND, in order to discharge the application capacitor connected on OUT pin.

The auto−discharge is activated when EN pin is set to low level (disable state).

The discharge path (Pull down NMOS) stays activated as long as EN pin is set at low level and V_{IN} > 1.2 V.

In order to limit the current across the internal discharge N−MOSFET, the typical value is set at 65 Ω.

Cin and Cout Capacitors

IN and OUT, 1 µF, at least, capacitors must be placed as close as possible the part for stability improvement.

APPLICATION INFORMATION

Power Dissipation

Main contributor in term of junction temperature is the power dissipation of the power MOSFET. Assuming this, the power dissipation and the junction temperature in normal mode can be calculated with the following equations:

$P_D = R_{DS(on)} \times (I_{OUT})^2$

P_D = Power dissipation (W)

$R_{DS(on)}$ = Power MOSFET on resistance (Ω)

I_{OUT} = Output current (A)

$T_J = P_D \times R_{\theta JA} + T_A$

T_J = Junction temperature (°C

$R_{\theta JA}$ = Package thermal resistance (°C/W)

T_A = Ambient temperature (°C)

PCB Recommendations

The NCP334 – NCP335 integrate an up to 2 A rated PMOS FET, and the PCB design rules must be respected to properly evacuate the heat out of the silicon. By increasing PCB area, especially around IN and OUT pins, the $R_{\theta JA}$ of the package can be decreased, allowing higher power dissipation.

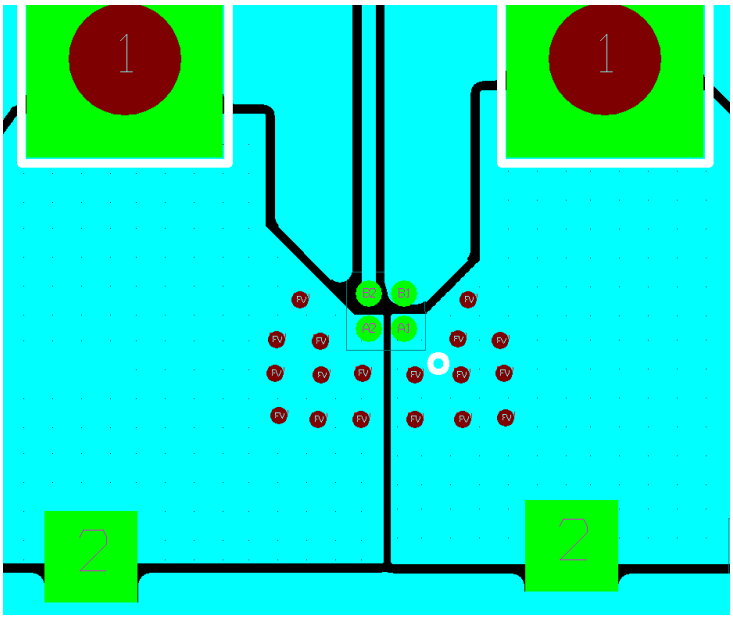


Figure 13. Routing Example 1 oz, 2 Layers, 100°C/W

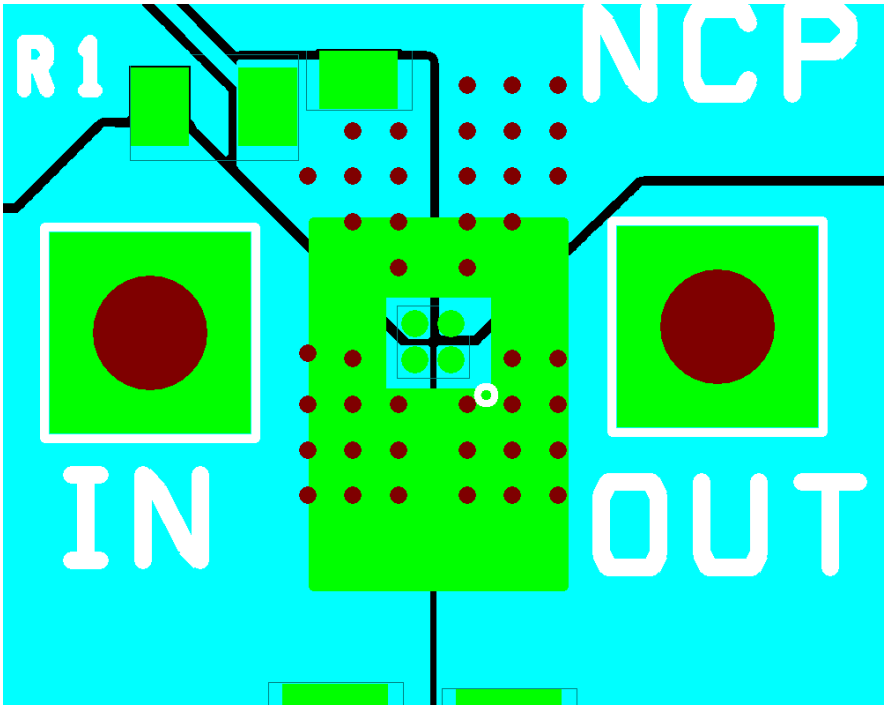


Figure 14. Routing Example 2 oz, 4 Layers, 60°C/W

Example of application definition.

$$T_J - T_A = R_{\theta JA} \times Pd = R_{\theta JA} \times R_{DS(on)} \times I^2$$

T_J: Junction Temperature.
T_A: Ambient Temperature.
R_θ = Thermal resistance between IC and air, through PCB.
$R_{DS(on)}$: Intrinsic resistance of the IC MOSFET.
I: load DC current.
Taking into account of Rtheta obtain with:
1 oz, 2 layers: 100°C/W.

At 2 A, 25°C ambient temperature, $R_{DS(on)}$ 42 mΩ @ V_{IN} 4.2 V, the junction temperature will be:

$$T_J = T_A + R_\theta \times Pd = 25 + \left(0.042 \times 2^2\right) \times 100 = 41.8°C/W$$

Taking into account of R_θ obtain with:
2 oz, 4 layers: 60°C/W.
At 2 A, 25°C ambient temperature, $R_{DS(on)}$ 42 mΩ @ V_{IN} 4.2 V, the junction temperature will be:

$$T_J = T_A + R_\theta \times Pd = 25 + \left(0.042 \times 2^2\right) \times 60 = 35°C.$$

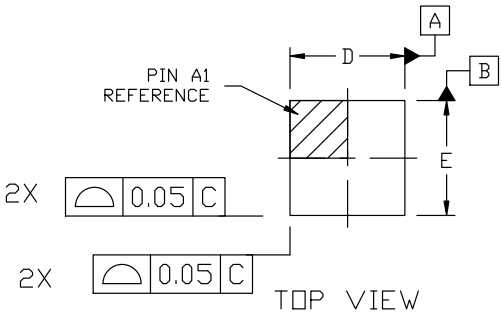
ORDERING INFORMATION

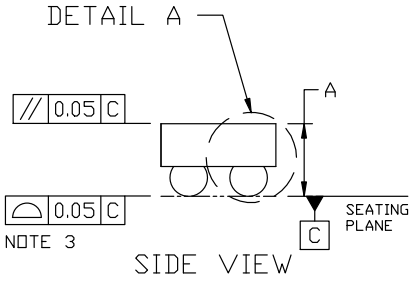
Device	Marking	Package	Shipping†
NCP334FCT2G	AD	WLCSP 0.96 x 0.96 mm (Pb−Free)	3000 / Tape & Reel
NCP335FCT2G	AA	WLCSP 0.96 x 0.96 mm (Pb−Free)	3000 / Tape & Reel

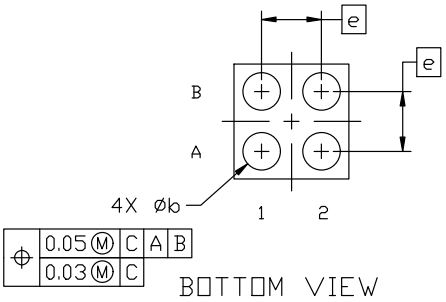
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

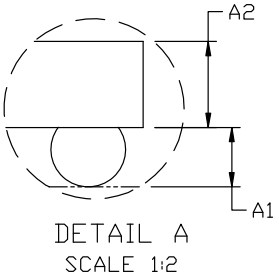
WLCSP4 0.96x0.96x0.609
CASE 567FG
ISSUE A

DATE 01 JUL 2022





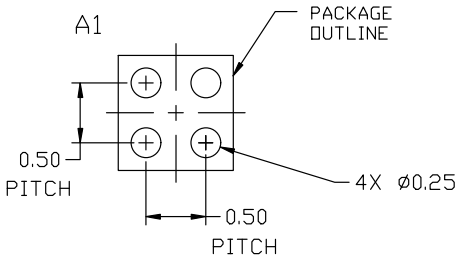




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.

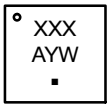
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.554	0.609	0.664
A1	0.219	0.249	0.279
A2	0.335	0.360	0.385
b	0.282	0.312	0.342
D	0.96 BSC		
E	0.96 BSC		
e	0.50 BSC		



RECOMMENDED
MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**WLCSP4 0.96x0.96x0.609**	**PAGE 1 OF 1**

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