Totem Pole Power Factor Correction Controller NCP1681

The NCP1681 is an innovative Multi−Mode (MM) and Continuous Conduction Mode (CCM) Power Factor Correction (PFC) controller IC designed to drive the bridgeless totem pole PFC topology. The bridgeless totem pole PFC consists of two totem pole legs: a fast−switching leg driven at the PWM switching frequency and a second leg that operates at the AC line frequency. This topology eliminates the diode bridge present at the input of a conventional PFC circuit, allowing significant improvement in efficiency and power density. The NCP1681 is available as a Fixed Frequency (NCP1681Ax) or Multi−Mode (NCP1681Bx) device.

General Features

- Totem Pole PFC Topology Eliminates Input Diode Bridge Enabling Very High Efficiency & Compact Design
- AC Line Monitoring Circuit & AC Phase Detection
- Brownout Detection
- Digital Loop Compensation
- Novel Current Sensing Scheme Providing Inductor Current Upslope and Downslope Sensing
- PFCOK Indicator
- Skip/Standby Mode for Optimizing Light Load Performance
- Near−Unity Power Factor in All Operating Modes

Multi−Mode Operation

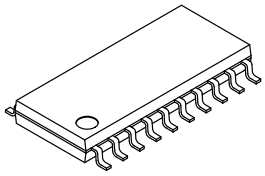
- Continuous Conduction Mode (CCM) in Heavy−Load Conditions
- Critical Conduction Mode (CrM) in Light & Medium Load Conditions
- Optional Fixed Frequency CCM Across Load Range
- Simplified Valley Sensing

Safety Features

- Soft and Fast Overvoltage Protection
- 2−level Latch Input for OVP & OTP
- Bulk Undervoltage Protection
- Internal Thermal Shutdown
- Cycle−by−cycle Current Limit

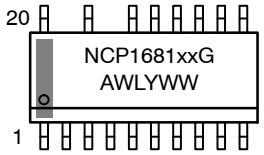
Applications

- Cloud/Server Power Supplies
- High Performance Computing
- 5G/Telecom Power Supplies
- Industrial Power Supplies
- Ultra−High Density (UHD) Power Supplies
- Merchant Power



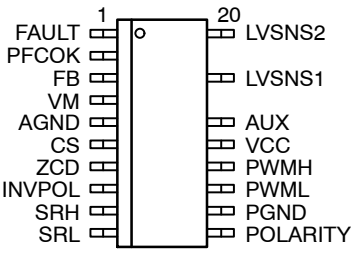
SOIC−20
NARROW BODY
CASE 751EZ

MARKING DIAGRAM



xx	= AA, AB or BA
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

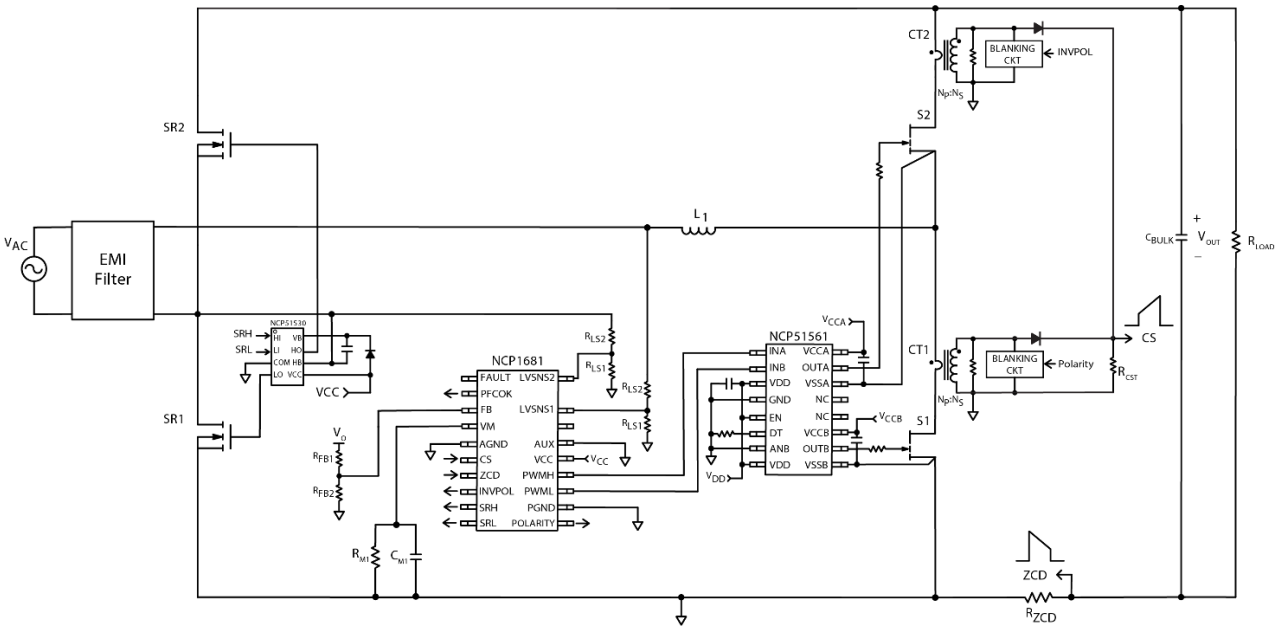


Figure 1. Typical CCM Application Schematic

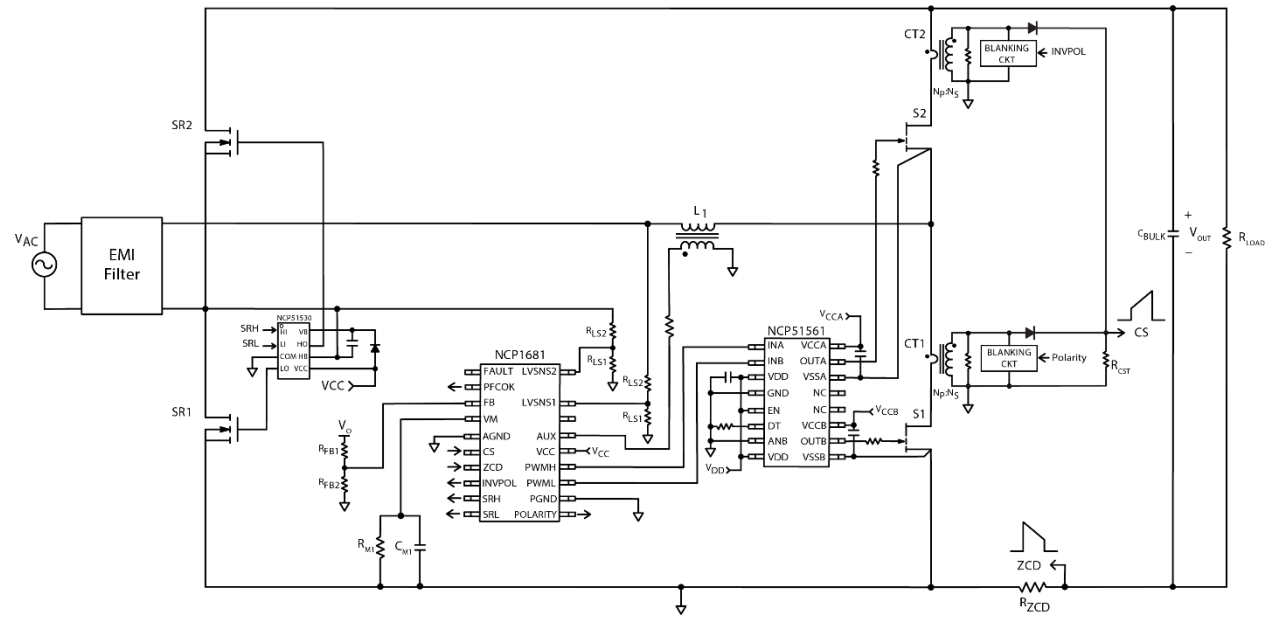


Figure 2. Typical Multi−Mode Application Schematic

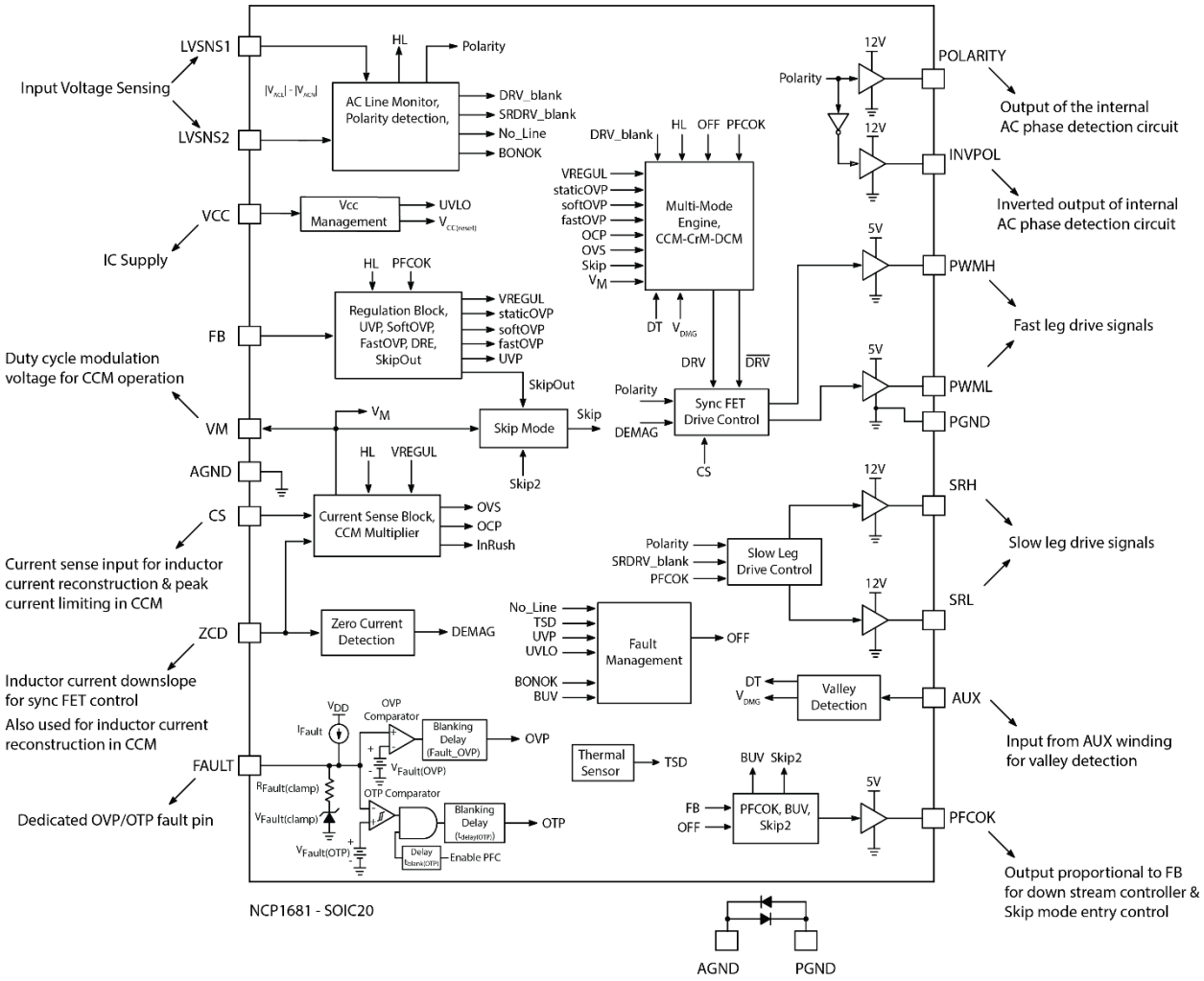


Figure 3. Block Diagram

Table 1. PIN DESCRIPTIONS

Pin Number	Pin Name	Pin Description
1	FAULT	Combined OVP/OTP fault pin.
2	PFCOK	The PFCOK pin is held low when the PFC output voltage is out of regulation and during fault conditions. The pin becomes active when the PFC output achieves regulation in nominal operation, sourcing a current proportional to the feedback voltage, V_{FB}. The PFCOK pin is bidirectional; it can be used to enable a downstream converter and can be used by the downstream converter to force the NCP1681 into Skip/Standby Mode operation.
3	FB	This pin senses the PFC output voltage for loop regulation.
4	V_M	Multiplier output. This pin provides the voltage for duty cycle modulation.
5	AGND	Signal ground reference.
6	CS	This pin senses the inductor current upslope through current sense transformers. Upslope signal is used for cycle−by−cycle current limiting and is summed with the ZCD signal to reconstruct an image of the inductor current in the IC. The reconstructed inductor current signal is used for generation of the multiplier voltage for duty cycle modulation in CCM.
7	ZCD	The pin senses the inductor current downslope. It is used to detect demagnetization and control the synchronous (1−D) switch. The pin voltage is summed with the CS pin voltage to reconstruct an image of the inductor current. The reconstructed inductor current signal is used for generation of the multiplier voltage for duty cycle modulation in CCM.
8	INVPOL	Inverted output of the internal AC polarity detection circuit.
9	SRH	Control signal for high side slow leg device.
10	SRL	Control signal for low side slow leg device.
11	POLARITY	Output of the internal AC polarity detection circuit.
12	PGND	Power ground reference.
13	PWML	PWM logic level output for control of low side fast leg switch.
14	PWMH	PWM logic level output for control of high side fast leg switch.
15	VCC	IC supply pin.
16	AUX	The pin is used to monitor the switch node resonance on the auxiliary winding and enable valley turn−on during CrM/DCM operation. For CCM operation (NCP1681Ax devices), the AUX pin must be tied to GND.
17		Removed for creepage distance.
18	LVSNS1	Low voltage input for AC line voltage monitoring. LVSNS1 resistor divider should be connected to AC line side of the boost inductor.
19		Removed for creepage distance.
20	LVSNS2	Low voltage input for AC line voltage monitoring. LVSNS2 resistor divider should be connected to the slow leg bridge node.

Table 2. ORDERING INFORMATION TABLE

OPN	Operating Mode	F_{CCM} (kHz)	V_{ILIM} (V) LL / HL	$V_{ZCD(ARM)}$ (mV)	Package	Shipping†
NCP1681AAD2R2G	CCM	65	1 / 1	150	SOIC−20 (Pb−Free)	2500 / Tape & Reel
NCP1681ABD2R2G	CCM	95	1 / 1	150		
NCP1681BAD2R2G	Multi−Mode	65	1.4 / 0.84	300		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Table 3. MAXIMUM RATINGS (All voltages measured with respect to AGND)

Rating	Pin	Symbol	Value	Unit
Supply Input Voltage, V_{CC} pin	VCC	$V_{CC(MAX)}$	−0.3 to 30	V
Maximum Current for V_{CC} pin	VCC	$I_{CC(MAX)}$	Internally limited	mA
PGND Maximum Voltage	PGND	$V_{PGND(MAX)}$	−0.3 to + 0.3	V
PWML pin Maximum Voltage	PWML	$V_{PWML(MAX)}$	−0.3 to 5.5	V
PWML pin Maximum Current	PWML	$I_{PWML(SRC\_MAX)}$ $I_{PWML(SNK\_MAX)}$	−100 +160	mA
PWMH pin Maximum Voltage	PWMH	$V_{PWMH(MAX)}$	−0.3 to 5.5	V
PWMH pin Maximum Current	PWMH	$I_{PWMH(SRC\_MAX)}$ $I_{PWMH(SNK\_MAX)}$	−100 +160	mA
SRx, Polarity, INVPOL pin Maximum Voltage	SRL, SRH, Polarity, INVPOL	$V_{SRx(MAX)}$	−0.3 to 14	V
SRx, Polarity, INVPOL pin Maximum Current	SRL, SRH, Polarity, INVPOL	$I_{SRx(SRC\_MAX)}$ $I_{SRx(SNK\_MAX)}$	−100 +160	mA
AUX pin Input Voltage	AUX	V_{AUX}	−0.3 to 5.5 (Note 1)	V
AUX pin Input Current	AUX	I_{AUX}	−2 / +5	mA
ZCD pin Input Voltage Range	ZCD	V_{ZCD}	−0.3 to 5.5 (Note 1)	V
ZCD pin Maximum Current	ZCD	$I_{ZCD(MAX)}$	−2 / +5	mA
Maximum Input Voltage Other Pins	LVSNS1, LVSNS2, CS, VM, FB, FAULT	V_{MAX}	−0.3 to 5.5 (Note 1)	V
Maximum Current Other Pins	LVSNS1, LVSNS2, CS, VM, FB, FAULT	I_{MAX}	−2 to +5	mA
Power Dissipation and Thermal Characteristics Maximum Power Dissipation at T_A = 70°C Thermal Resistance Junction−to−Air (1 Oz Cu, 0.155 Sq Inch Printed Circuit Copper Clad)		 P_D $R_{\theta JA}$	 660 121	 mW °C/W
Maximum Junction Temperature		$T_{J(MAX)}$	150	°C
Operating Temperature Range			−40 to +125	°C
Storage Temperature Range			−60 to +150	°C
ESD Capability, HBM model (Note 2)			3.5	kV
ESD Capability, CDM model (Note 2)			1.25	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This level is low enough to guarantee not to exceed the internal ESD diode and 5.5−V ZENER diode. More positive and negative voltages can be applied if the pin current stays within the −2 mA / +5 mA range.
2. This device contains ESD protection and exceeds the following tests: Human Body Model 3500 V per JEDEC Standard JESD22−A114E, Charged Device Model 1250 V per JEDEC Standard JESD22−C101E.
3. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.

Table 4. ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, V_{LVSNS1}= 1.2 V, V_{LVSNS2} = 0 V, V_{FB} = 2.4 V, V_{FAULT} = open, $C_{POLARITY}$ = 100 pF, V_{AUX} = 0 V, V_{ZCD} = 0 V, V_{CS} = 0 V, C_{VCC} = 100 nF, C_{SRL} = C_{SRH} = 100 pF, C_{PWML} = C_{PWMH} = 100 pF, for typical values T_J = 25°C, for min/max values, T_J is – 40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
START–UP & SUPPLY CIRCUITS						
Supply Voltage						V
Startup Threshold	V_{CC} increasing	$V_{CC(on)}$	9.75	10.5	11.25	
Minimum Operating Voltage	V_{CC} decreasing	$V_{CC(off)}$	8.2	8.8	9.4	
V_{CC} Hysteresis ($V_{CC(on)}$ – $V_{CC(off)}$)	V_{CC} decreasing	$V_{CC(HYS)}$	1.2	1.7	–	
Internal Latch / Logic Reset Level	V_{CC} decreasing	$V_{CC(reset)}$	2.5	4	6	
Supply Current						mA
Before Startup	V_{CC} = 9.5 V	I_{CC1}	–	1.8	2.2	
Fault or Latch	V_{FLT} = 0 V	I_{CC2}	–	1.8	2.2	
Operational, Switching at 100 kHz	All DRVs Open	I_{CC3}	–	3.3	4	
Operational, Skipping	V_{PFCOK} = 0 V	I_{CC4}	–	0.54	0.9	
AC ZERO CROSSING MANAGEMENT						
Recommended External Divider Ratio		K_{L_DIV}	–	100	–	
Main PWM Drive Control						
PWM Zero Crossing Blanking Thresholds						mV
Threshold to stop PWML/H pulses	V_{ZCB_STOP} = $\lvert V_{LVSNS1} - V_{LVSNS2}\rvert$ V_{LVSNS1} Decreasing, V_{LVSNS2} = 0 V; V_{LVSNS1} Increasing, V_{LVSNS2} = 4 V;	$V_{ZCB\_STOP1(LL)}$ $V_{ZCB\_STOP2(LL)}$	–	100	–	
Threshold to start PWML/H pulses	V_{ZCB_START} = $\lvert V_{LVSNS1} - V_{LVSNS2}\rvert$ V_{LVSNS1} Increasing, V_{LVSNS2} = 0 V; V_{LVSNS1} Decreasing, V_{LVSNS2} = 4 V	$V_{ZCB\_START1(LL)}$ $V_{ZCB\_START2(LL)}$		$V_{ZCB\_STOPx(LL)}$ + 20		
Zero Crossing Blanking Filter		$t_{FILT(ZCB)}$	–	20	25	μs
Polarity Detection Control						
Polarity Detection Filter		t_{POL_FILTER}	–	200	–	μs
Polarity Detection Threshold	V_{POL_DETx} = V_{LVSNS1} – V_{LVSNS2} V_{LVSNS1} Decreasing, V_{LVSNS2} = 0 V; V_{LVSNS1} Increasing, V_{LVSNS2} = 4 V;	V_{POL_DET1} V_{POL_DET2}	–55 –20	–15 15	20 55	mV
Slow Leg (SR) Drive Control						
Slow Leg Zero Crossing Blanking Thresholds						mV
Threshold to stop SRx pulses	V_{SR_STOP} = $\lvert V_{LVSNS1} - V_{LVSNS2}\rvert$ V_{LVSNS1} Decreasing, V_{LVSNS2} = 0 V; V_{LVSNS1} Increasing, V_{LVSNS2} = 4 V;	$V_{SR\_STOP1(LL)}$ $V_{SR\_STOP2(LL)}$	–	180	–	
Threshold to start SRx pulses	V_{SR_START} = $\lvert V_{LVSNS1} - V_{LVSNS2}\rvert$ V_{LVSNS1} Increasing, V_{LVSNS2} = 0 V; V_{LVSNS1} Decreasing, V_{LVSNS2} = 4 V	$V_{SR\_START1(LL)}$ $V_{SR\_START2(LL)}$		$V_{SR\_STOPx(LL)}$ + 20		
Synchronous (1 – d) Drive Control						
Sync Zero Crossing Blanking Thresholds						mV
Threshold to stop Sync pulses	V_{SYNC_STOP} = $\lvert V_{LVSNS1} - V_{LVSNS2}\rvert$ V_{LVSNS1} Decreasing, V_{LVSNS2} = 0 V; V_{LVSNS1} Increasing, V_{LVSNS2} = 4 V;	$V_{SYNC\_STOP1(LL)}$ $V_{SYNC\_STOP2(LL)}$	–	200	–	
Threshold to start Sync pulses	V_{SYNC_START} = $\lvert V_{LVSNS1} - V_{LVSNS2}\rvert$ V_{LVSNS1} Increasing, V_{LVSNS2} = 0 V; V_{LVSNS1} Decreasing, V_{LVSNS2} = 4 V	$V_{SYNC\_START1(LL)}$ $V_{SYNC\_START2(LL)}$		$V_{SYNC\_STOPx(LL)}$ + 20		
BROWN–OUT, LINE SAG AND LINE RANGE DETECTION						
Line Sag and Brown–Out Detection Upper Threshold	$\lvert V_{LVSNS1} - V_{LVSNS2}\rvert$ Increasing	$V_{BO(START)}$	1.02	1.10	1.18	V
Line Sag and Brown–Out Detection Lower Threshold	$\lvert V_{LVSNS1} - V_{LVSNS2}\rvert$ Decreasing	$V_{BO(STOP)}$	0.92	1.00	1.08	V
Brown–Out Detection Hysteresis	$\lvert V_{LVSNS1} - V_{LVSNS2}\rvert$ Increasing	$V_{BO(HYS)}$	60	100	–	mV

Table 4. ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, V_{LVSNS1}= 1.2 V, V_{LVSNS2} = 0 V, V_{FB} = 2.4 V, V_{FAULT} = open, $C_{POLARITY}$ = 100 pF, V_{AUX} = 0 V, V_{ZCD} = 0 V, V_{CS} = 0 V, C_{VCC} = 100 nF, C_{SRL} = C_{SRH} = 100 pF, C_{PWML} = C_{PWMH} = 100 pF, for typical values T_J = 25°C, for min/max values, T_J is – 40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
BROWN–OUT, LINE SAG AND LINE RANGE DETECTION						
Line Sag Detection Blanking Timer	$\|V_{LVSNS1} - V_{LVSNS2}\| < V_{BO(STOP)}$; Delay to Soft Stop Enable	$t_{SAG(blank)}$	20	25	30	ms
Brown–Out Detection Blanking Timer	$\|V_{LVSNS1} - V_{LVSNS2}\| < V_{BO(STOP)}$; Delay to Polarity Disable	$t_{BO(blank)}$	520	650	780	ms
High–Line Level Detection Threshold	$\|V_{LVSNS1} - V_{LVSNS2}\|$ Increasing	V_{HL}	2.20	2.36	2.52	V
Low–Line Level Detection Threshold	$\|V_{LVSNS1} - V_{LVSNS2}\|$ Decreasing	V_{LL}	2.07	2.22	2.37	V
Line Range Select Hysteresis	$\|V_{LVSNS1} - V_{LVSNS2}\|$ Increasing	$V_{LR(HYS)}$	100	140	–	mV
High to Low Line Mode Selector Timer	$\|V_{LVSNS1} - V_{LVSNS2}\| < V_{LL}$	$t_{blank(LL)}$	20	25	30	ms
Low to High Line Mode Selector Timer Filter	$\|V_{LVSNS1} - V_{LVSNS2}\| > V_{HL}$	$t_{filter(HV)}$	200	300	400	μs
Lockout Timer for Low to High Line Mode Transition	Low Line Mode; $\|V_{LVSNS1} - V_{LVSNS2}\| > V_{HL}$	$t_{line(lockout)}$	400	500	600	ms
AC LINE FREQUENCY MONITORING						
Line Frequency Upper Threshold		$t_{LINE(65)}$	66	72	78	Hz
Line Frequency Lower Threshold		$t_{LINE(45)}$	37	41	45	Hz
Device Enable Counter		N_{DRV_EN}	–	4	–	
Slow Leg Disable Counter		N_{SR_DIS}	–	1	–	
Line Frequency2 Timer	Delay to PWM Disable	$t_{LINEFREQ(DLY)}$	60	100	165	ms
VALLEY DETECTION CIRCUIT (NCP1681Bx Only)						
Valley Detection Thresholds in Positive Half Line Cycle	V_{LVSNS1} = 1.2 V, V_{LVSNS2} = 0 V; V_{AUX} rising (Arm) V_{AUX} falling (Trigger)	$V_{VD1\_TH(rising)}$ $V_{VD1\_TH(falling)}$	150 50	200 100	250 150	mV
Valley Detection Hysteresis in Positive Half Line Cycle		$V_{VD1(HYS)}$	50	100	–	mV
Propagation Delay of Valley Detection in Positive Half Line Cycle	Step V_{AUX} 1.5 V to –0.2 V; Time to PWML = 2.5 V	T_{VD1}	–	50	80	ns
Valley Detection Thresholds in Negative Half Line Cycle	V_{LVSNS1} = 0 V, V_{LVSNS2} = 1.2 V; V_{AUX} falling (Arm) V_{AUX} rising (Trigger)	$V_{VD2\_TH(falling)}$ $V_{VD2\_TH(rising)}$	50 150	100 200	150 250	mV
Valley Detection Hysteresis in Negative Half Line Cycle		$V_{VD2(HYS)}$	50	100	–	mV
Propagation Delay of Valley Detection in Negative Half Line Cycle	Step V_{AUX} 0 V to 1.5 V; Time to PWMH = 2.5 V	T_{VD2}	–	45	75	ns
Minimum AUX pulse width		T_{SYNC}	–	95	155	ns
AUX pin bias current, V_{AUX} = $V_{VD1\_TH(rising)}$		$I_{AUX(bias1)}$	0.5	1	2	μA
AUX pin bias current, V_{AUX} = $V_{VD1\_TH(falling)}$		$I_{AUX(bias2)}$	0.5	1	2	μA
FAST LEG DRIVE SIGNALS (PWML & PWMH)						
PWMx Rise Time, x = L, H	V_{PWMx} = 10% to 90% of 5 V C_{PWMx} = 1 nF	$T_{PWMx(rise)}$	–	95	–	ns
PWMx Fall Time	V_{PWMx} = 90% to 10% of 5 V C_{PWMx} = 1 nF	$T_{PWMx(fall)}$	–	30	–	ns
Source Resistance		ROH	–	15	25	Ω

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Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
FAST LEG DRIVE SIGNALS (PWML & PWMH)						
Sink Resistance		ROL	–	5	10	Ω
Peak Source Current (guaranteed by design)	V_{PWMx} = 0 V	$I_{PWMx(SRC)}$	–	100	–	mA
Peak Sink Current (guaranteed by design)	V_{PWMx} = 5 V	$I_{PWMx(SNK)}$	–	160	–	mA
PWMx Clamp Voltage	R_{PWMx} = 10 kΩ	$V_{PWMx(high)}$	4.5	5	5.5	V
Non−overlap time between falling edge of PWM(d) & rising edge of PWM(1−d)	V_{ZCD} = 0.5 V	T_{DT1}	90	130	170	ns
Non−overlap time between falling edge of PWM(1−d) rising edge of PWM(d)	V_{ZCD} = 0.5 V	T_{DT2}	110	150	190	ns
SLOW LEG DRIVE SIGNALS (SRL & SRH)						
SRx Rise Time x = LO, HI	V_{PWMSRx} = 10% to 90% of 12 V C_{PWMSRx} = 1 nF	$T_{PWMSRx(rise)}$	–	185	–	ns
SRx Fall Time	V_{PWMSRx} = 90% to 10% of 12 V C_{PWMSRx} = 1 nF	$T_{PWMSRx(fall)}$	–	125	–	ns
Source Resistance		ROH2	–	45	85	Ω
Sink Resistance		ROL2	–	30	60	Ω
SRx Peak Source Current (guaranteed by design)	V_{PWMSRx} = 0 V	$I_{PWMSRx(SRC)}$	–	100	–	mA
SRx Peak Sink Current (guaranteed by design)	V_{PWMSRx} = 12 V	$I_{PWMSRx(SNK)}$	–	160	–	mA
SRx Clamp Voltage	R_{PWMSRx} = 10 kΩ V_{CC} = 30 V	$V_{PWMSRx(high)}$	10	12	14	V
SRx Minimum Drive Voltage	R_{PWMSRx} = 10 kΩ V_{CC} = $V_{CC(off)}$ + 100 mV	$V_{PWMSRx(MIN)}$	7.8	9	–	V
POLARITY & INVPOL OUTPUT						
POLARITY Rise Time	$V_{POLARITY}$ = 10% to 90% of 12 V $C_{POLARITY}$ = 1 nF	$T_{POLARITY(rise)}$	–	185	–	ns
POLARITY Fall Time	$V_{POLARITY}$ = 10% to 90% of 12 V $C_{POLARITY}$ = 1 nF	$T_{POLARITY(fall)}$	–	125	–	ns
Source Resistance		ROH3	–	45	85	Ω
Sink Resistance		ROL3	–	30	60	Ω
POLARITY Peak Source Current (guaranteed by design)	$V_{POLARITY}$ = 0 V	$I_{POLARITY(SRC)}$	–	100	–	mA
POLARITY Peak Sink Current (guaranteed by design)	$V_{POLARITY}$ = 12 V	$I_{POLARITY(SNK)}$	–	160	–	mA
POLARITY Clamp Voltage	$R_{POLARITY}$ = 10 kΩ V_{CC} = 30 V	$V_{POLARITY(high)}$	10	12	14	V
POLARITY Minimum Drive Voltage	$R_{POLARITY}$ = 10 kΩ V_{CC} = $V_{CC(off)}$ + 100 mV	$V_{POLARITY(MIN)}$	7.8	9	–	V
INVPOL Rise Time	V_{INVPOL} = 10% to 90% of 12 V C_{INVPOL} = 1 nF	$T_{INVPOL(rise)}$	–	185	–	ns
INVPOL Fall Time	V_{INVPOL} = 90% to 10% of 12 V C_{INVPOL} = 1 nF	$T_{INVPOL(fall)}$	–	125	–	ns
Source Resistance		ROH4	–	45	85	Ω

Table 4. ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, V_{LVSNS1}= 1.2 V, V_{LVSNS2} = 0 V, V_{FB} = 2.4 V, V_{FAULT} = open, $C_{POLARITY}$ = 100 pF, V_{AUX} = 0 V, V_{ZCD} = 0 V, V_{CS} = 0 V, C_{VCC} = 100 nF, C_{SRL} = C_{SRH} = 100 pF, C_{PWML} = C_{PWMH} = 100 pF, for typical values T_J = 25°C, for min/max values, T_J is – 40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
POLARITY & INVPOL OUTPUT						
Sink Resistance		ROL4	–	30	60	Ω
INVPOL Peak Source Current (guaranteed by design)	V_{INVPOL} = 0 V	$I_{PINVPOL\ (SRC)}$	–	100	–	mA
INVPOL Peak Sink Current (guaranteed by design)	V_{INVPOL} = 12 V	$I_{INVPOL\ (SNK)}$	–	160	–	mA
INVPOL Clamp Voltage	R_{INVPOL} = 10 kΩ V_{CC} = 30 V	$V_{INVPOL\ (high)}$	10	12	14	V
INVPOL Minimum Drive Voltage	R_{INVPOL} = 10 kΩ V_{CC} = $V_{CC(off)}$ + 100 mV	$V_{INVPOL\ (MIN)}$	7.8	9	–	V
PWM CONTROL CIRCUIT						
CCM Switching Frequency NCP1681AA, BA NCP1681AB		F_{CCM}	 60.4 88.3	 65 95	 69.6 101.7	kHz
Switching Frequency Jitter Range		R_{JIT}	–	8.9	–	%
Switching Frequency Jitter Modulation Rate		F_{JIT}	–	2.4	–	kHz
Maximum duty cycle in CCM Operation NCP1681AA, BA NCP1681AB	V_M = 0 V	D_{MAX}	 92.7 92.2	 95.1 94.7	 97.5 97.2	%
PWM Ramp Peak Voltage		$V_{RAMP,PK}$	3.5	3.75	4	V
Maximum On Time in CrM NCP1681BA	V_{FB} < V_{REF}; V_{LVSN1} = 1.20V, V_{LSNS2} = 0V	$T_{on,\ max,CrM}$	13.8	17.1	20.3	μs
Maximum Frequency Clamp NCP1681BA Only		F_{clamp1}	–	130	–	kHz
On–Time Below Which Frequency Foldback is Engaged, NCP1681BA Only	Low line High Line	$(t_{ON,FF})_{LL}$ $(t_{ON,FF})_{HL}$	– –	3.84 1.92	– –	μs
Minimum Frequency Clamp		F_{MIN}	25	30.5	36	kHz
Minimum On–Time	V_{FB} > V_{REF}; C_{PWMx} = Open;	$T_{on,\ min}$	200	260	320	ns
Maximum On Time in DCM NCP1681BA Only		$T_{on,\ max,DCM}$	–	30.2	–	μs
REGULATION BLOCK						
Feedback Voltage Reference: @ 25°C Over the temperature range		V_{REF}	 2.475 2.44	 2.50 2.50	 2.525 2.56	V
Ratio for DRE Enable (V_{OUT} Low Detect Lower Threshold / V_{REF}) (guaranteed by design)	V_{FB} decreasing	$V_{DRE}L$ / V_{REF}	95.0	95.5	96.0	%
Ratio for DRE Disable (V_{OUT} Low Detect Higher Threshold / V_{REF}) (guaranteed by design)	V_{FB} increasing	$V_{DRE}H$ / V_{REF}	97.5	98.0	98.5	%
Ratio (V_{OUT} Low Detect Hysteresis / V_{REF}) (guaranteed by design)	V_{FB} increasing	H_{DRE} / V_{REF}	2	2.5	–	%
ZCD PIN						
ZCD Arming Threshold NCP1681AA, AB NCP1681BA	V_{ZCD} increasing	$V_{ZCD(ARM)}$	 – –	 150 300	 – –	mV

Table 4. ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, V_{LVSNS1}= 1.2 V, V_{LVSNS2} = 0 V, V_{FB} = 2.4 V, V_{FAULT} = open, $C_{POLARITY}$ = 100 pF, V_{AUX} = 0 V, V_{ZCD} = 0 V, V_{CS} = 0 V, C_{VCC} = 100 nF, C_{SRL} = C_{SRH} = 100 pF, C_{PWML} = C_{PWMH} = 100 pF, for typical values T_J = 25°C, for min/max values, T_J is – 40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
ZCD PIN						
ZCD Trigger Threshold NCP1681AA, AB NCP1681BA	V_{ZCD} decreasing	$V_{ZCD(TRG)}$	 – –	 30 50	 – –	mV
Threshold for Inrush Current Protection NCP1681AA, AB NCP1681BA		$V_{ZCD(INRUSH)}$	 – –	 30 50	 – –	mV
Propagation delay to (1–D) Drive Pulse	Step V_{ZCD} 0 V to $V_{ZCD(ARM)}$ + 250 mV; Time to PWMx = 2.5 V	$T_{ZCD(ARM)}$	–	45	75	ns
Propagation delay (1–D) Drive Termination	Step V_{ZCD} 1 V to $V_{ZCD(TRIG)}$ – 250 mV; Time to PWMx = 2.5 V	$T_{ZCD(TRG)}$	–	45	75	ns
ZCD Pullup Current Source	V_{ZCD} = 0 V V_{ZCD} = 2.7 V	I_{ZCD}	0.7 0.7	1 1	1.3 1.3	μA
CrM/CCM DETECTION FOR NCP1681Bx						
Switching Frequency Ratio for CCM Detection	F_{CrM} Decreasing; F_{CCM} / F_{CrM}	R_{CCM}	–	111	–	%
Blanking Time for CCM Mode End Detection		T_{CCMend}	288	360	432	ms
Minimum Operating Time in CrM Mode after CCM → CrM Transition		$T_{CrM(Min)}$	210	262	314	ms
Threshold Minimum V_{CS} for CCM Detection		V_{CS_CCM-H}	325	350	375	mV
Ratio Minimum V_{CS} for CCM Detection to Current Limit Threshold		K_{CCM-H}	–	25	–	%
Threshold Minimum V_{CS} for CCM Confirmation		V_{CS_CCM-L}	185	210	235	mV
Ratio Minimum V_{CS} for CCM Confirmation to Current Limit Threshold		K_{CCM-L}	–	15	–	%
MULTIPLIER CIRCUIT						
Multiplier Voltage in CrM/DCM NCP1681BA Only		$V_{M(CrM)}$	2	2.5	3	V
V_M Current capability in CrM/DCM NCP1681BA Only		I_{VM}	450	700	–	μA
V_M Pin Source Current	V_{FB} = 2 V, V_{CS} = 1 V	$I_{M1,LL}$	30.4	35.7	41	μA
V_M Pin Source Current	V_{FB} = 2 V, V_{CS} = 0.5 V	$I_{M2,LL}$	–	17.5	–	μA
Low Line Current Ratio	($I_{M2,LL}$ / $I_{M1,LL}$)	$K_{M1,LL}$	0.44	0.49	0.54	
V_M Pin Source Current High Line NCP1681AA, AB NCP1681BA	V_{FB} = 2 V, V_{CS} = 1 V	$I_{M1,HL}$	 – –	 35.7 150.1	 – –	μA
Ratio of High Line Current to Low Line Current NCP1681AA, AB NCP1681BA	($I_{M1,HL}$ / $I_{M1,LL}$)	$K_{M1,HL}$	 0.97 3.85	 1 4.2	 1.03 4.55	
V_M Pin Source Current High Line NCP1681AA, AB NCP1681BA	V_{FB} = 2 V, V_{CS} = 0.5 V	$I_{M2,HL}$	 – –	 17.5 73.9	 – –	μA
High Line Current Ratio NCP1681AA, AB NCP1681BA	($I_{M2,HL}$ / $I_{M1,LL}$)	$K_{M2,HL}$	 0.44 1.8	 0.49 2.1	 0.54 2.4	

Table 4. ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, V_{LVSNS1}= 1.2 V, V_{LVSNS2} = 0 V, V_{FB} = 2.4 V, V_{FAULT} = open, $C_{POLARITY}$ = 100 pF, V_{AUX} = 0 V, V_{ZCD} = 0 V, V_{CS} = 0 V, C_{VCC} = 100 nF, C_{SRL} = C_{SRH} = 100 pF, C_{PWML} = C_{PWMH} = 100 pF, for typical values T_J = 25°C, for min/max values, T_J is – 40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
MULTIPLIER CIRCUIT						
V_M Pin Source Current, 50% Duty	V_{FB} = 2 V, V_{CS} = V_{ZCD} = 1 V, V_M = 1.875 V; Low Line	$I_{M3,LL}$	–	35.7	–	μA
Low Line Current Ratio, 50% Duty	($I_{M3,LL}$ / $I_{M1,LL}$)	$K_{M3,LL}$	0.99	1	1.01	
CURRENT SENSE BLOCK (CS PIN)						
Low−Line Current Limit Threshold NCP1681AA, AB NCP1681BA		$V_{ILIMIT1(LL)}$	 0.95 1.33	 1 1.4	 1.05 1.47	V
High−Line Current Limit Threshold NCP1681AA, AB NCP1681BA	$\|V_{LS1} - V_{LS2}\|$ = 3	$V_{ILIMIT1(HL)}$	 0.95 0.8	 1 0.84	 1.05 0.88	V
Over−Current Protection (OCP) Delay	Step V_{CS} 0 V to $V_{ILIMIT1}$ + 250 mV; Time to PWMx = 2.5 V	T_{OCP1}	–	45	75	ns
OCP Leading Edge Blanking		$T_{OCP1(LEB)}$	150	220	290	ns
Threshold for Abnormal Current Detection NCP1681AA, AB NCP1681BA	$V_{ILIMIT2}$ = 1.5 * $V_{ILIMIT1(LL)}$	$V_{ILIMIT2}$	 1.425 1.995	 1.5 2.1	 1.575 2.205	V
Abnormal Overstress Timer		$T_{WDG(OS)}$	710	815	950	μs
Consecutive Abnormal Over Current Events to disable controller		$N_{CS(LIM2)}$	–	4	–	
Abnormal Over−Current Protection Delay	Step V_{CS} 0 V to $V_{ILIMIT2}$ + 250 mV; Time to PWMx = 2.5 V	T_{OCP2}	–	45	75	ns
Abnormal OCP Leading Edge Blanking		$T_{OCP2(LEB)}$	85	110	135	ns
CS Pullup Current Source	V_{CS} = $V_{ILIMIT2}$	I_{CS}	0.7	1	1.3	μA
Minimum Current Threshold for THD Enhancer Enable (NCP1681BA)	V_{CS} increasing	$V_{CS(MIN)}$	45	70	95	mV
CS Minimum Current Ratio (NCP1681BA)	$K_{CS(MIN)}$ = $V_{CS(MIN)}$/$V_{ILIM1(LL)}$	$K_{CS(MIN)}$	–	5	–	%
CS Protection Test Current		$I_{CS(TEST)}$	180	235	–	μA
CS Protection Voltage Threshold		$V_{CS(TEST)}$	100	150	200	mV
Recommended CS Filter Resistance		$R_{CS(FILT)}$	1	–	–	kΩ
UNDERVOLTAGE & OVERVOLTAGE PROTECTION						
UVP Threshold	V_{FB} decreasing	V_{UVP}	–	0.3	–	V
Ratio (UVP Threshold) over V_{REF} (V_{UVP}/V_{REF})	V_{FB} decreasing	R_{UVP}	8	12	16	%
UVP Hysteresis	V_{FB} increasing	$V_{UVP(HYST)}$	–	50	100	mV
Soft OVP Threshold	V_{FB} increasing	$V_{softOVP}$	–	2.625	–	V
Ratio (soft OVP Threshold) over V_{REF} ($V_{softOVP}$/V_{REF})	V_{FB} increasing	$R_{softOVP}$	104	105	106	%
Ratio (soft OVP Hysteresis) over V_{REF}	V_{FB} decreasing	$R_{softOVP(H)}$	1.5	2	2.5	%
Fast OVP Threshold	V_{FB} increasing	$V_{fastOVP}$	–	2.7	–	V
Ratio (Fast OVP Threshold) over (soft OVP Upper Threshold) ($V_{fastOVP}$/$V_{softOVP}$)	V_{FB} increasing	$R_{fastOVP1}$	102.4	103	103.4	%

Table 4. ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, V_{LVSNS1}= 1.2 V, V_{LVSNS2} = 0 V, V_{FB} = 2.4 V, V_{FAULT} = open, $C_{POLARITY}$ = 100 pF, V_{AUX} = 0 V, V_{ZCD} = 0 V, V_{CS} = 0 V, C_{VCC} = 100 nF, C_{SRL} = C_{SRH} = 100 pF, C_{PWML} = C_{PWMH} = 100 pF, for typical values T_J = 25°C, for min/max values, T_J is – 40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
UNDERVOLTAGE & OVERVOLTAGE PROTECTION						
Ratio (Fast OVP Threshold) over V_{REF} ($V_{fastOVP}/V_{REF}$)	V_{FB} increasing	$R_{fastOVP2}$	106.5	108	109.5	%
FB Threshold for Recovery from a Soft or Fast OVP	V_{FB} decreasing	$V_{OVPrecover}$	–	2.575	–	V
FB bias Current @ V_{FB}=$V_{softOVP}$ and V_{FB}=V_{UVP}		$(I_B)_{FB}$	50	250	450	nA
PFCOK & BUV PROTECTION						
PFCOK voltage in OFF mode	PFCOK pin sink current = 1 mA	$V_{PFCOK(low)}$	–	–	100	mV
PFCOK current	V_{FB} = 2.5 V, V_{PFCOK} = 1 V	I_{PFCOK}	23	25	27	μA
BUV threshold	V_{FB} decreasing	V_{BUV}	1.95	2.0	2.05	V
BUV delay during which operation is disabled		T_{BUV}	400	500	600	ms
STATIC OVP						
Duty ratio	V_{FB} = 3 V	D_{MIN}	–	–	0	%
SOFT SKIP CIRCUIT						
V_M Threshold Voltage to Enter Skip Mode (NCP1681BA Only)		$V_{SKIP(th)}$	1.2	1.5	1.8	V
Minimum pulse duration for SKIP detection	V_M < $V_{SKIP(th)}$	T_{SKIP1}	56	–	–	μs
PFCOK SKIP Threshold		V_{SKIP2}	0.4	0.5	0.6	V
Minimum PFCOK negative pulse duration for SKIP detection		T_{SKIP2}	10	30	50	μs
V_{FB} lower value at the end of a soft skip cycle burst defined as a V_{REF} percentage		$(R_{FB})_{recover}$	92.5	94	95.5	%
V_{FB} Restart Level in Skip Cycle		$V_{RESTART}$	–	2.35	–	V
Blanking time for operation recovery		$T_{recover}$	400	500	600	ms
V_M Skip Confirmation Window		T_{WINDOW}	–	400	–	μs
FAULT PROTECTION						
OTP Fault Threshold	V_{Fault} decreasing	$V_{FLT(OTP)}$	0.38	0.40	0.42	V
OTP Fault Source Current	V_{Fault} = $V_{FLT(OTP)}$ + 200 mV	I_{FLT}	43	46	49	μA
OTP Detection Filter Delay	V_{Fault} decreasing	$t_{OTP(DLY)}$	22.5	30	37.5	μs
OTP Blanking During Startup		$t_{OTP(BLANK)}$	4	5	6	ms
OTP Fault Recovery Threshold	V_{Fault} increasing	$V_{FLT(REC)}$	0.874	0.92	0.966	V
OVP Fault Threshold	V_{Fault} increasing	$V_{FLT(OVP)}$	2.88	3	3.12	V
OVP Detection Filter Delay	V_{Fault} increasing	$t_{OVP(DLY)}$	22.5	30	37.5	μs
Fault Clamp Voltage	V_{Fault} = open	$V_{FLT(CLAMP)}$	1.15	1.7	2.25	V
Fault Clamp Resistance		$R_{FLT(CLAMP)}$	1.32	1.55	1.78	kΩ
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	Temperature increasing	T_{SHDN}	–	150	–	°C
Thermal Shutdown Hysteresis	Temperature decreasing	$T_{SHDN(HYS)}$	–	50	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Totem Pole Theory of Operation

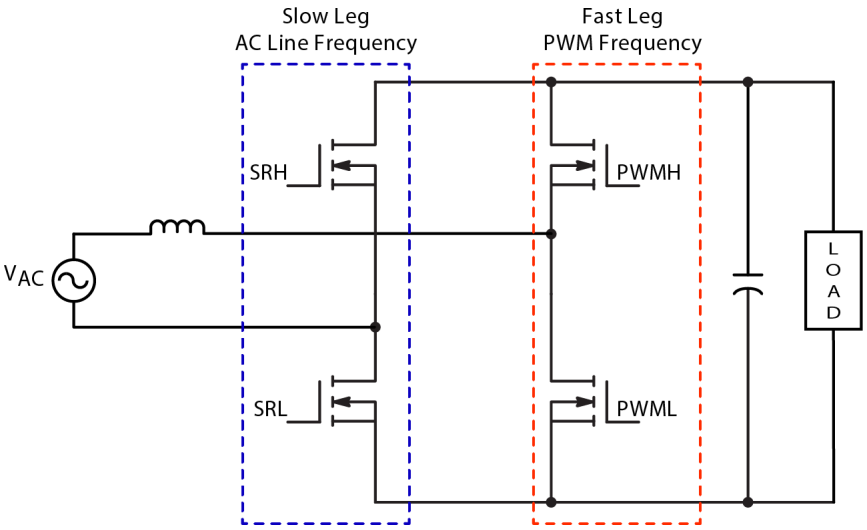


Figure 4. Totem Pole PFC Circuit

The Totem Pole PFC (TPFC) circuit is shown in Figure 4. The topology consists of two half−bridge configurations; one half bridge, commonly referred to as the “Fast Leg” switches at the PWM frequency and the other, commonly referred to as the “Slow Leg” switches at the AC line frequency. The fast leg switches perform the role of the switch and the diode in a classical boost PFC, that is these switches function to regulate the output voltage and shape the input current to provide high power factor and low harmonic distortion. The slow leg switches perform the role of the diode bridge in a classical boost PFC. Active switches with low ON resistance are utilized instead of diodes resulting in improved efficiency. Also, as will be described in the discussion below, the TPFC operates with only one slow leg and one fast leg device in the conduction path whereas the conventional boost PFC operates with two bridge diodes and one active switch or boost diode in the conduction path. Fewer devices in the conduction path and active switches replacing bridge diodes allow the TPFC topology to achieve higher system efficiency and power density than the classical boost PFC.

In Figure 4 the fast leg switches are represented as MOSFETs, but Wide Bandgap (WBG) transistors are generally recommended for NCP1681 applications. WBG devices, whether Silicon Carbide (SiC) or Gallium Nitride (GaN), offer excellent Q_g*$R_{ds(on)}$ figure of merit and virtually no reverse recovery charge, Q_{rr}, making them optimal devices for the TPFC fast leg, particularly when operating in continuous conduction mode (CCM). The PWM drive signals produced by the NCP1681 are logic level signals so an external gate driver IC must be used to properly drive the fast leg switches. A galvanically isolated gate driver, such as NCP51561, is recommended due to the noise induced by the hard switching that occurs in CCM.

The TPFC operates with bidirectional current flow in the inductor and the command of the fast and slow leg switches changes depending on the polarity of the AC line cycle. Operation of the TPFC during the positive and negative half line cycles is illustrated in Figure 5 and Figure 6, respectively.

Positive Half Cycle Operation

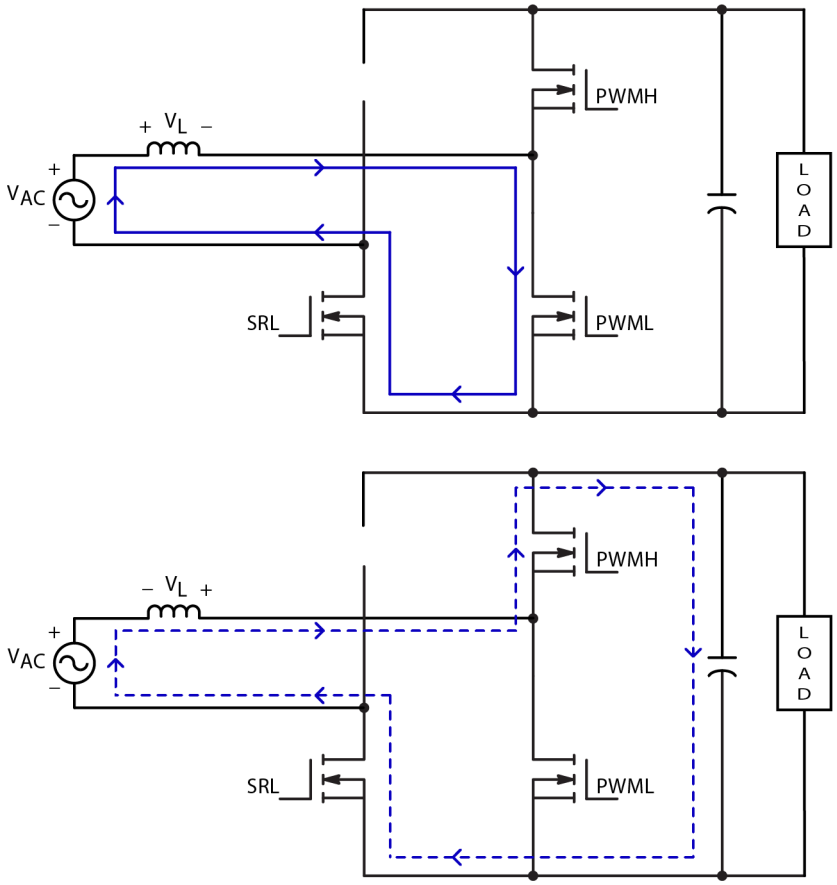


Figure 5. Positive Half Cycle Operation

During the positive AC line cycle the PWML signal is responsible for performing pulse width modulation or duty cycle control of the converter. PWML toggles high turning on the low side fast leg device, allowing current to charge and store energy in the inductor, as shown by the solid blue line in Figure 5. When the PWML signal toggles low the inductor current diverts through the high side fast leg switch, transferring energy from the inductor to the load, as shown by the dashed blue line. In this half line cycle the high side fast leg device does not need to conduct for proper PFC operation, however the PWMH signal can toggle high to turn on the high side device, providing enhanced system efficiency at higher loads. Throughout the positive half line cycle current is flowing left to right through the inductor and always returning to the source through the low side slow leg device, hence the SRL signal will toggle high to turn on the respective slow leg device for optimum converter efficiency.

Negative Half Cycle Operation

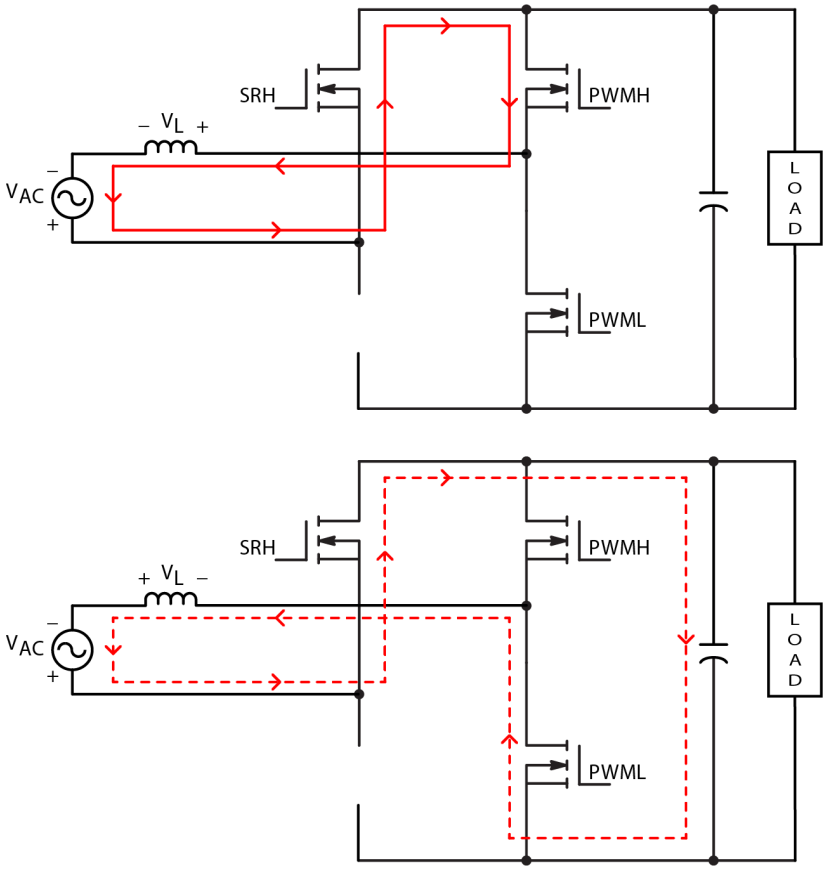


Figure 6. Negative Half Cycle Operation

During the negative AC line cycle the PWMH signal is responsible for performing pulse width modulation or duty cycle control of the converter. PWMH toggles high commanding the high side fast leg device to conduct, allowing current to charge and store energy in the inductor, as shown by the solid red line in Figure 6. When the PWMH signal toggles low the inductor current diverts through the low side fast leg switch, transferring energy from the inductor to the load, as shown with the dashed red line. In this half line cycle the low side fast leg device does not need to conduct for proper PFC operation, however the PWML signal can toggle high to turn on the low side device, providing enhanced system efficiency at higher loads. Throughout the negative half line cycle current is flowing right to left through the inductor and always returning to the source through the high side slow leg device, hence the SRH signal will toggle high to turn on the respective slow leg device for optimum converter efficiency.

V_{CC} Management and Startup Sequence

The NCP1681 controller requires a supply bias of at least $V_{CC(ON)}$, typically 10.5 V, to enable and begin normal operation. Since the controller does not include an internal high voltage startup, the bias supply will have to come from an external source such as a dedicated auxiliary supply or from a downstream converter. Additionally, the controller must have sufficient input voltage (BONOK cleared) and validation that the ac line frequency is within the expected operating range ($N_{DRV\_EN} \geq 4$), then the control can power up on the next rising polarity edge, synchronizing the startup to a positive half line cycle. The startup requirements are summarized:

- Brown−out protection, BONOK, is cleared
- $V_{CC} > V_{CC(ON)}$
- $N_{DRV\_EN} \geq 4$
- Polarity rising edge

If the supply voltage is in the hysteresis band, i.e. if $V_{CC(OFF)} < V_{CC} < V_{CC(ON)}$ then the controller will not start up. This is done to ensure that the minimum specified hysteresis between $V_{CC(ON)}$ and $V_{CC(OFF)}$ of 1.2 V, is available for the device so that the increased current consumption at startup doesn't pull V_{CC} below $V_{CC(OFF)}$, typically 8.8 V. Once the device has been enabled then the V_{CC} voltage can fall to as low as $V_{CC(OFF)}$ without disabling but for startup the V_{CC} voltage must exceed and remain above $V_{CC(ON)}$.

Line Voltage Sensing

Figure 7 shows the recommended application configuration for the line voltage sensing scheme. External resistor dividers are required to divide down two high voltage nodes to perform differential line sensing. The recommended divide down factor for universal input consumer applications is K_{L_DIV}, typically 100; i.e.

$$\frac{R_{LOWERx}}{(R_{LOWERx} + R_{UPPERx})} = \frac{1}{K_{L\_DIV}} \qquad \text{(eq. 1)}$$

such that the low voltage signals which interface to the NCP1681 are approximately 1% of the high voltage signals that are being monitored. The LVSNS1 pin is intended to interface with the low frequency node of the main boost inductor, L_{BOOST}, and the LVSNS2 pin is intended to interface with the bridge voltage of the slow leg power switches. The internal Line Detector circuit is designed with substantially high input impedance allowing for large external resistors to minimize the power dissipation in the dividers, enabling the application to achieve low no load power consumption. Typical values for R_{UPPERx} can be in the range of 5 – 10 MΩ while R_{LOWERx} can be 50 – 100 kΩ. In practice the upper portion of the resistor divider should consist of at least two 1206 components connected in series to withstand the voltage drop.

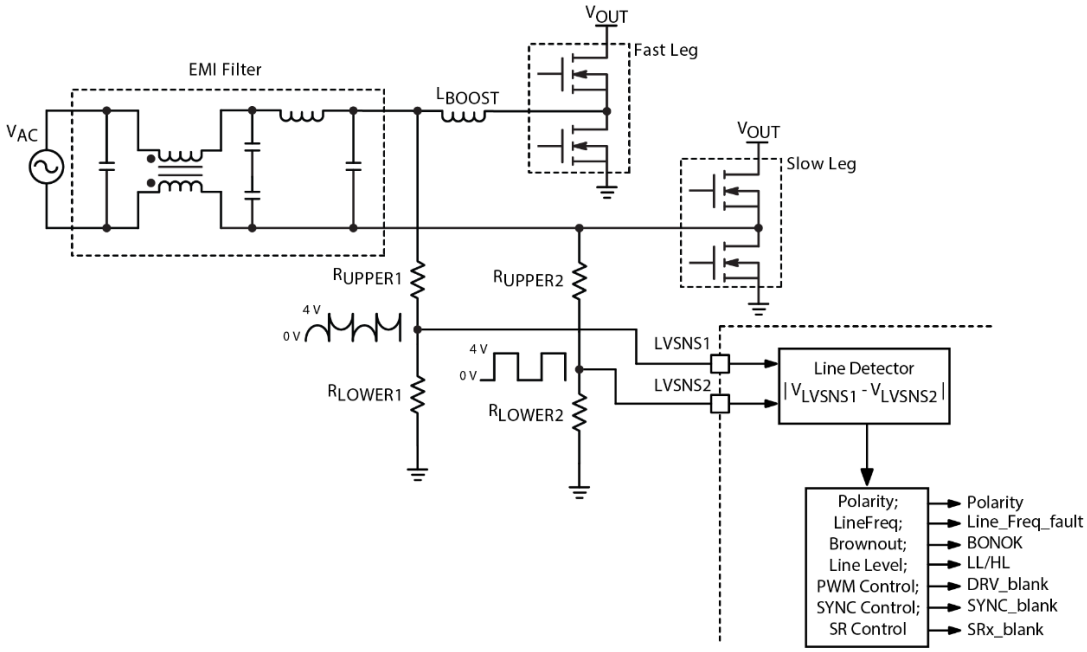


Figure 7. Line Sensing Configuration

In the Totem Pole topology, the AC line voltage floats with respect to the controller ground. This necessitates a differential measurement technique to determine the AC line voltage magnitude. The NCP1681 employs differential voltage detection and rectification to reconstruct a waveform equal to $|V_{LVSNS1} - V_{LVSNS2}|$. For simplicity $|V_{LVSNS1} - V_{LVSNS2}|$ will be referred to as V_{LINE}. The key waveforms are shown in Figure 8. The reconstructed waveform is utilized to perform functions such as brown−out and line level detection where it is necessary to measure the amplitude of the line voltage. The line voltage sensing will additionally be responsible for determining the polarity (i.e. positive or negative half−line cycle) of the AC voltage and for measuring the frequency of the AC line voltage. In total, the line sense will be utilized for the following functions –

a. Polarity detection,
b. AC Line Frequency Monitoring,
c. Brownout protection feature,
d. Line level detection,
e. AC zero crossing drive management

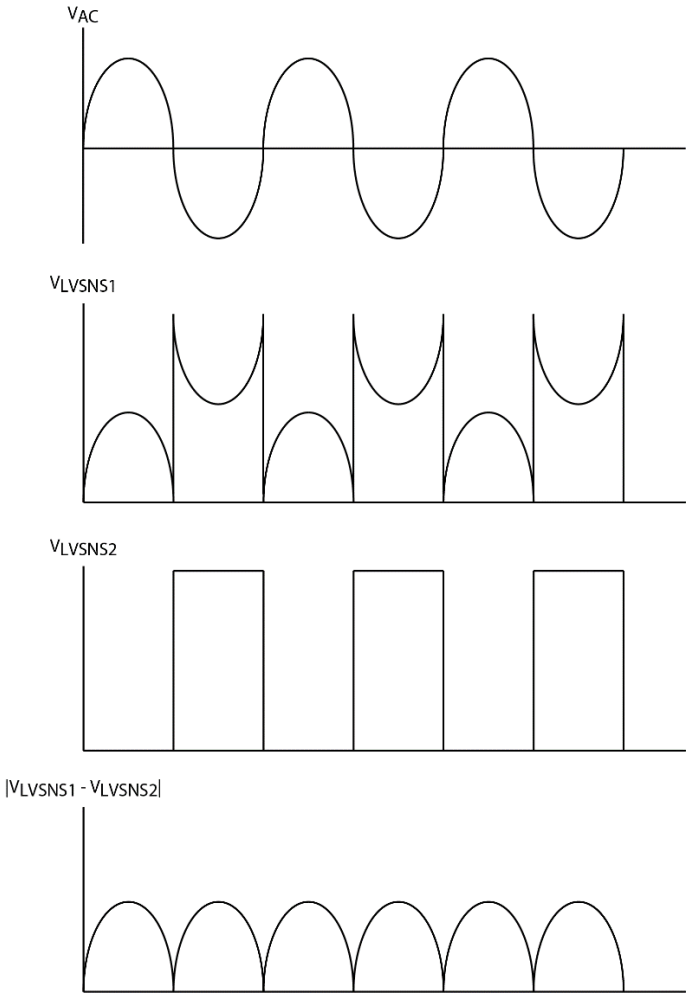


Figure 8. Line Sense Waveforms

Polarity Detection

Figure 9 shows a simplified diagram of the polarity detection circuitry. The two line sense signals are compared directly against each other to determine when they intersect. The intersection or crossover of the two signals indicates that the AC line voltage has changed polarity. External filter capacitance may be added to improve noise immunity of the polarity detection circuitry; the recommend time constant of the RC filter is about 20 – 200 μs, enough to provide noise immunity from the switching frequency of the power supply but not such a large time constant to introduce significant lag in the line sense signals.

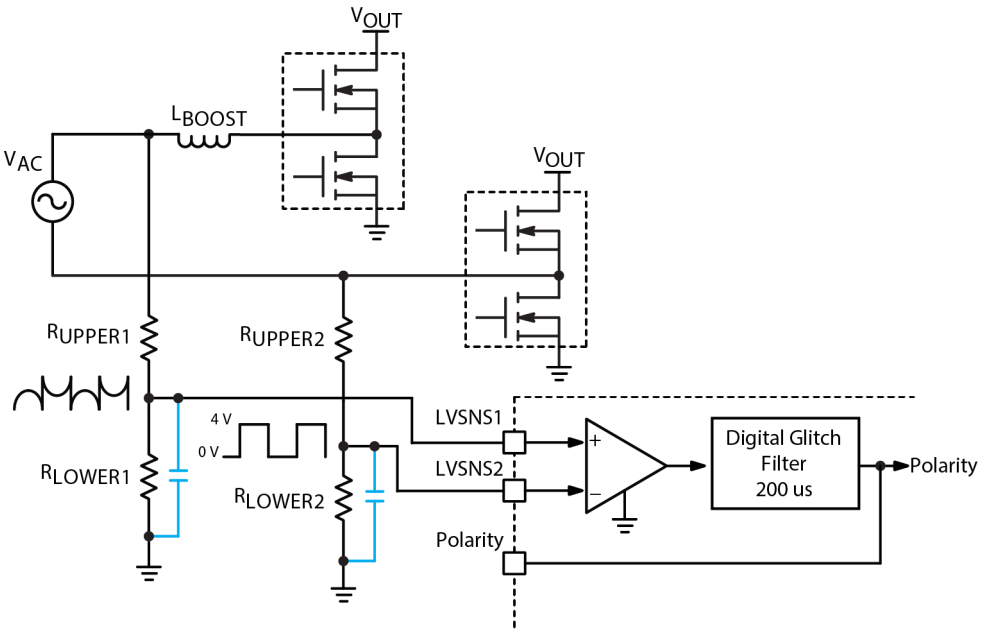


Figure 9. Polarity Detection Diagram

Additionally, the output of the polarity sense comparison circuit is passed through a digital glitch filter which will provide additional immunity if the comparison circuit is toggling repeatedly. The glitch filter has a timer, T_{POL_FILTER}, of 200 μs. The behavior of the filter is shown below in Figure 10. The input to the filter must remain at a logic state (high or low) for greater than the filter's timer for the output to transition to that state. If the input transitions from high to low (or vice versa) but does not remain in that state for a time greater than T_{POL_FILTER}, then the output will remain in its previous logic state and the timer will effectively reset. In Figure 10, time durations t1, t2, t3 and t5, t6, t7 are all less than T_{POL_FILTER} and hence the output of the filter remains unchanged. Time durations t4 and t8 are greater than T_{POL_FILTER}, causing the output to transition to the new state.

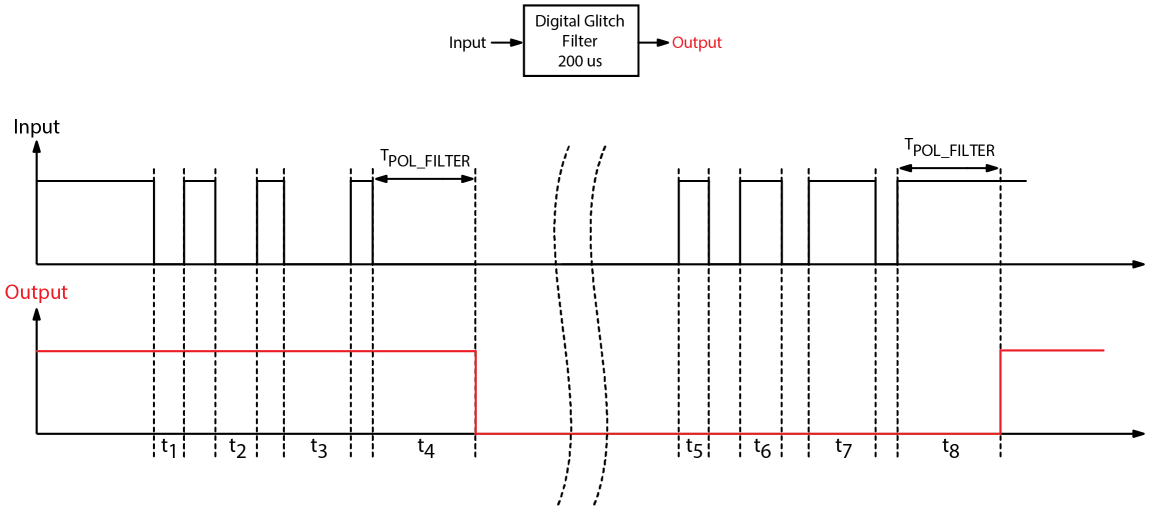


Figure 10. Polarity Glitch Filter Operation

AC Line Frequency Monitoring

The NCP1681 controller comes with an optional line frequency monitoring circuit. The NCP1681 utilizes timers & counters to monitor the AC line frequency ($T_{LINEFREQ}$) to ensure that the polarity comparator output toggles at a rate consistent with the mains frequency specification of 45 – 65 Hz. A timing diagram of the AC line frequency monitor operation is shown in Figure 11. Practically the controller measures the time between every edge transition of the filtered polarity signal. If one timing interval, such as t_1, measures outside of the expected frequency range then the controller will disable the slow leg drive signals, SRL and SRH, and start a 100 ms timer, $t_{LINEFREQ(DLY)}$. If a timing interval within the specification is measured prior to

$t_{LINEFREQ(DLY)}$ expiring, then $t_{LINEFREQ(DLY)}$ is reset and slow leg drive pulses are again enabled. This is shown with timing interval t_2 and t_3.

Should the polarity toggles continue to measure outside of the mains frequency specification and the timer expires then the controller will disable fast leg drive pulses and enter fault mode as shown after t_5. Note that throughout timing interval t_5 the slow leg pulses are disabled. While in fault mode the polarity signal and the line frequency monitor will remain active, performing continuous time interval measurements of the polarity signal. The device will auto−recover from the fault mode once the device detects 4 consecutive polarity edges that are within the line frequency specification, same as a new startup. The thresholds for the AC line frequency monitor are given by $t_{LINE(65)}$, nominally 72 Hz, and $t_{LINE(45)}$, nominally 42 Hz. These thresholds are designed to provide some margin so that under worst case tolerance the AC line frequency can always operate from 45 – 65 Hz.

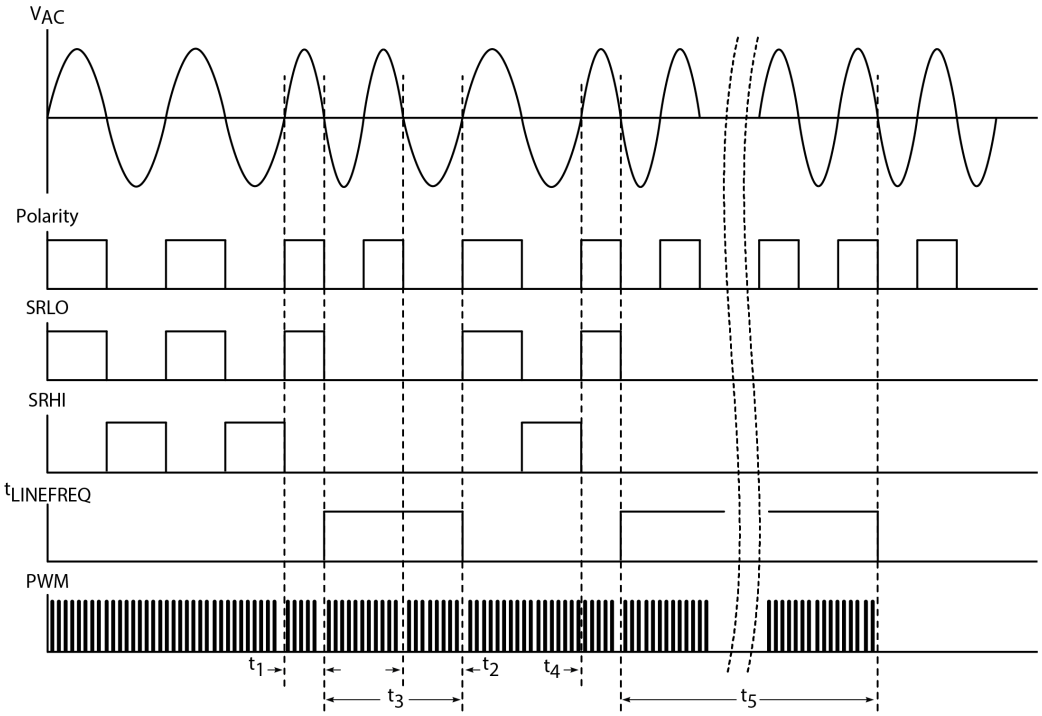


Figure 11. Line Frequency Faults Timing Diagram

As previously mentioned, startup of the NCP1681 controller is synchronized to the rising edge of the filtered polarity signal and requires at least 4 consecutive half−line cycles (polarity toggles) to be within the valid $T_{LINEFREQ}$ duration. The controller enable counter is denoted as N_{DRV_EN} in the electrical table. Line Frequency operation is shown in Figure 12 where the Line Freq OK flag is set high on the rising edge of the 4th consecutive polarity toggle with valid time duration. The rising edge of the polarity signal indicates that the AC line is entering a positive half line cycle which is the preferred conduction angle for starting up the application because the low−side fast leg device will be the duty cycle controlled device.

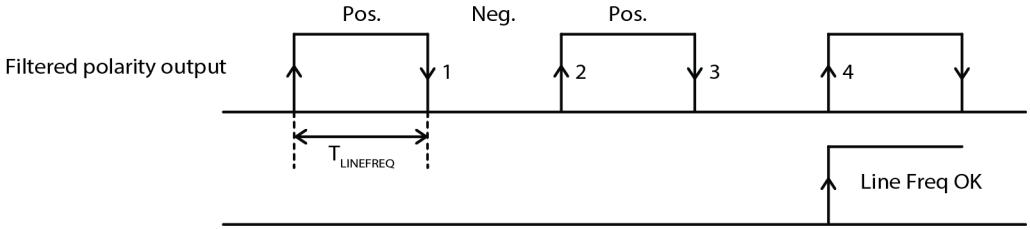


Figure 12. Polarity Startup Timing Diagram

Brown−Out and Line Sag Protection

The NCP1681 feature set includes line voltage Brown−out (BO) and Line sag (SAG) detection. These detection circuits function collaboratively as a line voltage UVLO, enabling drive pulses when the peak line voltage exceeds the $V_{BO(start)}$ threshold, typically 1.1 V, and disabling drive pulses when the line voltage falls below the $V_{BO(stop)}$ threshold, typically 1 V, for a given timer duration. Considering that the LVSNSx inputs are recommended to be 1% of the AC line voltage, this translates to a nominal enable threshold of ~ 110 V, or ~ 78 V_{AC}, and a nominal disable threshold of ~ 100 V, or ~ 71 V_{AC}.

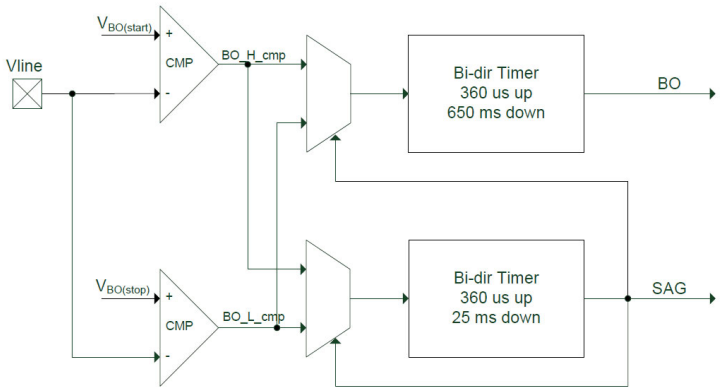


Figure 13. BO/SAG Detection Circuit

Figure 13 is a representative schematic of the NCP1681 BO/SAG detection circuitry. The circuitry monitors the line voltage, V_{LINE}, generated by the NCP1681's internal differential line sensing. V_{LINE} is compared against the two V_{BO} thresholds. Both the BO and SAG voltage thresholds are the same, with the difference between the two features being the timing after which the respective output is set high, and the action taken by the controller after each of the respective outputs. Figure 14 illustrates the controller response during a line sag and brownout.

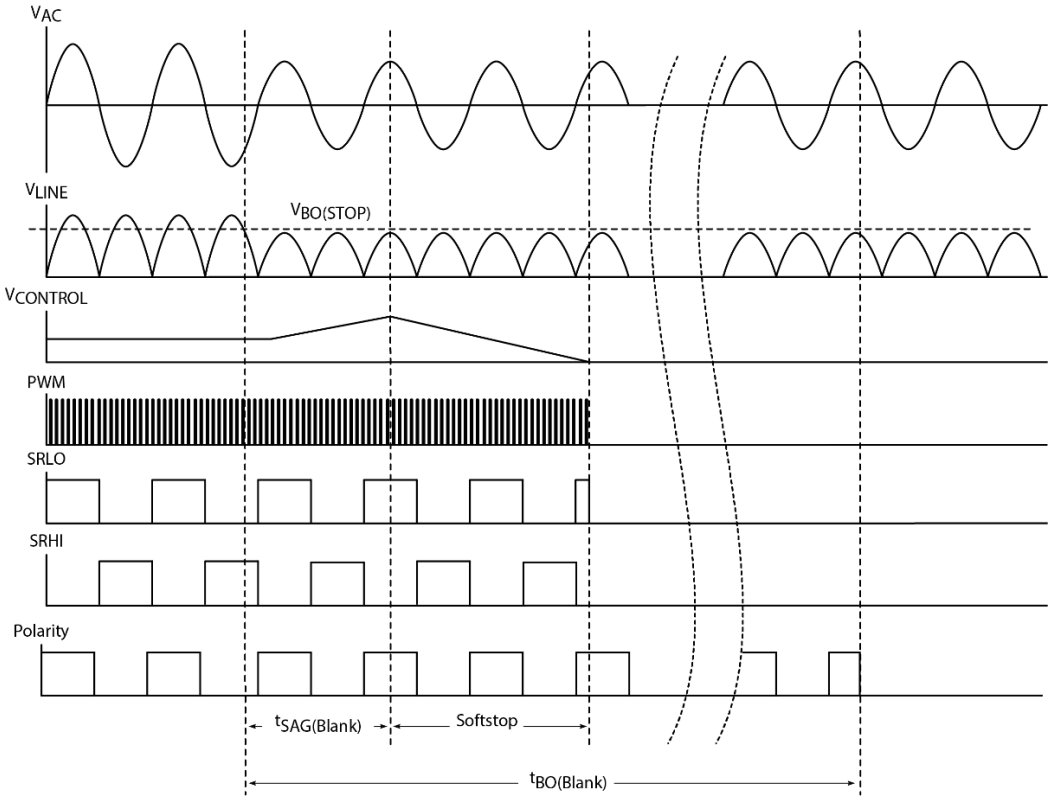


Figure 14. Line Sag and Brownout Timing Diagram

The 25 ms SAG timer, $t_{SAG(blank)}$, allows the application to sustain a line voltage dropout for a single AC line cycle while the NCP1681 continues to deliver drive pulses. If the SAG timer expires, the controller will enter a soft stop period where the internal control voltage is slowly discharged to 0 V and the pulse width of the PWM is gradually narrowed, reducing the power delivery of the application. After the soft stop period the polarity signal remains active and the controller will be ready for immediate restart should the line voltage exceed the $V_{BO(start)}$ threshold. If the 650 ms brown−out timer expires, the NCP1681 will disable the polarity detection circuit and reset the device, including any latching faults. When the application restarts from a BO the controller functions as it would for an initial power up.

Line Range Detection

The NCP1681 features input voltage range detection, which distinguishes between high line (nominally 230 V_{AC}) and low line (nominally 115 V_{AC}) input voltages. The input voltage range is detected based on the peak voltage measured with the reconstructed V_{LINE} signal. By default, the controller will power up into low line mode. If V_{LINE} exceeds the high line threshold, V_{HL}, typically 2.36 V, for a duration longer than $t_{filter(HV)}$, typically 300 μs, the controller transitions to high line mode. Once in high line mode the peak line voltage must fall below V_{LL}, typically 2.22 V, for a duration longer than $t_{blank(LL)}$, typically 25 ms, to enter back into the low line mode. The blanking duration, $t_{blank(LL)}$, is set long enough to allow the controller to remain in high line mode in the event of a single line cycle dropout.

Should the controller transition from high line to low line mode, a lockout timer $t_{line(lockout)}$, typically 500 ms, is enabled. The lockout timer blocks the controller from transitioning back to high line immediately after a low line transition for the duration of the timer, preventing the controller from oscillating between low line and high line mode. The transition thresholds of 2.36 and 2.22 V typically translate to line voltages of 167 and 157 V_{AC}, respectively, which are intermediate voltages that do not correspond to any national standard for AC mains, leaving little likelihood that the input voltage to the application will operate near the transition thresholds. Further, the transition thresholds have a minimum hysteresis, $V_{LR(HYS)}$, of 100 mV to act as another protection against the device oscillating back and forth between low and high line.

The purpose of line range detection is that the controller modifies the gain of the internal digital compensator in order to optimize performance and operation of the PFC for universal, wide−input mains applications. Specifically, the loop gain of the digital compensator is reduced by a factor of 4 when the device detects that it is in the high line range.

AC Zero Crossing Management

AC zero crossing management is the feature in the NCP1681 that determines when to enable and disable the various drive signals at the beginning and end of each of the half line cycles. This feature is critical to the robustness and performance of the Totem pole topology. The NCP1681 features 6 drive signals that can be divided into three classes: 1) The primary or duty−cycle controlled PWM drive signal; 2) The synchronous (sync) PWM drive signal that occurs during the (1 − d) portion of the switching period; and 3) The slow leg “rectifier” or SR drive signal that switches once per half line cycle. Each drive signal has a respective stop and start threshold, which is a function of the line voltage amplitude, V_{LINE}, where $V_{LINE} = |V_{LVSNS1} - V_{LVSNS2}|$ as previously mentioned.

Figure 15 illustrates the zero crossing management thresholds for the primary PWM drive, denoted as PWMd. The same stop and start principle applies to the Synchronous PWM and SR drives, although with different thresholds.

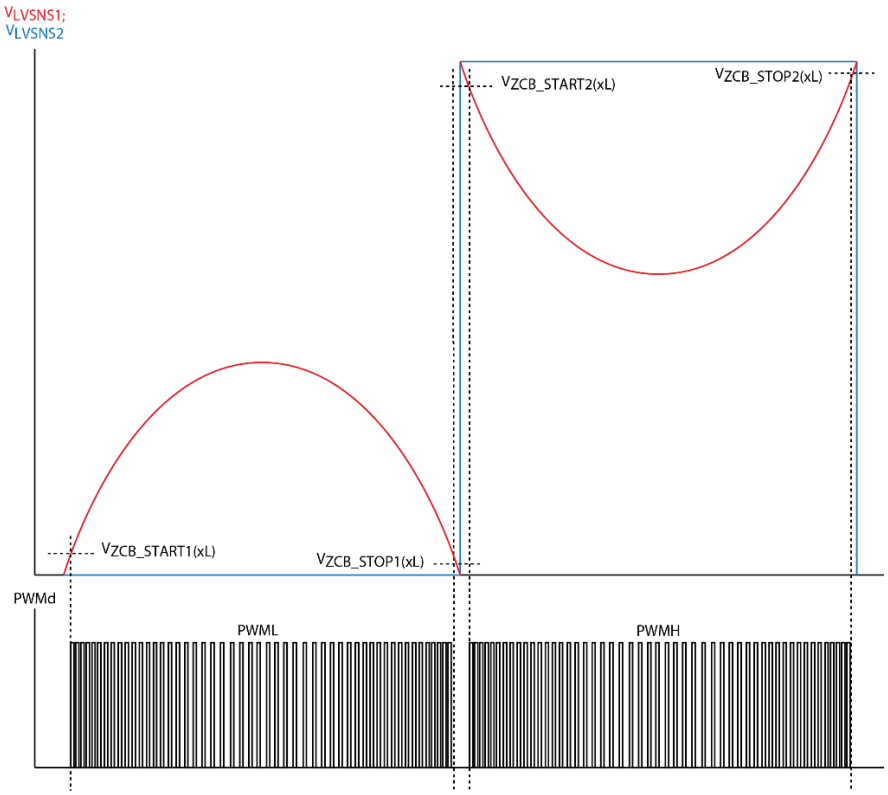


Figure 15. AC Zero Crossing Management Thresholds

Figure 15 shows a full AC line cycle beginning with a positive half−line cycle, i.e. conduction angle between 0 – 180°. In the positive half−line cycle the voltage at the LVSNS2 pin is pulled to 0 V and the voltage at LVSNS1 is increasing proportional to the AC line amplitude. When the AC line amplitude exceeds the threshold $V_{ZCB\_START1(xL)}$, typically 120 mV, the controller begins issuing drive signals to the duty−controlled device, PWML in this case. As the conduction angle approaches 180°, V_{LINE} will eventually fall below the $V_{ZCB\_STOP1(xL)}$ threshold, typically 100 mV, and the controller will blank drive pulses to the duty−controlled device.

In the negative half line cycle the zero crossing management works largely the same as positive half line cycle with the controller processing the different LVSNS signals that are unique to negative half line cycle operation. In this half line cycle LVSNS2 is pulled up to a voltage proportional to about 1% of the PFC bulk voltage, and the LVSNS1 decreases in amplitude relative to the controller GND pin, but increases in amplitude relative to the LVSNS2 signal. The controller's differential line sensing reconstructs $V_{LINE} = |V_{LVSNS1} - V_{LVSNS2}|$ so that V_{LINE} is symmetrical in positive and negative half line cycle and the zero crossing management can use the same comparison thresholds for both half line cycles. The $V_{ZCB\_START2(xL)}$ threshold is 120 mV, and the $V_{ZCB\_STOP2(xL)}$ threshold is 100 mV, same as the start and stop thresholds in positive half line cycle, ensuring that the zero crossing management is symmetric across a full AC line cycle.

Zero crossing management of the synchronous PWM and SR drives follows the same principle as that used to manage the primary PWM drive, however the thresholds are higher as the primary PWM switches for a greater portion of the half line cycle. For the slow leg SR drive, $V_{SR\_START1(xL)}$ is typically 200 mV and $V_{SR\_STOP1(xL)}$ is typically 180 mV and because operation is symmetric the start and stop thresholds in negative half line cycle are the same. For the sync drive, the start threshold, $V_{SYNC\_START1(xL)}$, is typically 220 mV and the stop threshold is typically 200 mV.

All the thresholds in the AC zero crossing management block include hysteresis to ensure stable operation without repeated enabling and disabling should noise corrupt the LVSNS signals. Also, all the drive signals are disabled before the AC line voltage reaches its true zero crossing. While this can lead to a small amount of increased zero crossing distortion, the benefit of disabling all drives is to create a quite environment to ensure the precision and robustness of the polarity signal which is critical to guarantee that the PWM and SR drive signals are directed to the proper device during the respective half line cycle.

Open Loop Drive Pulses

Another critical feature of the NCP1681 is the open loop drive pulses that are issued immediately following a polarity transition. After the AC line zero crossing, the slow leg bridge maintains a residual voltage charge from the previous half line cycle and must be transitioned from V_{BULK} to 0 V (or vice versa) during the upcoming half line cycle.

Considering that PWM−controlled drive pulses near an AC line zero crossing would typically operate with a high duty cycle, using these pulses to transition the slow bridge voltage can result in excessively high current spikes in the inductor; hence it is beneficial to use shorter drive pulses with a smaller, fixed duty cycle to initiate the slow leg bridge node transition. The ON time of the main duty−controlled FET is gradually increased during this phase to assist the slow leg bridge node voltage in transitioning between the bulk voltage and ground. The OFF time of the main duty−controlled FET is also gradually increased during this phase to maintain the same duty ratio. During the open loop drive pulses, the slow leg drive and (1−d) drives are held low, and the current sense input is blanked. The duration and period of the open loop drive pulses is captured in Table 5.

Table 5. OPEN LOOP DRIVE PULSES

	Ton (μs)	Toff (μs)	Period (μs)	
1st pulse	1	3	4	
2nd pulse	2	6	8	
3rd pulse	4	12	16	
4th pulse	6	18	24	
			52	total

Figure 16 provides an annotated timing diagram of a zero crossing transition including the open loop drive pulses. For simplicity, the sync PWM (1−D) drive signals are not shown in this figure.

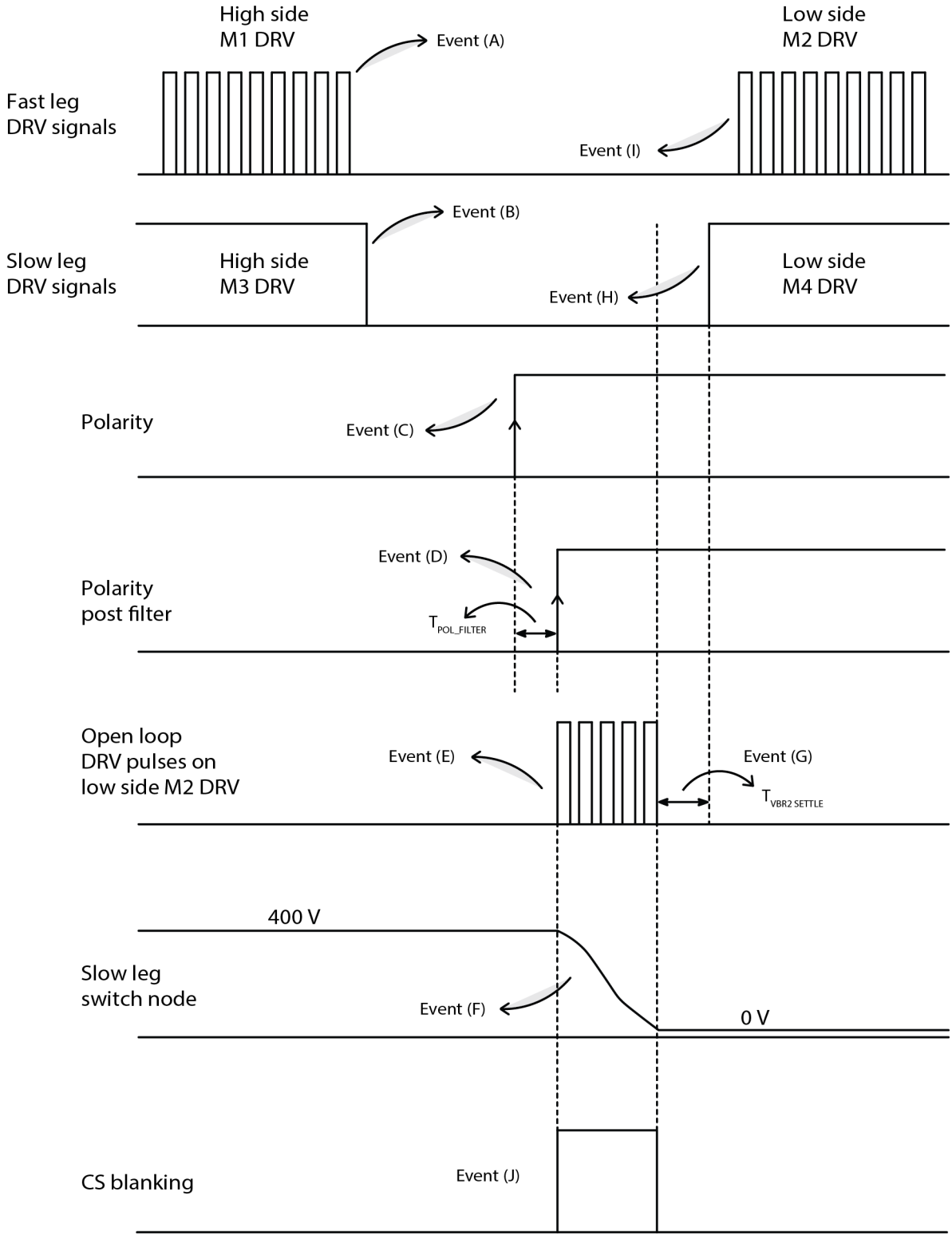


Figure 16. Zero Crossing Timing Diagram

Event (A) – When the sensed line voltage falls below $V_{ZCB\_STOP2(xL)}$, the 'D' drive signal is disabled.

Event (B) – When the sensed line voltage falls below $V_{SR\_STOP2(xL)}$, the slow leg drive signal is disabled. Events (A) & (B) can occur at the same instant or event (A) slightly before or after event (B).

Event (C) – The two sense nodes cross over, representing the actual AC phase reversal instant.

Event (D) – The polarity edge after the filter.

Event (E) – Open Loop Drive pulses issued on the low side M2 (PWML) drive during the negative to positive half line cycle transition or on the high side M1 (PWMH) drive during the positive to negative half line cycle transition.

Event (F) – The open loop drive pulses assist the slow leg switch node transition from 400 V to 0 V or from 0 V to 400 V.

Event (G) – Settling of the slow leg switch node voltage.

Event (H) – Low side slow leg M4 is enabled if the line voltage exceeds $V_{SR\_START1(xL)}$.

Event (I) – Fast leg drive M2 is enabled if the line voltage exceeds $V_{ZCB\_START1(xL)}$. Note that Event(H) doesn't necessarily occur before Event(I); based on the selected options it is possible that Event(I) will occur first.

Event (J) – The current sense used for CCM duty cycle modulation (V_M generation) is blanked/shorted during event (E)/(F). This ensures that the control loop does not respond to this interval.

Operating Modes

The NCP1681 is available in two versions: The "A" version operates at a fixed switching frequency with predictive current mode control, making it well suited for high power (> 1 kW) CCM applications where full load efficiency and low harmonic distortion are critical design requirements. The "B" version is a Multi−Mode (MM) device which can operate in fixed frequency CCM at high power, Frequency Clamped Critical Conduction Mode (FCCrM) at medium loads, and discontinuous conduction mode (DCM) with reduced switching frequency at lighter loads. The MM device is best suited for applications where the output power requirement is ~ 300 W – 1 kW or where light load efficiency and THD must be optimized. Additionally, the MM control algorithm enables higher power density for the boost inductor when compared to typical CCM applications.

Multi−Mode Operation

The "B" version of the NCP1681 controller is designed for Multi−Mode operation where the converter can operate in fixed frequency CCM at heavy loads, Frequency Clamped Critical Conduction Mode (FCCrM) at medium loads, and discontinuous conduction mode with valley switching at light loads. Transitioning between the different operating modes is dependent on the duration of the inductor current conduction period. This is illustrated in Figure 17.

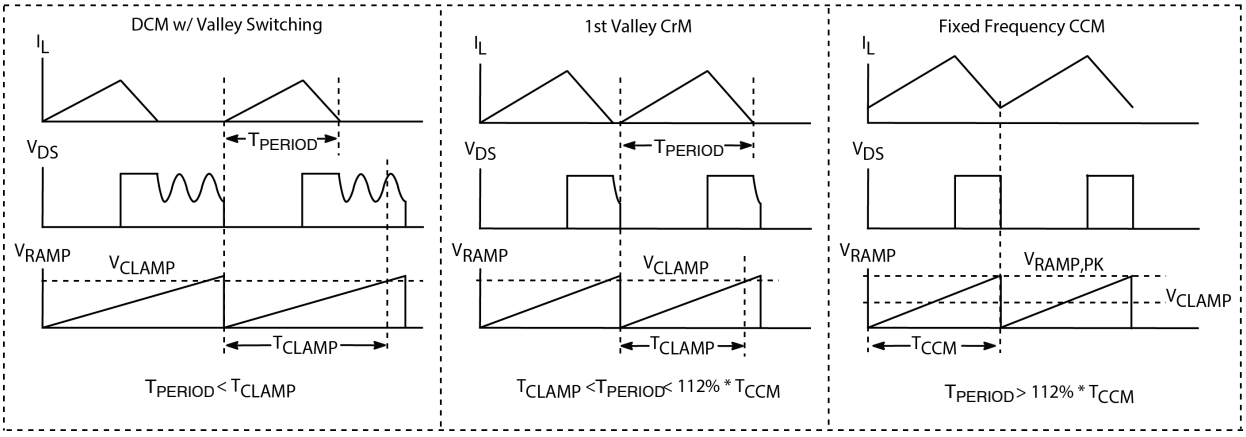


Figure 17. Multi−Mode Operating Modes

In FCCrM, the controller operates in variable frequency critical conduction mode (CrM) if the switching frequency remains below the frequency clamp threshold of 130 kHz. Once the switching frequency exceeds the clamp frequency the controller transitions into discontinuous conduction mode (DCM) with turn−on of the next switching cycle synchronized to the valley of the switch node resonance. At medium loads, transitions between CrM and DCM can occur within half of the AC line cycle. Often, the controller will operate in CrM near the peak of the AC line where the inductor conduction period is longer and switching frequency is lower, and transition to DCM as the AC line voltage approaches zero and the inductor conduction period reduces.

As the load reduces the converter may operate in DCM across the entire AC half−line cycle, switching in different valleys throughout. With further reduction in load the controller enters a switching frequency reduction mode where the switching frequency is pushed to lower frequencies the lighter the load. The frequency reduction in

DCM is achieved by a novel ramp modulation circuit that forces longer switching periods, and more resonant valleys as the load is decreasing. As the load decreases towards 0, the controller clamps the switching frequency to a minimum, F_{MIN}, typically ~ 30 kHz, to mitigate audible noise. All the transitions with FCCrM are determined exclusively based on the inductor conduction period and the controller performs these transitions seamlessly causing no discontinuity in operation while maintaining good power factor.

Fixed frequency CCM operation is obtained in heavy loads when the inductor conduction period regularly exceeds 112% of the CCM switching period, T_{CCM}. In NCP1680BA the CCM switching frequency is 65 kHz so the inductor conduction period must exceed ~ 17.2 μs (1.12 / F_{CCM}). In addition to the switching frequency threshold, there are multiple conditions that must be met for the controller to transition to CCM operation. These conditions are summarized here:

- The inductor current conduction period must exceed 112% of the CCM switching period for at least 8 consecutive switching cycles.
- The peak upslope current measured at the CS pin must exceed a minimum value equal to 25% of the low line CS peak current limit. This threshold, V_{CS_CCM-H}, is nominally 350 mV.
- The controller cannot transition back into CCM immediately following a transition to CrM. A CCM → CrM transition requires at least 260 ms of CrM operation before the controller allows a transition back to CCM.

Once the controller has transitioned to fixed frequency CCM operation it will remain in this operating mode until meeting the criteria to exit CCM. In this operating mode the PFC will switch at a fixed frequency across the entire AC line cycle regardless of the duration of the inductor current conduction period. There is no valley synchronization for turn−on even if the inductor has completed demagnetization and the switch node is resonating.

The criteria to exit CCM are intended to provide some hysteresis in output power so that the controller does not continuously oscillate between CrM and CCM operation. To exit CCM, the PFC output power must have reduced enough that the following exit conditions are met:

- The inductor current conduction period must not exceed 112% of the CCM switching period for at least 8 consecutive switching cycles.
- The peak upslope current measured at the CS pin must be continuously below a minimum value equal to 15% of the CS peak current limit. This threshold, V_{CS_CCM-L}, is nominally 210 mV.
- Either of the two criteria listed above must continue for a period of at least T_{CCMend}, nominally 360 ms.

Fixed Frequency PWM Operation

In fixed frequency operation the NCP1681 incorporates a predictive average current mode control scheme to accomplish power factor correction and output voltage regulation. This control method utilizes a transconductance multiplier, illustrated in Figure 18, which senses the inductor current and produces an output current proportional to the inductor current. The multiplier receives three input signals: (A) 2 V voltage reference, (B) the reconstructed inductor current as a sum of two signals – the upslope current sensed by the CS pin and downslope current sensed by the ZCD pin, and (C) the control voltage from the output of the digital compensator. The multiplier output current is fed into an external resistor, R_M, that sets the multiplier voltage, V_M, which is then used for duty cycle modulation. A capacitor to ground in parallel with R_M is needed to filter the switching ripple present on V_M. The recommended time constant for the multiplier filter is 50 – 100 μs.

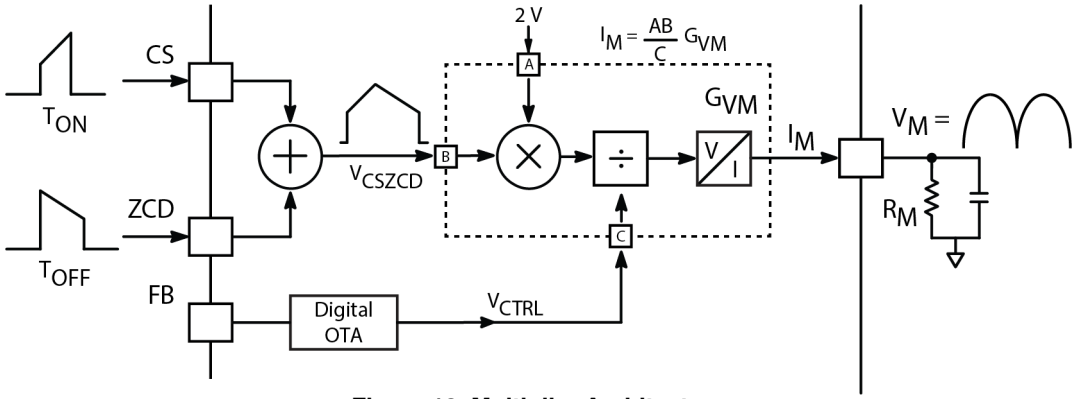


Figure 18. Multiplier Architecture

The voltage generated at the output of the multiplier is shown in Equation 2 where G_{VM} is the transconductance of the multiplier, nominally 75 μA/V.

$$V_M = \frac{2 \cdot V_{CSZCD}}{V_{CTRL}} \cdot G_{VM} \cdot R_M \qquad \text{(eq. 2)}$$

This voltage is utilized in the PWM drive control logic to command the switching duty cycle of the PWM controlled switch. The switching duty cycle, *d*, and complement, *d'*, are determined by the following equations where $V_{RAMP,PK}$ is nominally 3.75 V:

$$d = 1 - \frac{V_M}{V_{RAMP,PK}} \quad \text{(eq. 3)}$$

$$d' = \frac{V_M}{V_{RAMP,PK}} \quad \text{(eq. 4)}$$

To achieve good power factor and low harmonic distortion, PFC converters must control the amplitude of the inductor current so that the inductor current effectively follows the waveshape of the AC input voltage throughout AC voltage line cycle. This is typically accomplished by compensating the PFC with a suitably low bandwidth (< 20 Hz) and having a control algorithm which sets the inductor current to be directly proportional to the input voltage. In the NCP1681, the loop bandwidth requirement is accomplished by the digital compensator and the inductor current shaping is achieved by multiplier voltage control of the duty cycle.

The multiplier resistance, R_M, impacts the loop dynamics and controls the maximum power capability of the PFC. Equation 5 should be used to calculate the maximum value of R_M. This calculation should be done at the lowest RMS input voltage for the application. In Equation 5 the maximum control voltage of 4.2 V should be used for V_{CTRL}, and the value of K_{ZCD} is the scaling factor of the inductor current to ZCD voltage, typically equal to the R_{ZCD} resistor value established later in the datasheet.

$$R_M < \frac{\eta \cdot V^2_{IN} \cdot V_{RAMP,PK} \cdot V_{CTRL}}{2 \cdot V_O \cdot P_O \cdot G_{VM} \cdot K_{ZCD}} \quad \text{(eq. 5)}$$

On Time Modulation Block

While in FCCrM the NCP1681Bx operates with a constant on−time control algorithm. The on time of the main PWM switch is controlled by the control voltage and a modulating ramp as shown in Figure 19.

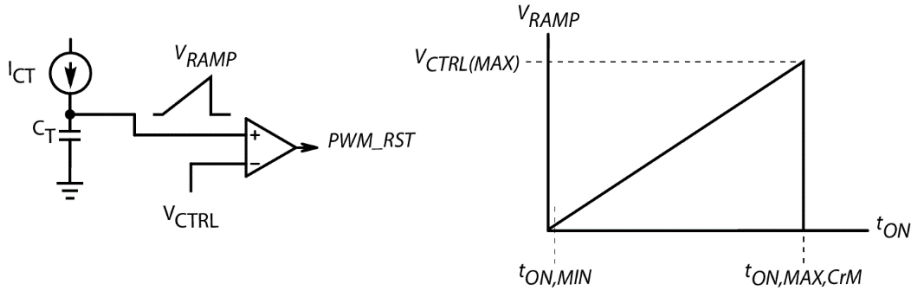


Figure 19. On Time Modulation

The circuitry for the on−time modulator is internal to the NCP1681; the compensation voltage is generated by the internal digital compensator and translated into the analog domain, and the timing components for the modulator ramp are also internal. In CrM the slope of the modulating ramp is fixed and the maximum on time, $T_{on,max,CrM}$, occurs when the compensation voltage has railed to $V_{CTRL(MAX)}$ of 4.2 V.

Designing for MM operation requires designing the inductor to switch below the CCM switching frequency at a given line voltage and power level. Equation 6 can be used to approximate the inductor value needed to achieve the desired transition point at a given output power, P_{TRAN}. For example, to transition from CrM to CCM at P_{TRAN} = 250 W with an input voltage of 90 V, an inductance of ~ 180 μH is needed.

$$L = \left(\frac{1.12}{F_{CCM}}\right) \cdot \left(\frac{\eta \cdot V_{IN}{}^2}{2 \cdot P_{TRAN}}\right) \cdot \left(\frac{V_O - \sqrt{2} \cdot V_{IN}}{V_O}\right) \quad \text{(eq. 6)}$$

As long as the application remains in CrM operation the average input current to the PFC is approximately equal to half of the peak inductor current, i.e., and a modulating ramp with a fixed slope will continue to achieve good power factor. However, when the application transitions to DCM operation the inductor current remains at zero for some portion of the switching cycle and the input current will begin to distort unless that portion of the switching cycle is compensated out. Figure 20 shows a sample inductor current in DCM operation and the associated dead time that occurs prior to the next drive pulse.

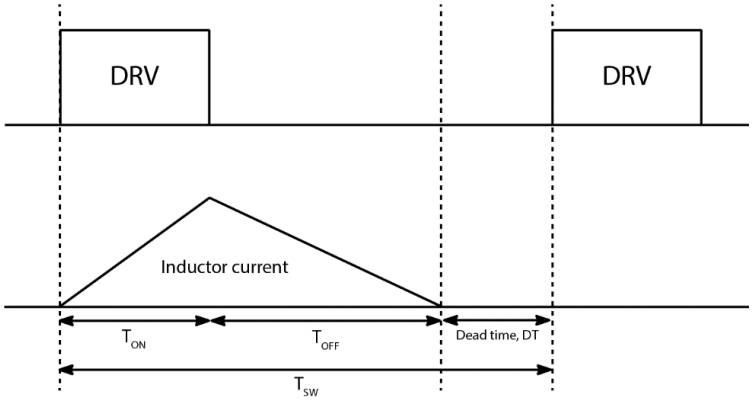


Figure 20. DCM Operation and Dead Time Compensation

In DCM the average input current is now a function of the dead time, specifically

$$I_{in} = \frac{I_{L,PK}}{2} \cdot \frac{T_{ON} + T_{OFF}}{T_{SW}},$$

and the input current will begin to distort if the on−time generator continues using a modulating ramp with a fixed slope. The NCP1681 dead time compensation mitigates input current distortion, retaining good power factor across all operating modes, by adjusting the slope of the modulating ramp by a factor equal to

$$k_{DT} = \frac{T_{ON} + T_{OFF}}{T_{SW}}.$$

Multiplying the slope of the modulating ramp by a factor of k_{DT} increases the on−time inversely proportionally to k_{DT} compensating out the effects of the inductor current dead time and allowing the application to maintain good power factor performance across CrM and DCM operation.

Output Voltage Regulation Block

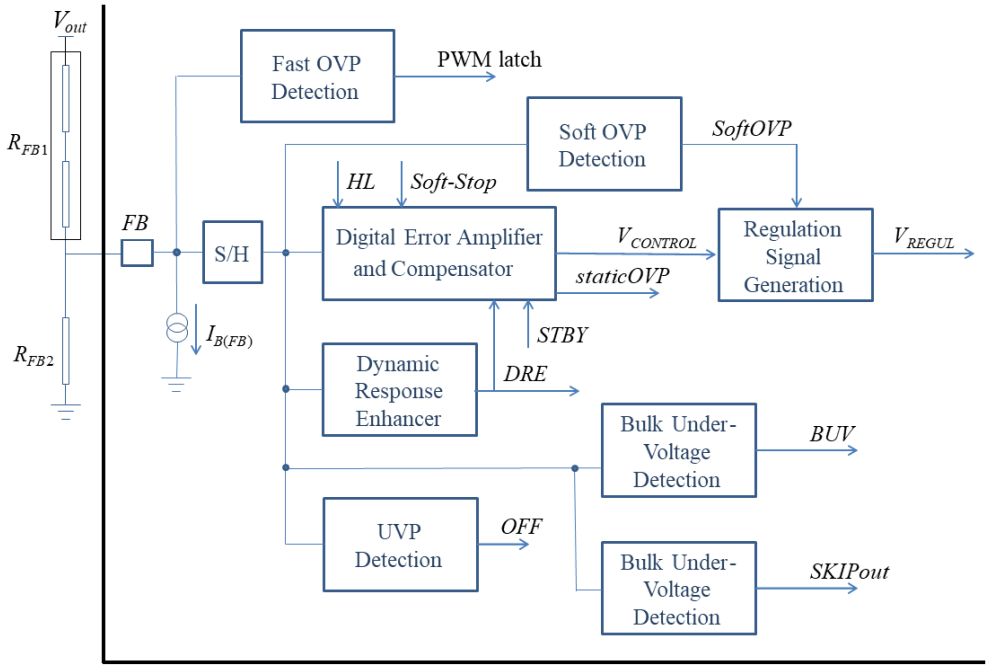


Figure 21. FB and Regulation Architecture

The general structure of the feedback and regulation architecture is shown in Figure 21. The bulk voltage is divided down via a resistor divider and input to a sample and hold circuit which passes the sensed voltage to the input of the error amplifier where it is compared against a 2.5 reference voltage.

The NCP1681 is internally compensated with a digital error amplifier and a control voltage ripple cancellation

circuit. The “Digital Error Amplifier and Compensator” block performs the compensation generating the error voltage, $V_{CONTROL}$, and the “Regulation Signal Generation” block performs additional processing of the error voltage, including the ripple voltage cancellation, to generate the V_{REGUL} signal. Practically, in FFCrM operation the V_{REGUL} signal is the digital domain version of V_{CTRL} signal from Figure 19 which dictates the on−time of the application.

The compensation in NCP1681 is equivalent to a Type−II analog compensator as shown in Figure 22 with the following component values: G_{OTA} = 200 μS, R_Z = 24 kΩ, C_Z = 4.62 μF, C_P = 97.24 nF. Based on these values the key characteristics of the compensator are the following:

- Mid−band gain = 20*log10(R_Z*G_{OTA}) = ~ 13.6 dB
- Compensation zero location = 1/(2*π*R_Z*C_Z) = ~1.44 Hz
- High frequency pole location = 1/(2*π*R_Z*C_P) = ~ 68.2 Hz

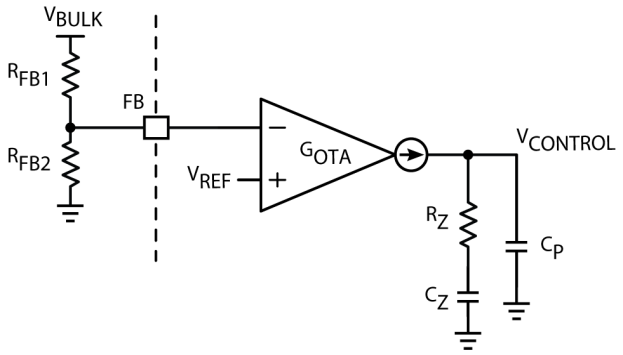


Figure 22. Equivalent Analog Compensator

This compensator provides greater than 50° of phase boost at 2 Hz, over 70° of phase boost between 5 – 10 Hz, and the mid−band gain measures at 13.4 dB. For most PFC applications, having a mid−band gain between 10 – 15 dB will ensure a loop crossover frequency in the range of 5 – 10 Hz, hence the NCP1681 compensator is designed to satisfy a 5 – 10 Hz loop bandwidth with > 60° of phase margin.

Additionally, the $V_{CONTROL}$ voltage is passed through an optional line frequency ripple cancellation circuit which is designed to eliminate the AC ripple present on the $V_{CONTROL}$ voltage. High amplitude AC ripple on the control voltage can increase harmonic distortion of the AC line current, hence the desire to eliminate this ripple component. However, a side effect of the ripple cancellation circuit is that it behaves as another filter in the control loop, degrading the phase boost provided by the compensator. Figure 23 provides a Bode plot of the transfer function from *FB* to V_{REGUL} including the effects of sampling, compensation, and ripple cancellation. The overall compensation loop is optimized for a crossover point of ~ 5 Hz where 60° phase margin can be achieved, and bandwidths up to ~ 14 Hz can be designed with an acceptable 45° phase margin.

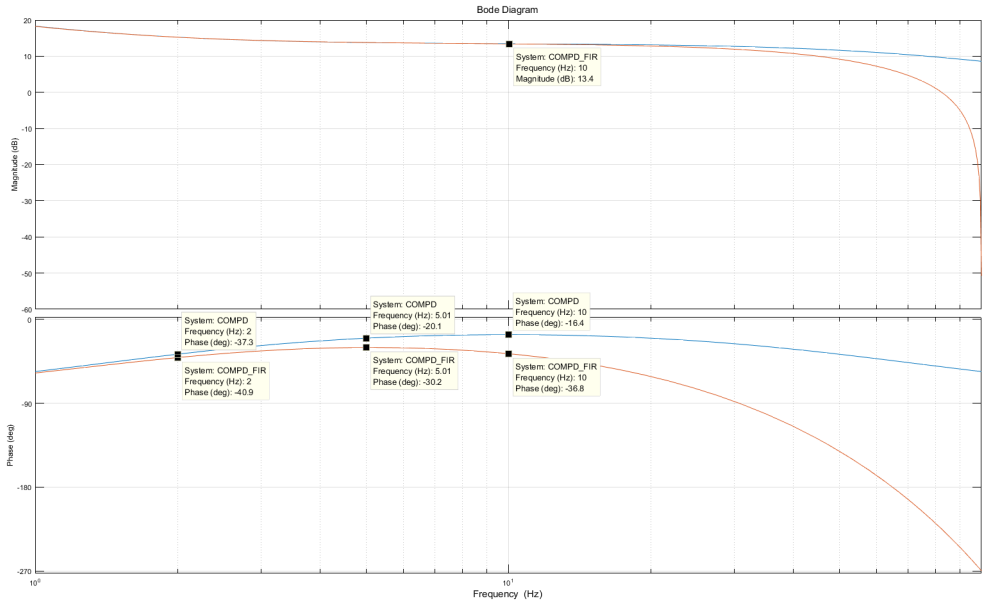


Figure 23. Bode Plots with Ripple Cancellation Filter

Output Voltage Protection Features

The NCP1681 features multiple protection and enhancement features for improved performance and robustness of the application. The soft OVP, UVP and DRE comparators monitor the sampled FB pin voltage. Based on the typical value of their parameters and if ($V_{out,nom}$) is the output voltage nominal value (e.g., 395 V), we can deduce the following levels:

- Output Regulation Level:

$$V_{out,nom} = \frac{V_{REF}}{k_{FB}}$$

- Output soft OVP Level:

$$V_{out,SOVP} = 105\% \cdot V_{out,nom}$$

- Output Fast OVP Level:

$$V_{out,FOVP} = 108\% \cdot V_{out,nom}$$

- Output UVP Level:

$$V_{out,UVP} = 12\% \cdot V_{out,nom}$$

- Output DRE Level:

$$V_{out,DRE} = 95.5\% \cdot V_{out,nom}$$

- Output BUV Level:

$$V_{out,BUV} = \frac{V_{BUV}}{V_{REF}} \cdot Vout, nom = 80\% \cdot V_{out,nom}$$

- Output Upper Soft−SKIP Level:

$$\left(V_{out,softSKIP}\right)_H = V_{out,nom}$$

- Output Lower Soft−SKIP Level:

$$\left(V_{out,softSKIP}\right)_L = 94\% \cdot V_{out,nom}$$

V_{REF} is the regulation reference (2.5 V typically) and R_{FB1} and R_{FB2} are the feedback resistors per Figure 21; k_{FB} is the scale down factor of the feedback resistors

$$\left(k_{FB} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}}\right).$$

V_{BUV} is the internal threshold for the bulk under−voltage protection (BUV). Its typical value is 2 V. The BUV protection thus typically trips when the output voltage drops to 80% of its nominal level.

$(V_{out,softSKIP})_H$ and $(V_{out,softSKIP})_L$ are the levels between which the output voltage swings when in soft−SKIP mode (see the “Soft−SKIP Mode” section).

The soft−OVP trips when the feedback voltage exceeds 105% of V_{REF} and remains in this mode until V_{FB} drops below 103% of V_{REF}. When the soft−OVP trips, it reduces the power delivery down to zero in 4 steps as shown in Figure 24.

- Step 1: V_{REGUL} drops to 75% of the $V_{CONTROL}$ value for 400 μs
- Step 2: V_{REGUL} drops to 50% of the $V_{CONTROL}$ value for 400 μs
- Step 3: V_{REGUL} drops to 25% of the $V_{CONTROL}$ value for 400 μs
- Step 4: V_{REGUL} drops to 0 until the soft−OVP fault is over, that is, when the output voltage drops below 103% of its regulation level.

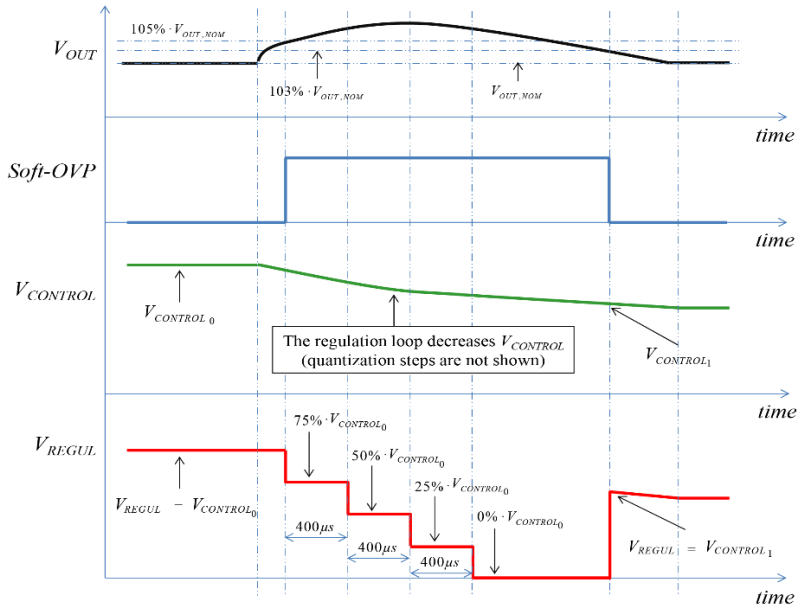


Figure 24. Soft−OVP Timing Diagram

The fast OVP comparator is analog and directly monitors the feedback pin voltage for immediate blanking of the drive pulses. The Fast OVP comparator trips when the feedback voltage exceeds 108% of V_{REF} and does not allow drive pulses until the feedback voltage falls below 103% of V_{REF}.

The dynamic response enhancer circuit functions to firmly contain undershoot of the output by increasing the gain of the control loop in response to the bulk voltage falling below a percentage of the desired regulation voltage. Practically when the FB pin voltage falls below 95.5% of V_{REF}, the DRE speeds up the charge of the compensation network until the FB pin voltage exceeds 98% of V_{REF}.

The FB pin also features a small 250−nA sink current for protection against an open FB pin, in which case V_{FB} will be pulled below the V_{UVP} (300 mV typically) threshold tripping the UVP protection. The UVP feature further works as a protection in the case of a FB pin that is shorted to GND.

Auxiliary Winding and Valley Detection Block

The TPFC topology presents a unique challenge to the use of an auxiliary winding for valley detection in FCCrM. Unlike the classical bridged CrM boost PFC, the TPFC operates differently in the positive and negative AC line cycles. The PWM−controlled switch changes from the low side switch to the high side switch, the inductor current changes from 1st to 3rd quadrant operation, and the “valley” of the switch node does not always occur when the auxiliary winding voltage approaches zero. Specifically, in negative half line cycle, the “valley” is really a peak and the desired turn−on of the PWM switch occurs when the switch node voltage is approaching the bulk voltage. This is illustrated in Figure 25 where the switch node voltage is depicted in both positive and negative half line cycles.

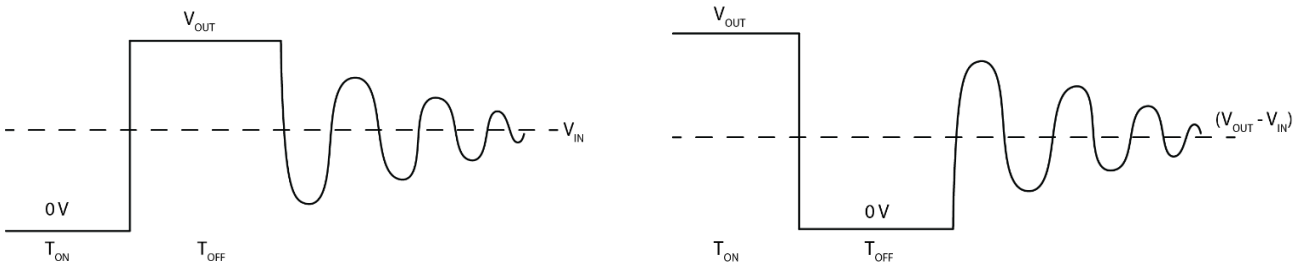


Figure 25. Switch Node Voltage in Positive (left) and Negative (right) Half Line Cycles

To adapt to the changing operation of the TPFC, while maintaining the use of a single low−cost auxiliary winding, the NCP1681 implements a novel “valley” sensing scheme combining edge detection with threshold detection. The NCP1681 accomplishes this by changing the “Arming” and “Triggering” thresholds depending on the polarity of the AC line. During positive half line cycle, the valley detection arms when the aux voltage goes above 200 mV, and triggers when the aux voltage falls below 100 mV. During negative half line cycle the opposite occurs, namely the valley detection arms when the aux voltage goes below 100 mV and triggers when the aux voltage comes back above 200 mV. By reusing the same comparators and thresholds, and only changing the function of the thresholds, the NCP1681 effectively combines edge and threshold detection to achieve a robust, low−cost solution that overcomes the bidirectional operation of the TPFC.

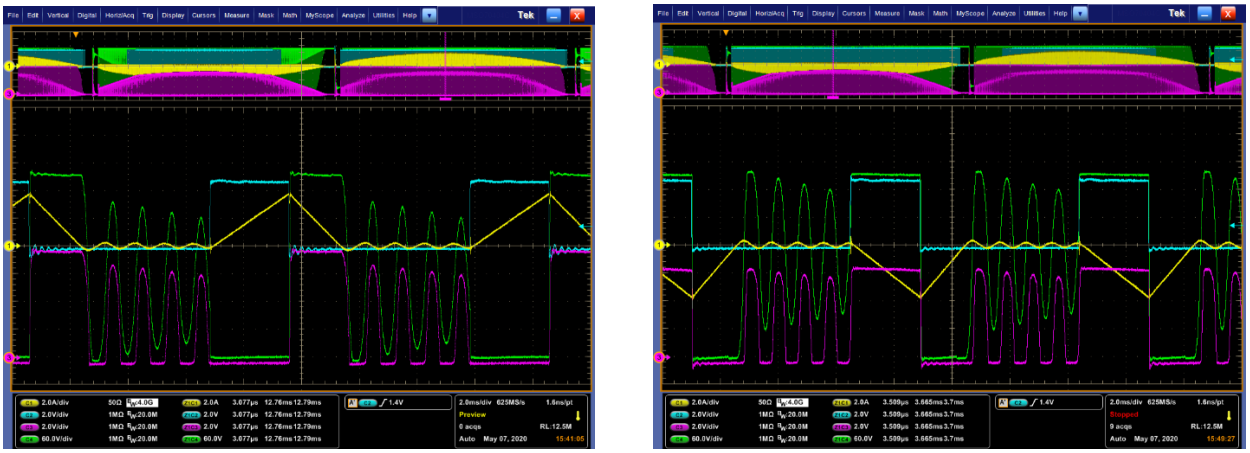


Figure 26. Valley Detection in DCM. Positive Line Cycle on Left, Negative on Right

Figure 26 shows waveforms demonstrating the valley detection implementation of the NCP1681 in DCM operation. The waveforms show the switch node voltage (Ch.4) and the auxiliary winding voltage (Ch.3) as its image traversing through 5 valleys before the respective PWM signal sets high. In both positive and negative half line cycle the turn on occurs on the correct edge of the auxiliary winding voltage.

Figure 27 is an example of valley detection in CrM operation. The switch node voltage is again shown on channel 4 and although there is no image of the auxiliary winding voltage, it can be seen that the turn−on of the PWML (Ch.2) on the left, and PWMH (Ch.3) on the right are coordinated to the “valley” of the switch node enabling very low turn−on voltage for optimized efficiency.

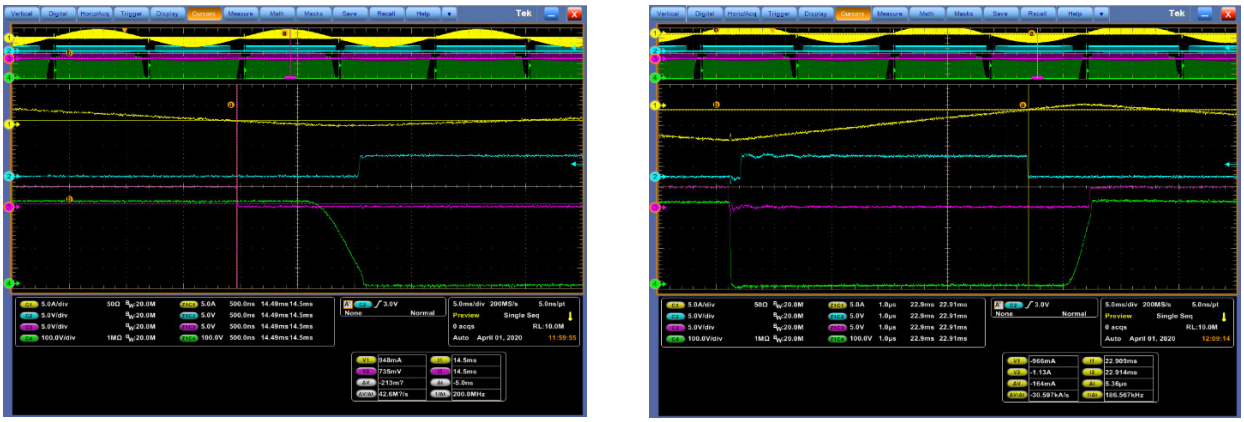


Figure 27. Valley Detection in CrM. Positive Half Line Cycle on Left, Negative on Right

The recommended auxiliary winding connection is shown in Figure 28. To optimize the symmetry of the valley detection between positive and negative half line cycles, a resistance, R_{AUX1}, with no series blocking diode is recommended between the auxiliary winding and the AUX pin. A pulldown resistance at the pin, R_{AUX2}, helps divert current to ground when the auxiliary winding voltage swings high, reducing the current into the ESD protection of the valley detect circuit. A Schottky diode, D_{AUX}, is recommended to protect the AUX pin voltage from going too far below ground when the auxiliary winding voltage goes negative. Finally, a capacitor to ground, C_{AUX}, can be used to tune the valley detection for optimizing valley switching and efficiency in the fast leg.

It should be noted that the AUX winding detection is only needed for multi−mode operation. For the NCP1681Ax which employs only CCM operation, the AUX pin should be connected directly to ground.

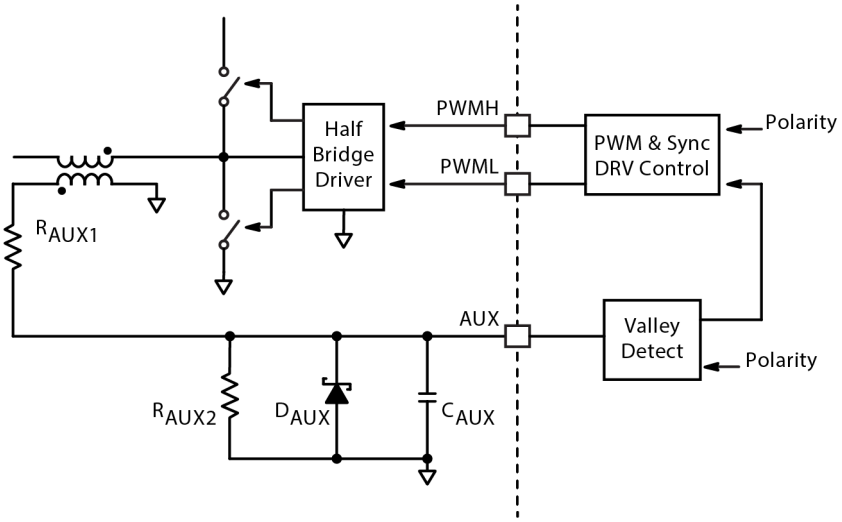


Figure 28. Recommended Auxiliary Winding Circuit

Inductor Current Sensing

In CCM the NCP1681 implements predictive current mode control that requires the controller to receive an accurately sensed image of the inductor current. This is a challenge with the TPFC topology because the inductor and each of the fast leg switches conduct current bidirectionally, as shown in Figure 29. Depending on the line cycle polarity, the inductor current flows in either the 1st or 3rd quadrant while the duty−controlled fast leg device conducts current from drain to source, and the (1−d) fast leg device conducts current from source to drain.

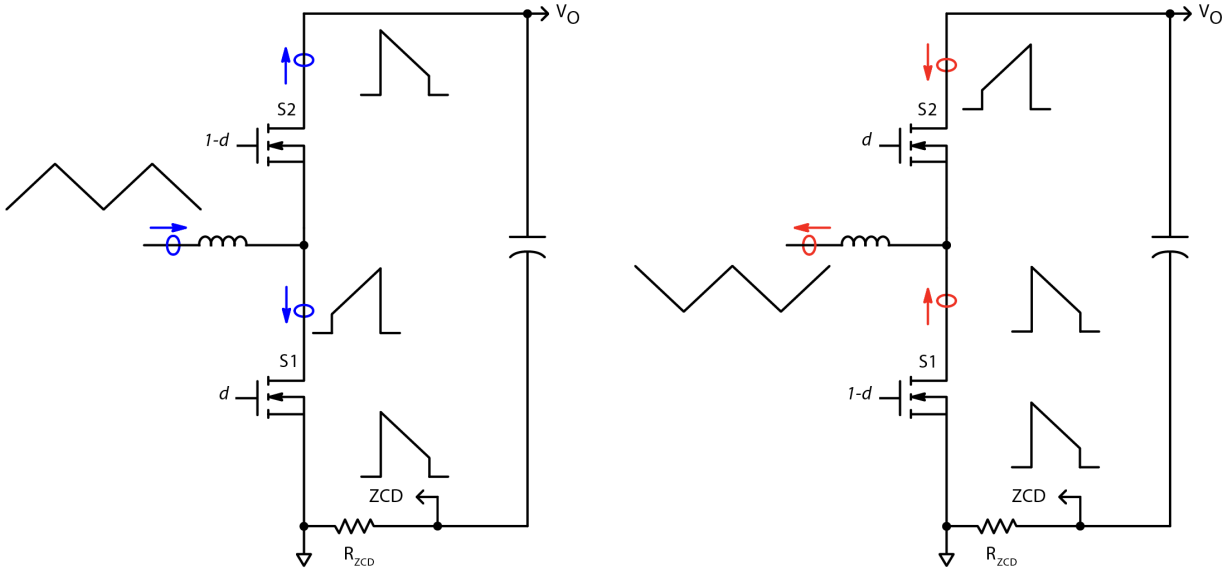


Figure 29. Current Flow in Positive and Negative Half Line Cycles

The NCP1681 incorporates a novel current sensing scheme utilizing two inputs – one for sensing inductor current during the duty−controlled portion of the switching cycle and one for sensing inductor current during the (1−d) portion of the switching cycle. These two signals are summed together inside the controller to reconstruct an image of the inductor current. The current sense configuration used in a typical application is illustrated in Figure 30.

Current Sense (CS) Input

The CS input senses the inductor current during the duty−controlled portion of the switching cycle. This can be referred to as the inductor current upslope. The recommended scheme for the CS input requires two current sense transformers (CTs), one in series with each of the fast leg switches, a diode OR'ed output from the CT secondaries, a single current sense resistor, and an RC filter to mitigate noise pickup on the sense circuit. Additionally, a "blanking" circuit is needed across each secondary to selectively shunt the CT output to ground.

Current Transformer Blanking Circuits

Each of the CTs is active during the half line cycle when the respective switch is duty controlled. When the respective switch is (1−d) controlled then the blanking circuit is active, and the CT secondary is shunted to ground. In Figure 30 the blanking circuits are shown as generic blocks with 3 ports as there are different discrete circuit implementations that will meet the operational requirements for these blanking circuits. The CT is active when current flows drain to source in the respective switch. During this portion of the switching cycle current flows out of the secondary dot, into the anode of the diode and eventually through the current sense resistor. To avoid disrupting the CS signal the blanking circuit must block voltage across ports A−B shown in Figure 30, parallel to the CT secondary winding, but the breakdown voltage that must be held off is just a diode drop above the current sense limit.

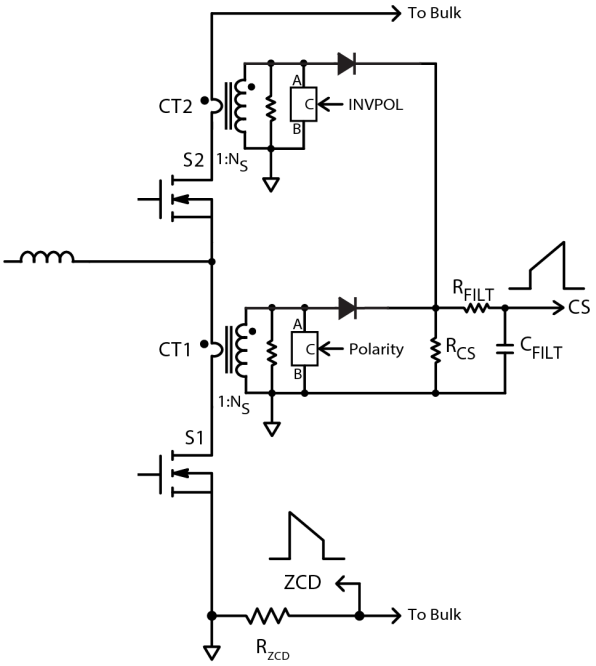


Figure 30. NCP1681 Current Sensing Scheme

When the CT is active it develops magnetizing current during the duty portion of the switching cycle that must then be reset during the (1−d) period. During the (1−d) period the magnetizing current in the secondary flows through the reset resistor and appears at the secondary dot as a negative voltage with respect to ground. The blanking circuit is then required to block the reset voltage across ports B−A. The two secondary diodes used in the ORing circuit and the blanking circuit have a minimum breakdown voltage equal to this reset voltage.

The blanking circuit is required to be active/conducting whenever the primary current is flowing in the direction of source to drain. In this case the secondary side current would be flowing into the dot, hence the blanking circuit must be able to conduct current across ports B−A to successfully short the secondary. The current carrying capability should match the capability of the diodes and the effective impedance across port B−A should be an order of magnitude lower than the current sense resistor to ensure that the secondary can be shorted without generating substantial magnetizing current.

The blanking circuit also requires a control port to switch the circuit between its conducting and non−conducting state. The circuit will switch at a frequency equal to the AC line frequency and the NCP1681 features two outputs, Polarity and Inverted Polarity (INVPOL), which can be used to drive the control port. A circuit configuration that features all the necessary requirements is shown in Figure 31. This configuration consisting of two PMOS transistors with a common source/cathode connection can block voltage bidirectionally and conduct current bidirectionally, behaving much like an ideal switch. The control port requires a capacitive charge pump for driving the PMOS transistors, and the drive logic for this circuit is inverting, meaning that the blanking circuit is conducting when the POL/INVPOL signal is low and non−conducting when POL/INVPOL signal is high.

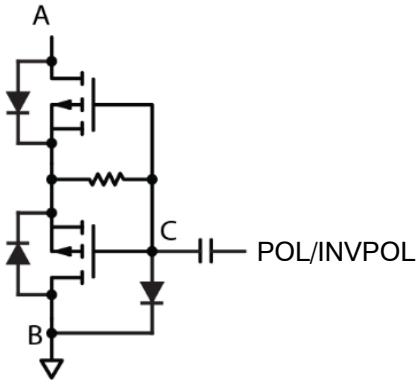


Figure 31. CT Blanking Circuit

Overload and Peak Current Limit Protection

The CS pin is also utilized for cycle−by−cycle peak current limiting and overload protection. This function helps protect the application from destructive damage due to inductor saturation, output power overload, or thermal overstress, by immediately terminating the duty−controlled drive pulse when the peak current limit threshold is reached.

To calculate the CS resistor value needed for peak current limiting, one must first calculate the maximum peak inductor current in the application using Equation 7 where P_O is output power, η is efficiency, V_{AC} is the RMS input voltage, L is the inductance of the boost choke, F_{SW} is the CCM switching frequency, and D_{PK} is duty cycle at the peak AC line voltage. Once the maximum peak current is determined, Equation 8 is used to find an upper limit on the CS resistor based on the CS current limit threshold, $V_{ILIMIT(xL)}$, and the turns ratio of the current sense transformers. This calculation should be done at the minimum AC input voltage, usually 90 V_{AC}, and may also need to be repeated at the minimum high line voltage in the application, typically 180 V_{AC}, depending on the application's output power requirements.

The NCP1681Ax utilizes a 1 V current limit threshold in both low line and high line to accommodate applications that may require more output power capability at high line when compared to low line. The NCP1681Bx has a low line peak current threshold of 1.4 V and implements a 60% reduction of the current limit at high line, as the multi−mode version of the device is more likely to be utilized in applications that have a consistent power output requirement at all line voltages. If the calculation is needed at both low and high line, the user should choose the lower of the two calculated values.

$$I_{L,PK} = \frac{\sqrt{2} \cdot P_O}{\eta \cdot V_{ac}} + \frac{\sqrt{2} \cdot V_{ac} \cdot D_{PK}}{2 \cdot L \cdot F_{SW}} \quad \text{(eq. 7)}$$

$$R_{CS} < N_S \cdot \frac{V_{ILIMIT(xL)}}{I_{L,PK}} \quad \text{(eq. 8)}$$

THD Enhancer

Another feature of the NCP1681 that is derived from the CS voltage is the THD enhancer, which produces a small on−time extension proportional to the time duration that the CS voltage is less than the $V_{CS(MIN)}$ threshold. This is shown in Figure 32 where the orange block represents the time duration that the THD enhancer integrates to produce an on−time extension. Typically, at lighter loads and near the AC zero crossings the amplitude of the inductor current reduces, and the CS voltage will spend longer durations below this minimum threshold resulting in larger on−time extensions. Note that the THD enhancer feature is only actively utilized for on−time control in CrM/DCM, hence this feature is only active in the NCP1681Bx version of the device. The THD enhancer working in conjunction with the dead time compensation circuit allows the NCP1681Bx to optimize THD performance across line and load.

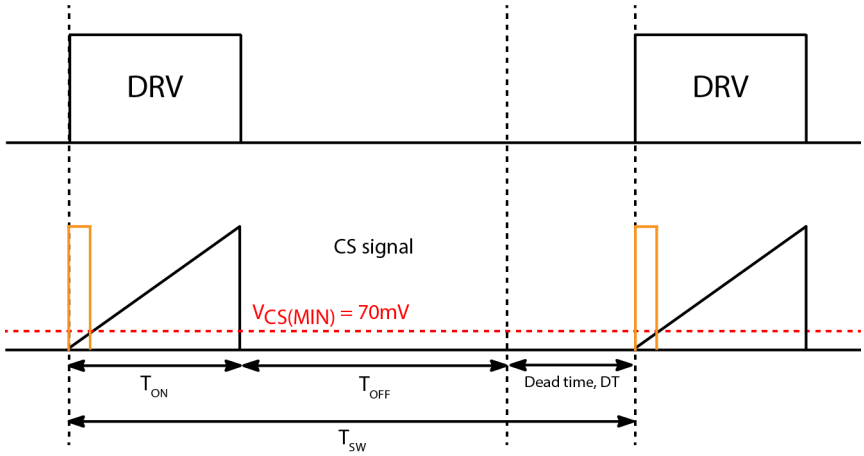


Figure 32. THD Enhancer Diagram

Current Sense Open/Short Protection

The CS pin is critical for performance and robustness of the application so it is necessary to ensure an active sensing circuit is present and the CS pin has not been left open or accidentally shorted to ground as this would inhibit the ability of the NCP1681 to provide protection against overload or inductor saturation.

To protect against an open CS pin, the NCP1681 features an internal 1 μA pull−up current and a second level current limit comparator. The second level current limit threshold is nominally 1.5 times that of the peak current limit threshold. If the CS pin is open the pull−up current source pulls the pin voltage above the comparator threshold causing the drive pulse to terminate. Following a trip of the second level comparator the controller also implements an overstress timer, typically 800 μs, before initiating a new drive pulse. The overstress timer is beneficial for limiting thermal stress in case the second level comparator trips due to a failed transistor in the fast leg. If the second level comparator is tripped on 4 consecutive switching cycles, then the controller shuts off all drive pulses and requires a complete power−on reset before allowing more drive pulses.

To protect against a CS pin that may be shorted to ground, the NCP1681 employs a one−time impedance check of the external circuitry connected to the pin. Specifically, the controller outputs a 230 μA test current out of the CS pin during the prestart phase when the controller is awaiting the line frequency monitor to clear 4 consecutive AC line cycles within the timing threshold. The 230 μA test current should flow through the filter resistor, R_{FILT}, which interfaces the current sense resistor to the CS pin. The controller measures the minimum voltage generated externally and inhibits operation if the voltage is less than 150 mV. To meet this requirement, it is recommended that R_{FILT} have a minimum resistance of 1 kΩ. The recommended time constant for the filter is 50 – 150 ns.

Zero Current Detection (ZCD) Input

The ZCD input senses the inductor current during the (1−d) portion of the switching cycle. This can be referred to as the inductor current downslope or demagnetization. The recommended sensing element for the ZCD input is either a high power, low inductance, current sense resistor; or a current transformer circuit like what is used for inductor upslope detection. For ZCD the CT circuit does not require a blanking mechanism because the current through the ZCD sensing element is unidirectional and the CT remains active. Figure 33 shows the two recommended sense circuit configurations.

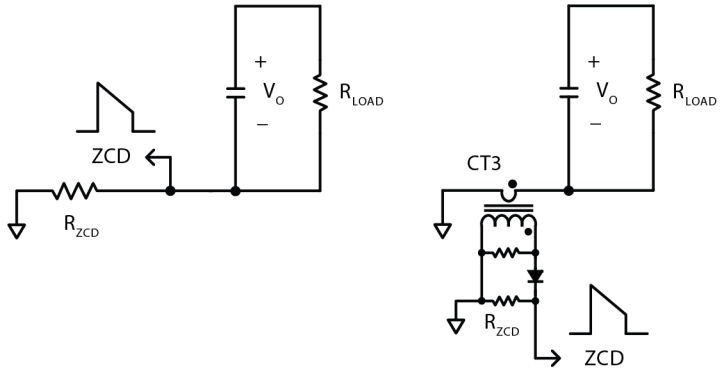


Figure 33. ZCD Sense Circuits

ZCD Resistor Calculation

The NCP1681 takes the CS and ZCD inputs and sums them together to provide the internal multiplier with a signal representative of the inductor current. This inductor current signal is critical to optimizing THD performance in the application and therefore the relative signal amplitude of these two inputs should be approximately equal.

If the ZCD sensing element is a high−power current sense resistor then Equation 9 should be used to calculate the resistor value that ensures equal signal amplitude between the CS and ZCD inputs. In case that the application designer chooses a CT circuit for the ZCD input then the value for R_{ZCD} and the number of turns for CT3 should be identical to what is used for the CS sensing circuitry. Like the CS input, additional RC filtering is recommended at the ZCD input to mitigate noise pickup from switching events. It is recommended that the filter values at the ZCD input match the R_{FILT} and C_{FILT} values used for CS.

$$R_{ZCD} = \frac{R_{CS}}{N_S} \qquad \text{(eq. 9)}$$

Synchronous PWM Drive Control

The synchronous PWM or (1−d) device in the TPFC topology enables higher efficiency performance but proper gating of the device is necessary for optimizing efficiency and ensuring robustness in the application. A diagram of the sync control methodology is shown in Figure 34. First, the NCP1681 employs a dead time, T_{DT1}, typically 130 ns, following the falling edge of the PWM duty−controlled drive to prevent cross conduction. After the dead time has expired the controller looks for the ZCD voltage to exceed the $V_{ZCD(ARM)}$ threshold to enable the sync drive. In lighter loads, the ZCD voltage may never exceed this $V_{ZCD(ARM)}$ threshold, and the sync device will never enable. This is done to prevent switching of the sync device at light loads where the associated switching losses could negatively impact the overall efficiency of the application.

At increasing loads, the ZCD voltage will exceed the arming threshold and the sync drive will remain enabled until the ZCD falls below the $V_{ZCD(TRIG)}$ threshold. The trigger threshold has been set close to 0 to keep the sync conduction period as long as possible but without letting the inductor current reverse polarity. Should the sync device remain on for too long the inductor current would reverse polarity and begin cycling energy from the bulk capacitance. This would lead to increased RMS currents in the system and could diminish overall efficiency.

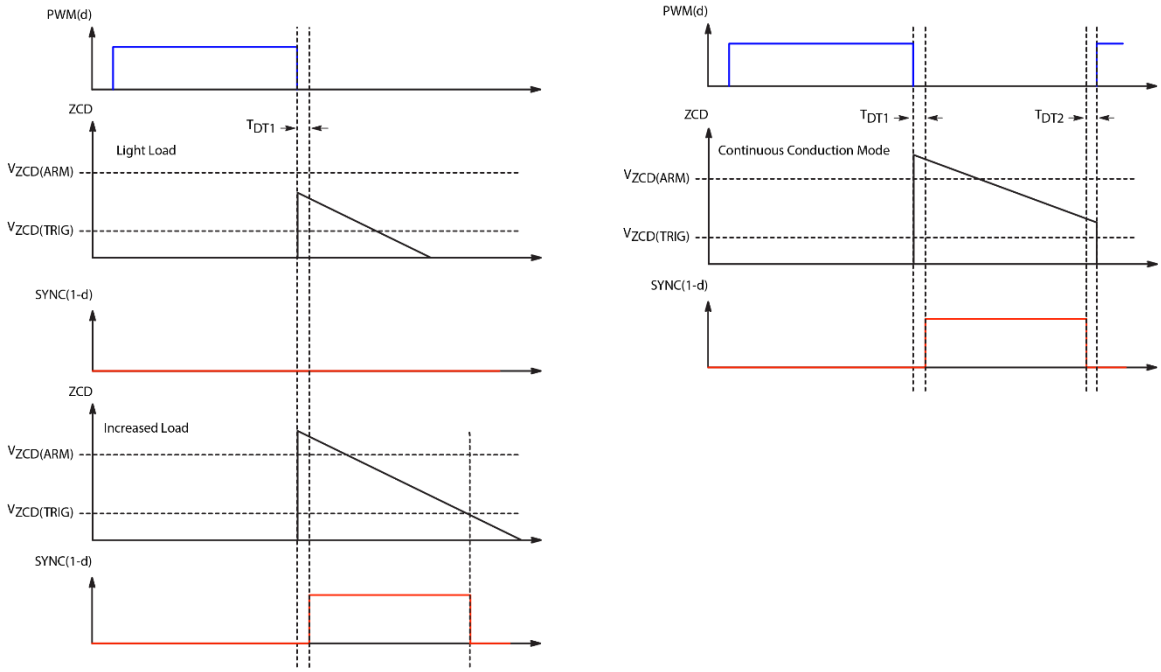


Figure 34. Synchronous PWM Drive Control

In CrM operation it is required that the ZCD voltage fall below the $V_{ZCD(TRIG)}$ threshold before the start of the next PWM drive pulse, but in CCM this may not be the case as the PWM drive pulse is set based on the internal oscillator. Therefore, when the NCP1681 operates in CCM, the device implements an additional dead time, t_{DT2}, which shuts off the sync drive pulse 150 ns prior to the start of a new switching period. This additional dead time feature allows the sync drive to remain high for most of the (1−d) conduction period enabling better system efficiency while still preventing cross conduction of the two switches.

Summarizing, the sync (1−d) pulses are gated by the following criteria:

- A delay, t_{DT1}, of 125 ns (typical) after the PWM(d) turn−off – This prevents cross conduction
- ZCD voltage crosses the $V_{ZCD(ARM)}$ threshold – This ensures sync pulses are enabled only at higher loads for efficiency improvement across all load conditions.
- V_{LINE} voltage crossing 220 mV which is 22 V on the AC line with a 100:1 divider – This avoids premature enabling of the sync pulses and enhances efficiency
- PFCOK sets high – To avoid reverse currents during startup
- In CrM/DCM operation, the sync pulse is terminated by the $V_{ZCD(TRIG)}$ threshold. The device will not allow a new drive PWM pulse if this threshold has not been in crossed.
- In CCM operation there is an additional dead time, t_{DT2}, which terminates the sync pulse 150 ns (typical) before the start of the new switching period if the ZCD voltage remains above the $V_{ZCD(TRIG)}$ threshold.

Skip/Standby Mode

The NCP1681 features a Skip/Standby mode which enables the application to achieve very good no load and light performance. The device must be externally commanded to enter the Skip mode by pulsing of either the PFCOK or V_M pins, however because the V_M pin is used for duty cycle modulation in CCM mode it is highly recommended that the user utilize the PFCOK pin for skip mode control. When the device enters the Skip mode, it sheds much of its functionality except for FB and V_{CC} monitoring, and the internal consumption of the device is reduced to I_{CC4}, typically 540 μA. While in Skip mode the output voltage decays to 94% of the regulation voltage allowing for a long period, sometimes up to 1 minute, of inactivity. When the output voltage reaches 94% of its nominal value, the device exists Skip mode for a brief burst period during which drives are enabled and the output voltage is pushed back up to the nominal regulation value. Provided that the NCP1681 continues to receive Skip command pulses from an external source, the device will continue to operate in this Skip−burst−skip mode indefinitely. A timing diagram of the Skip operation is shown in Figure 35.

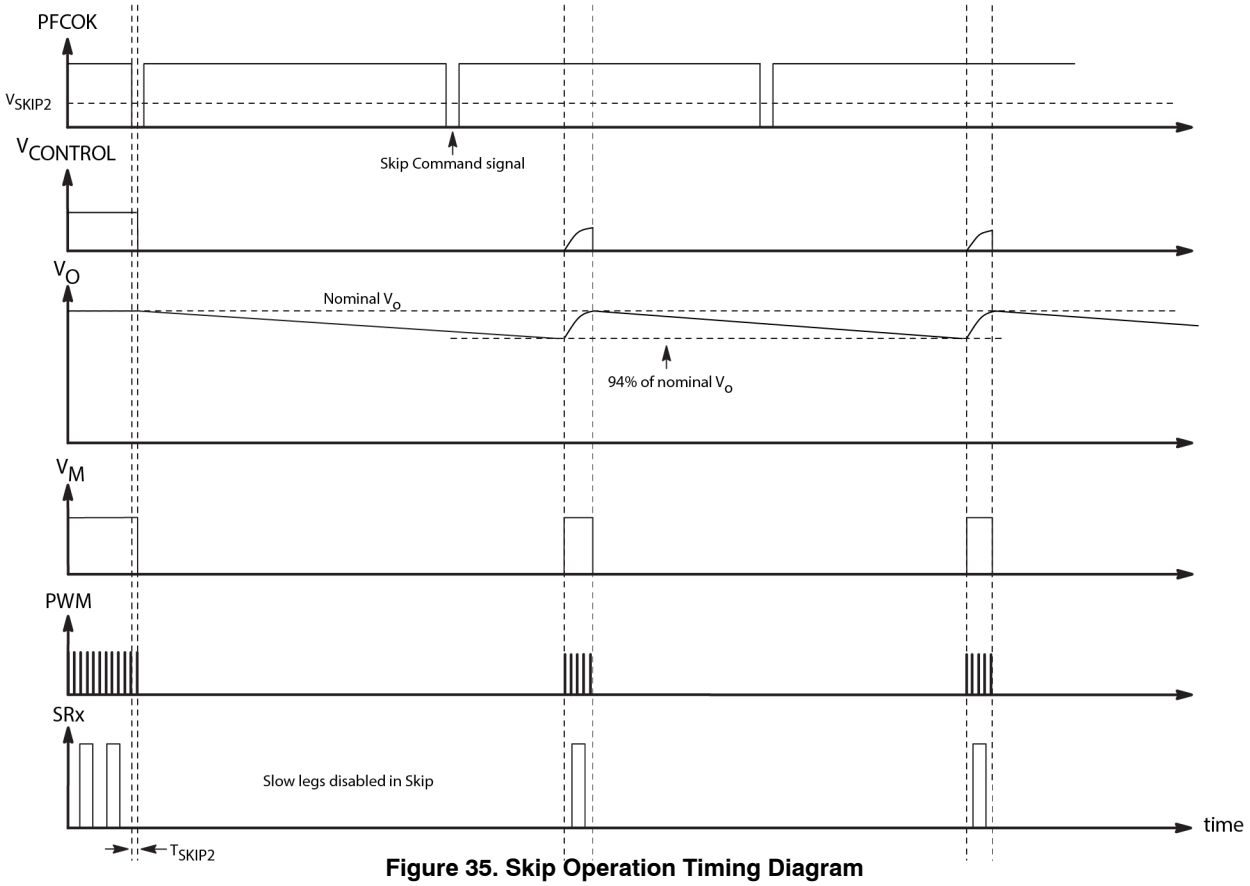


Figure 35. Skip Operation Timing Diagram

Skip Command Pulses

The PFCOK pin is typically utilized for communication to a downstream converter, acting as an enable or UVLO. In this case it may be necessary for the PFCOK pin to remain high during the skip mode so that the downstream converter does not shutdown. For that reason, the command pulse logic for the PFCOK pin is optimized for a pulse train, where the PFCOK pin must be pulled below the $V_{SKIP2(th)}$, typically 0.5 V, for a duration greater than T_{SKIP2}, typically 30 μs. The frequency of the PFCOK pulse train needs to be faster than the burst frequency of the PFC. Figure 36 shows a sample schematic and timing diagram for the interface between the downstream converter and the PFCOK pin of the NCP1681.

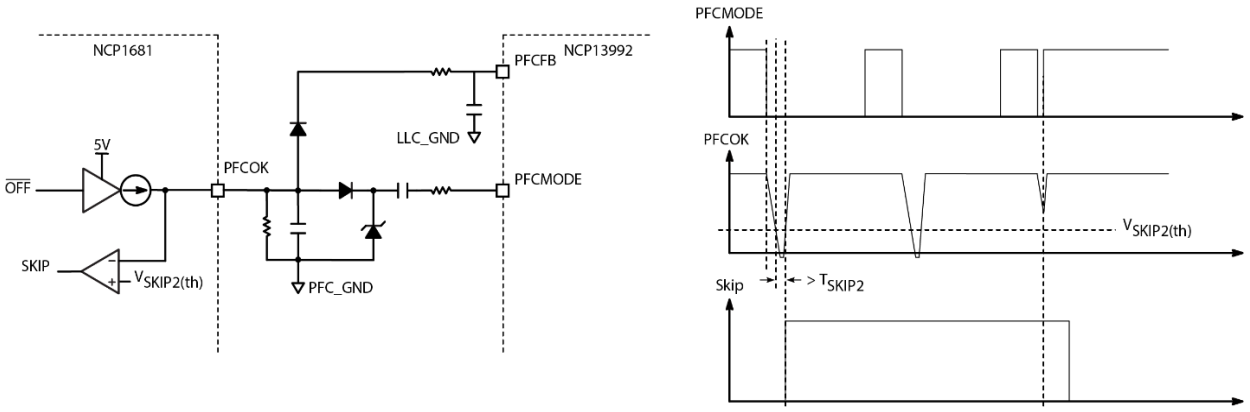


Figure 36. PFCOK Schematic and Timing Diagram

PFCOK Operation

The PFCOK pin is intended to control operation of a downstream DC−DC converter by acting as an enable or UVLO signal. The pin output is high when the application is in nominal operation and low when the application is in startup or when the device detects a fault condition. The output of the pin is a current source proportional to the FB pin voltage with a gain of 10 μA/V. A resistor to ground placed at the pin will give the downstream converter an image of the bulk voltage for use as a UVLO or as a logic enable.

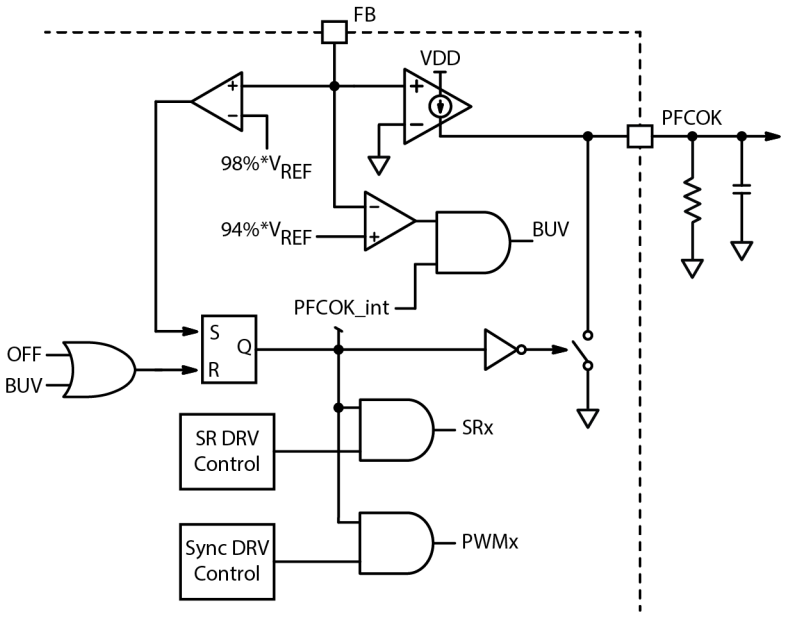


Figure 37. PFCOK Schematic

A logic diagram detailing the PFCOK pin operation is shown in Figure 37. Worth noting is that at startup of the application the PFCOK pin remains pulled to ground until the V_{FB} voltage reaches 98% of V_{REF}. Once the FB voltage exceeds 98% of V_{REF} the internal PFCOK flag goes high which enables the sync PWM and slow leg SR drive pulses. Sync PWM and slow leg SR pulses are also gated by other criteria but prior to achieving regulation, they are completely disabled. The PFCOK flag also gates skip mode operation and the bulk undervoltage (BUV) fault so that the device is unable to enter skip mode or declare a BUV fault until having first achieved regulation.

Fault Pin and Fault Matrix

Fault Pin

The NCP1681 includes a dedicated fault input accessible via the Fault pin. The controller can be latched by pulling the pin up above the upper fault threshold, $V_{FLT(OVP)}$, typically 3.0 V. The controller is disabled if the Fault pin voltage, V_{Fault}, is pulled below the lower fault threshold, $V_{FLT(OTP)}$, typically 0.4 V. The lower threshold is normally used for detecting an overtemperature fault. The controller operates normally while the Fault pin voltage is maintained within the upper and lower fault thresholds. Figure 38 shows the architecture of the Fault input.

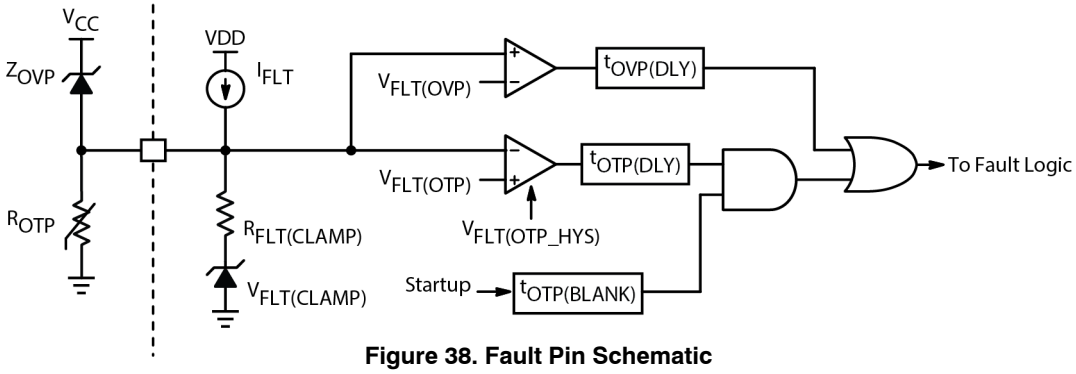


Figure 38. Fault Pin Schematic

The lower fault threshold is intended to be used to detect an overtemperature fault using an NTC thermistor. A pull up current source I_{FLT}, (typically 46 μA) generates a voltage drop across the thermistor. The resistance of the NTC thermistor decreases at higher temperatures resulting in a lower voltage across the thermistor. The controller detects a fault once the thermistor voltage drops below $V_{FLT(OTP)}$. The OTP fault is an auto−recoverable fault so the NCP1681 will enable switching once the fault pin voltage exceeds the $V_{FLT(REC)}$ threshold, typically 0.92 V. The OTP fault also includes a 5 ms blanking circuit, $t_{OTP(BLANK)}$, which prevents the OTP fault from being asserted when the device first powers up. The blanking period is needed to allow any external pin capacitance to be charged up above the OTP threshold.

A clamp circuit prevents the Fault pin voltage from reaching the upper latch threshold if the pin is left open. To reach the upper threshold, the external pull−up current must be higher than the pull−down capability of the clamp (set by $R_{FLT(CLAMP)}$ at $V_{FLT(CLAMP)}$. The upper fault threshold can be used for V_{CC} over−voltage protection in the application, particularly for protecting external gate drivers. The NCP1681 V_{CC} pin is rated for 30 V, however external devices used to drive either the fast of slow leg transistors often have V_{CC} pins rated only up to 20 V so a simple Zener diode connected between VCC and the FAULT pin can protect those external devices. The controller is latched once V_{Fault} exceeds $V_{FLT(OVP)}$. Both of the Fault signals include internal filtering to prevent noise from triggering the fault detectors. Upper and lower fault detector blanking delays, $t_{OVP(DLY)}$ and $t_{OTP(DLY)}$ are both typically 30 μs. A fault is detected if the fault condition is asserted for a period longer than the blanking delay. Some external capacitance is also recommended at the FAULT pin to provide additional noise immunity.

Fault Matrix

The NCP1681 has an extensive suite of fault handling capabilities designed to enable a robust application design utilizing the Totem Pole PFC topology. Although much of the fault handling has been described in some detail throughout the datasheet, Table 6 is provided as a Fault Handling Matrix summarizing the key protection features including the conditions needed to set the fault, reset the fault, and the specific action taken by the controller for the given fault.

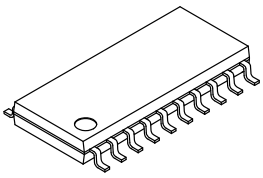
Table 6. NCP1681 FAULT HANDLING MATRIX

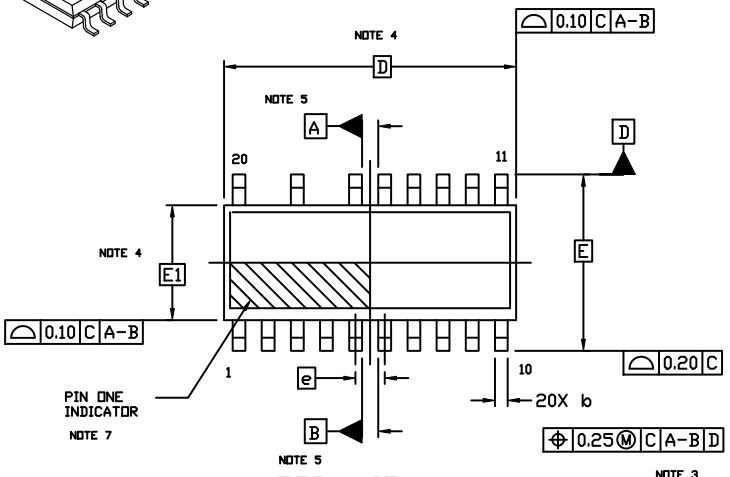
Fault	Set	Reset	Controller Action
Line SAG	(V_{LINE} < $V_{BO(STOP)}$) + $t_{SAG(blank)}$ expires	V_{LINE} > $V_{BO(START)}$	– Begin soft stop sequence – PWM and SR drives disabled after soft stop – PFCOK pulled low if StaticOVP or BUV (OFF Mode) – Cancels T_{BUV}
BO Fault	(V_{LINE} < $V_{BO(STOP)}$) + $t_{BO(blank)}$ expires	V_{LINE} > $V_{BO(START)}$	– Resets Controller – Polarity signal disabled – PFCOK pulled low if StaticOVP (OFF Mode)
Line Frequency1	t_{LINE} < $t_{LINE(45)}$ or > $t_{LINE(65)}$	$t_{LINE(45)}$ < t_{LINE} < $t_{LINE(65)}$	– SR drives disabled – Starts $t_{LINEFREQ(DLY)}$ timer
Line Frequency2	$t_{LINEFREQ(DLY)}$ timer expires	N_{DRV_EN} = 4: $t_{LINE(45)}$ < t_{LINE} < $t_{LINE(65)}$ for 4 consecutive polarity toggles	– PWM Drive disables – Polarity signal remains active – PFCOK pulled low (OFF Mode)
UVP	V_{FB} < V_{UVP}	V_{FB} > V_{UVP} + $V_{UVP(HYS)}$	– PWM and SR drives disabled – Polarity signal remains active – PFCOK pulled low (OFF Mode)
Bulk Under−Voltage (BUV)	PFCOK high & (V_{FB} < V_{BUV})	T_{BUV} expires	– PWM and SR drives disabled – Polarity signal remains active – PFCOK pulled low (OFF Mode) – Automatic restart after T_{BUV}
Soft OVP	V_{FB} > $V_{softOVP}$	V_{FB} < $V_{OVPrecover}$	– Begin soft OVP sequence – PWM Drive disables after soft OVP sequence – Polarity & SR remain active
Hard OVP	V_{FB} > $V_{hardOVP}$	V_{FB} < $V_{OVPrecover}$	– PWM Drive disables immediately – Polarity & SR remain active
Over−Current Protection (OCP)	V_{CS} > $V_{ILIMIT1(xL)}$	Cycle−by−Cycle, No Reset Required	– PWM Drive terminates immediately – Polarity & SR remain active
Abnormal/Short Circuit Protection (SCP)	V_{CS} > $V_{ILIMIT2}$	Cycle−by−Cycle, No Reset Required	– PWM Drive terminates immediately – New PWM delayed for $T_{WDG(OS)}$ – Polarity & SR remain active
$N_{CS(LIM2)}$	$N_{CS(LIM2)}$ > 4	Master Reset	– PWM and SR drives disabled – Polarity signal remains active – PFCOK pulled low (OFF Mode)
CS Short to GND	V_{CS} < $V_{CS(TEST)}$	Master Reset	– PWM Drive disables – Polarity signal remains active – PFCOK pulled low (OFF Mode)
Open PGND	V_{PGND} > $V_{CS(TEST)}$	Master Reset	– PWM Drive disables – Polarity signal remains active – PFCOK pulled low (OFF Mode)
V_{CC} UVLO	V_{CC} < $V_{CC(OFF)}$	V_{CC} > $V_{CC(ON)}$	– PWM and SR drives disabled – Polarity signal disabled – PFCOK pulled low (OFF Mode)
Fault OTP	$t_{OTP(BLANK)}$ expires +V_{FLT} < ($V_{FLT(OTP)}$ + $t_{OTP(DLY)}$)	V_{FLT} > $V_{FLT(REC)}$	– PWM and SR drives disabled – Polarity signal remains active – PFCOK pulled low (OFF Mode)
Fault OVP	V_{FLT} > $V_{FLT(OVP)}$ + $t_{OVP(DLY)}$)	Master Reset	– PWM and SR drives disabled – Polarity signal remains active – PFCOK pulled low (OFF Mode)
TSD	T_J > T_{SHDN}	T_J < (T_{SHDN} − $T_{SHDN(HYS)}$)	– PWM and SR drives disabled – Polarity signal remains active – PFCOK pulled low (OFF Mode)

SOIC20 NB LESS PIN 17 & 19

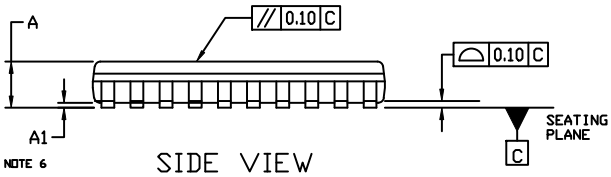
CASE 751EZ
ISSUE O

DATE 23 SEP 2019

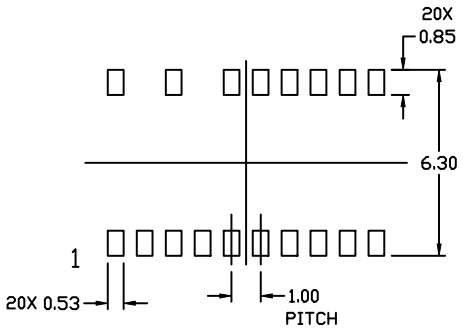




TOP VIEW



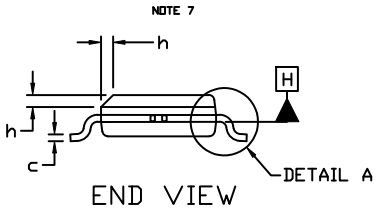
SIDE VIEW



RECOMMENDED
MOUNTING FOOTPRINT

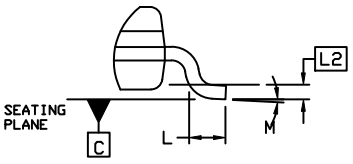
* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 TOTAL IN EXCESS OF "b" DIMENSION. DIMENSION b APPLIES TO THE FLAT PORTION OF THE LEAD AND SHALL BE MEASURED BETWEEN 0.13 AND 0.25 FROM THE TIP.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS BUT DO INCLUDE MOLD MISMATCH. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. CHAMFER FEATURE IS OPTIONAL. IF NOT PRESENT, THEN A PIN ONE IDENTIFIER MUST BE LOCATED IN THIS AREA.



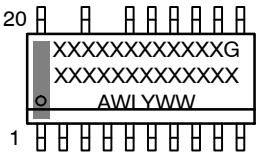
END VIEW

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	---	---	1.70
A1	0.00	---	0.20
b	0.31	0.41	0.51
c	0.10	0.20	0.25
D	9.80	9.90	10.00
E	5.90	6.00	6.10
E1	3.80	3.90	4.00
e	1.00 BSC		
h	0.25	---	0.50
L	0.40	---	0.85
L2	0.25 REF		
M	0°	---	8°



DETAIL A

GENERIC MARKING DIAGRAM*



XXXXX	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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