NCP1588, NCP1589

Low Voltage Synchronous Buck Controller

The NCP158x is a low cost PWM controller designed to operate from a 5 V or 12 V supply. This device is capable of producing an output voltage as low as 0.8 V. This device is capable of converting voltage from as low as 2.5 V. This 10−pin device provides an optimal level of integration to reduce size and cost of the power supply. Features include a 1.5 A gate driver design and an internally set 300 kHz oscillator. In addition to the 1.5 A gate drive capability, other efficiency enhancing features of the gate driver include adaptive non−overlap circuitry. The NCP158x also incorporates an externally compensated error amplifier. Protection features include programmable short circuit protection and undervoltage lockout (UVLO).

Features

- V_{CC} Range from 4.5 to 13.2 V
- 300 kHz Internal Oscillator
- Boost Pin Operates to 26.4 V
- Voltage Mode PWM Control
- Precision 0.8 V Internal Reference
- Adjustable Output Voltage
- Internal 1.5 A Gate Drivers
- 80% Max Duty Cycle
- Input Under Voltage Lockout
- Programmable Current Limit
- This is a Pb−Free Device

Applications

- Graphics Cards
- Desktop Computers
- Servers / Networking
- DSP & FPGA Power Supply
- DC−DC Regulator Modules

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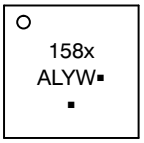
MARKING DIAGRAMS

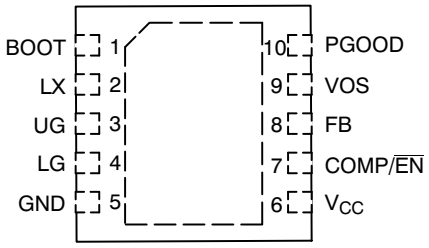
DFN10
CASE 485C



158x	= Specific Device Code
x	= 8 or 9
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Device

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP1588MTR2G	DFN10 (Pb−Free)	3000/Tape & Reel
NCP1589MNTZG	DFN10 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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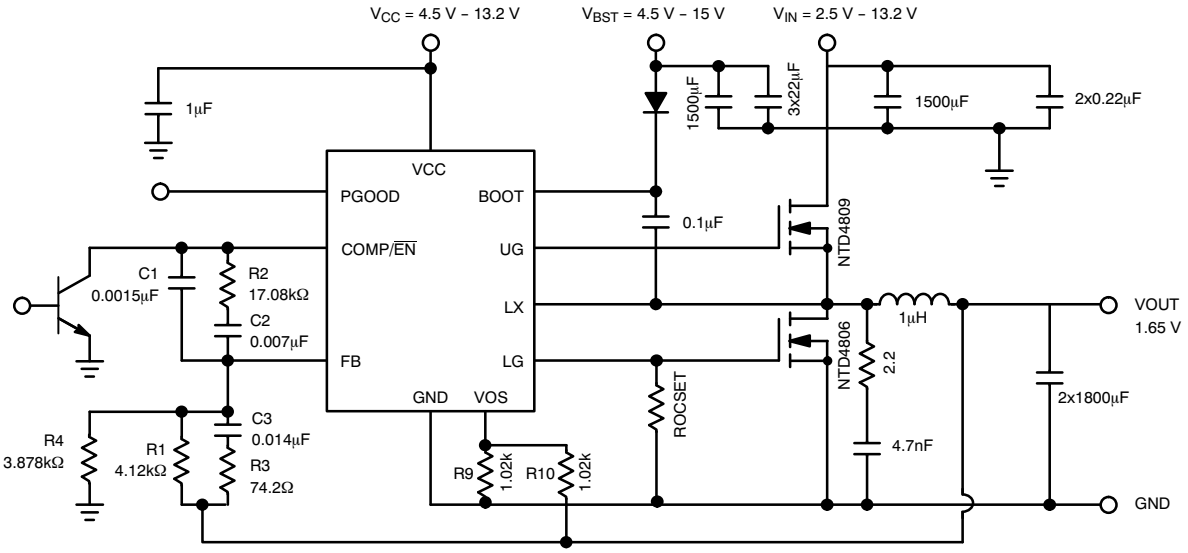


Figure 1. Typical Application Diagram

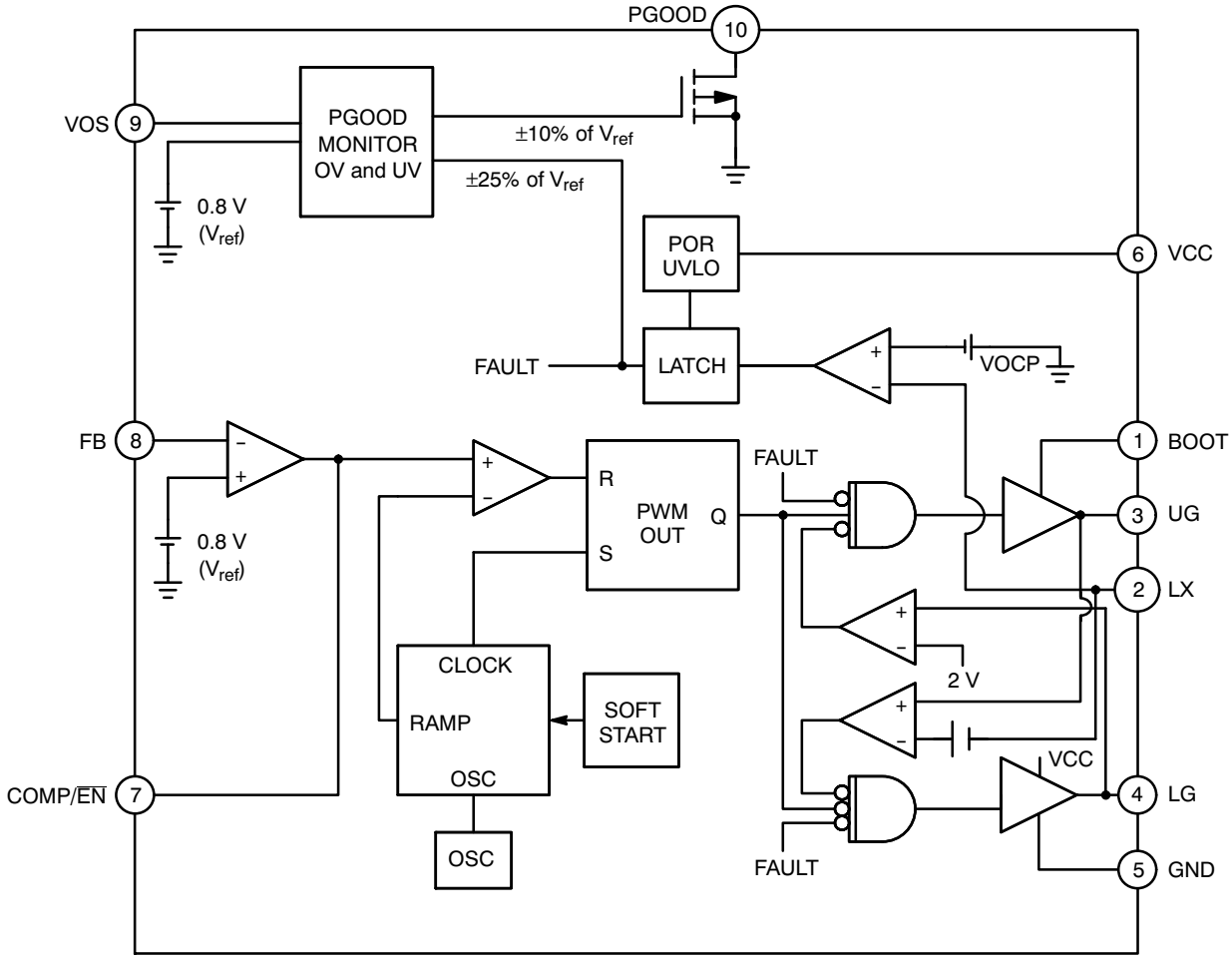


Figure 2. Detailed Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Description
1	BOOT	Supply rail for the floating top gate driver. To form a boost circuit, use an external diode to bring the desired input voltage to this pin (cathode connected to BOOT pin). Connect a capacitor (C_{BOOT}) between this pin and the LX pin. Typical values for C_{BOOT} range from 0.1 μF to 1 μF. Ensure that C_{BOOT} is placed near the IC.
2	LX	Switch node pin. This is the reference for the floating top gate driver. Connect this pin to the source of the top MOSFET.
3	UG	Top gate MOSFET driver pin. Connect this pin to the gate of the top N−channel MOSFET.
4	LG	Bottom gate MOSFET driver pin. Connect this pin to the gate of the bottom N−channel MOSFET.
5	GND	IC ground reference. All control circuits are referenced to this pin.
6	V_{CC}	Supply rail for the internal circuitry. Operating supply range is 4.5 V to 13.2 V. Decouple with a 1 μF capacitor to GND. Ensure that this decoupling capacitor is placed near the IC.
7	COMP/$\overline{EN}$	Compensation Pin. This is the output of the error amplifier (EA) and the non−inverting input of the PWM comparator. Use this pin in conjunction with the FB pin to compensate the voltage−control feedback loop. Pull this pin low for disable.
8	FB	This pin is the inverting input to the error amplifier. Use this pin in conjunction with the COMP pin to compensate the voltage−control feedback loop. Connect this pin to the output resistor divider (if used) or directly to V_{out}.
9	VOS	Offset voltage pin from V_{out}.
10	PGOOD	Power Good output. Open drain type output that is flagged low if ±10% of V_{out}.

ABSOLUTE MAXIMUM RATINGS

Pin Name	Symbol	V_{MAX}	V_{MIN}
Main Supply Voltage Input	V_{CC}	15 V	−0.3 V
Bootstrap Supply Voltage Input	BOOT	30 V wrt/GND 38−40 V < 100 ns 15 V wrt/LX	−0.3 V
Switching Node (Bootstrap Supply Return)	LX	25 V 30 V for < 100 ns	−5 V
High−Side Driver Output (Top Gate)	UG	30 V wrt/GND 15 V wrt/LX 40 V for < 100 ns	−0.3 V wrt/LX
Low−Side Driver Output (Bottom Gate)	LG	V_{CC} + 0.3 V	−0.3 V −2 V < 100 ns
Feedback, VOS	FB, VOS	3.6 V	−0.3 V
COMP/$\overline{EN}$	COMP/$\overline{EN}$	3.6 V	−0.3 V
PGOOD	PGOOD	7 V	−0.3 V

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	165	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	45	°C/W
NCP1588 Operating Junction Temperature Range	T_J	0 to 150	°C
NCP1588 Operating Ambient Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Moisture Sensitivity Level	MSL	3	−

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS ($-40°C < T_A < 85°C$, $0°C < T_J < 125°C$; $4.5\ V < V_{CC} < 13.2\ V$, $4.5\ V < BOOT < 26.4\ V$, $C_{UG} = C_{LG} = 1.0\ nF$ (REF:NTD30N02), for min/max values unless otherwise noted.)

Characteristic		Conditions	Min	Typ	Max	Unit
Input Voltage Range			4.5		13.2	V
Boost Voltage Range		13.2 V wrt LX	4.5		26.4	V
Supply Current						
Quiescent Supply Current		V_{FB} = 1.0 V, No Switching, V_{CC} = 13.2 V		1.0	4.0	mA
Boost Quiescent Current		V_{FB} = 1.0 V, No Switching		140		μA
Undervoltage Lockout						
UVLO Threshold	NCP1588 NCP1589	V_{CC} Rising Edge	3.8 3.9		4.0 4.1	V
UVLO Hysteresis	NCP1588 NCP1589			0.37 0.2		V
Switching Regulator						
VFB Feedback Voltage	NCP1588 NCP1589	(FB Tied to Comp. Measure FB Pin.)	0.792 0.7936	0.8 0.8	0.808 0.8064	V
Oscillator Frequency			270	300	330	kHz
Ramp−Amplitude Voltage				1.1		V
Minimum Duty Cycle				0		%
Maximum Duty Cycle			70	75	80	%
LG Minimum on Time				500		ns
Error Amplifier						
Open Loop DC Gain (Note 1)			70	80		dB
Output Source Current Output Sink Current		V_{fb} < 0.8 V V_{fb} > 0.8 V	2.0 2.0			mA
Input Offset Voltage (Note 1)			−2.0	0	2.0	mV
Input Bias Current				0.1	1.0	μA
Unity Gain Bandwidth (Note 1)			15			Mhz
Disable Threshold	NCP1588 NCP1589		0.3 0.6	 0.8	0.5	V
Output Source Current During Disable					100	μA
Gate Drivers						
Upper Gate Source		V_{CC} = 5 V, VUG − VLX = 2.5 V	1.5			A
Upper Gate Sink				1.4		Ω
Lower Gate Source			1.5			A
Lower Gate Sink		V_{CC} = 12 V		1.0		Ω
UG Falling to LG Rising Delay		V_{CC} = 12 V, UG−LX < 2.0 V, LG > 2.0 V		30	90	ns
LG Falling to UG Rising Delay		V_{CC} = 12 V, LG < 2.0 V, UG > 2.0 V		30	60	ns

ELECTRICAL CHARACTERISTICS ($-40°C < T_A < 85°C$, $0°C < T_J < 125°C$; $4.5\ V < V_{CC} < 13.2\ V$, $4.5\ V < BOOT < 26.4\ V$, $C_{UG} = C_{LG} = 1.0\ nF$ (REF:NTD30N02), for min/max values unless otherwise noted.)

Characteristic	Conditions	Min	Typ	Max	Unit
Soft−Start					
Soft−Start time		3.0		7.0	ms
Power Good					
Output Saturation Voltage	IPG = 4 mA, V_{CC} = 12 Vdc			0.4	V
OVP Threshold to Part Disable			1.0		V
UVP Threshold to Part Disable			0.6		V
OVP Threshold to PGOOD Output Low			0.88		V
UVP Threshold to PGOOD Output Low			0.72		V
Overcurrent Protection					
OC Current Source	Sourced from LG pin, before SS		10		μA

1. Guaranteed by design but not tested in production.

TYPICAL CHARACTERISTICS

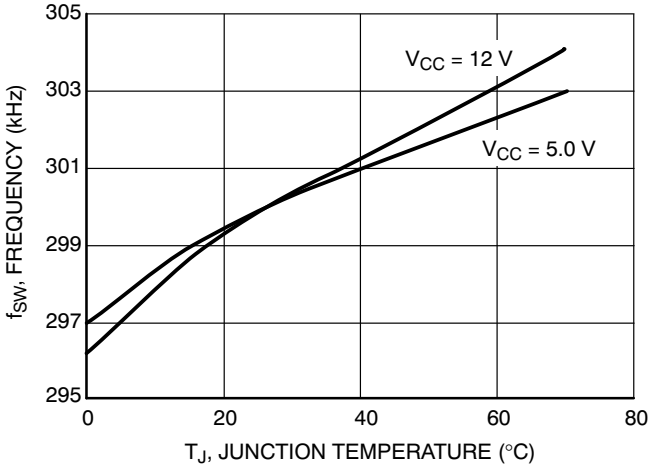


Figure 3. Oscillator Frequency (f_{SW}) vs. Temperature

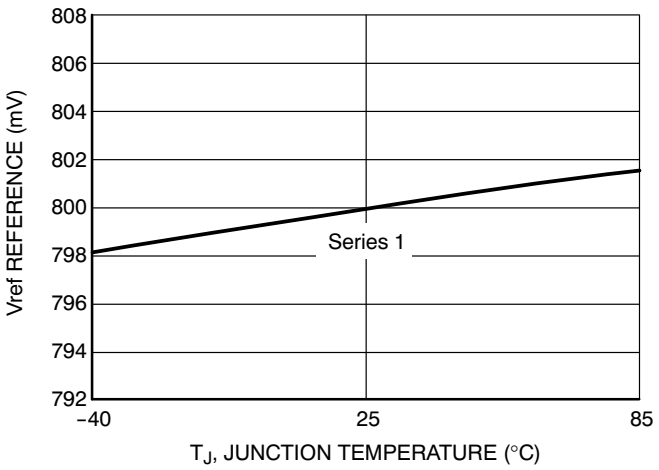


Figure 4. Reference Voltage (V_{ref}) vs. Temperature

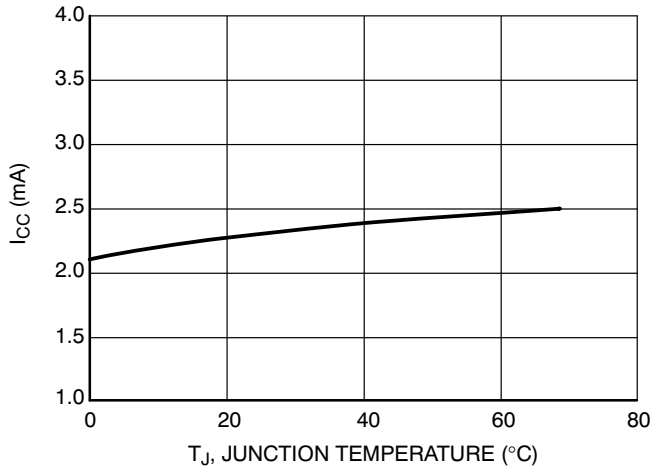


Figure 5. I_{CC} vs. Temperature

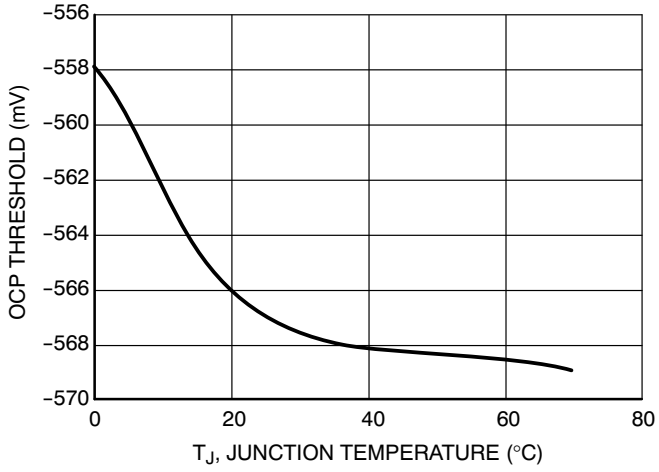


Figure 6. OCP Threshold with 55k Rset vs. Temperature

APPLICATIONS INFORMATION

Overcurrent Protection (OCP)

The low−side R_{DSon} sense is implemented by comparing the voltage at the LX, at the end of LG on time to an internally generated fixed voltage. If the phase voltage is lower than OCP trip voltage, an overcurrent condition occurs and a counter is initiated.

When the counter completes after two clock cycles, the PWM logic and both HS−FET and LS−FET are turned off. Power has to be recycled to exit out of the overcurrent fault. The minimum turn−on time of the LS−FET is set to be 500 ns.

NCP158x allows to easily program an Overcurrent Threshold ranging from 50 mV to 550 mV, simply by adding a resistor (ROCSET) between LG and GND. During a short period of time following V_{CC} rising over UVLO threshold, an internal 10 μA current (IOCSET, trimmed to ±5%) is sourced from LG pin, determining a voltage drop across ROCSET. This voltage drop will be sampled and internally held by the device as OverCurrent Threshold. The OC setting procedure overall time length is about 4.2 ms. Connecting a ROCSET resistor between LG and GND, the programmed threshold will be:

$$I_{OCth} = \frac{I_{OCSET} \cdot R_{OCSET}}{R_{DS(on)}}$$

RSET values range from 5 kΩ to 55 kΩ. In case ROCSET is not connected, the device switches the OCP threshold to a fixed 640 mV value: an internal safety clamp on BG is triggered as soon as LG voltage reaches 700 mV, enabling the 640 mV fixed threshold and ending OC setting phase. The current trip threshold tolerance is ±25 mV. The accuracy of the set point is best at the highest set point. The accuracy will decrease as the set point decreases.

Internal Soft –Start

The NCP158x features an internal soft−start function, which reduces the inrush current and overshoot of the output voltage. Figure 7. shows a typical soft−start sequence. Soft−Start is achieved by ramping the internal reference using the oscillator clock (64 steps from 0 V to 0.8 V of V_{ref}). The order of startup sequence is as follows: UVLO → OCP programming → Comp voltage reach the lower end of the Ramp voltage (1.45 V). The typical soft−start time is 4.2 ms. The internal soft−start is held low when the part is in UVLO or Disable mode.

Power Good

Power Good is an open drain and active high output. This output can be pulled up high to the appropriate level with an external resistor. It monitors the output voltage through the VOS pin. The PGOOD is flagged low for ±10% of Vout for OV/UV trip points respectively. The separate VOS input is not slowed down by the compensation on the VFB pin. The PGOOD output can deliver a max of 4 mA sink current at 0.4 V when de−asserted. The PGOOD pin is held low during soft−start. Once soft−start is complete PGOOD goes high if there are no faults without any delays associated to it.

Undervoltage Protection

If the voltage at VOS pin drops below UV threshold, the device turns off both HS and LS MOSFETs, latching the condition. This requires a POR to recover.

Overvoltage Protection

If the voltage at VOS pin rises over OV threshold (1V typ), overvoltage protection turns off UG MOSFET and turns on LG MOSFET. The LG MOSFET will be turned off as soon as VOS goes below Vref/2 (0.4 V). The condition is latched, and requires POR to recover. The device still controls the LG MOSFET and can switch it on whenever VOS rises above 1.0 V.

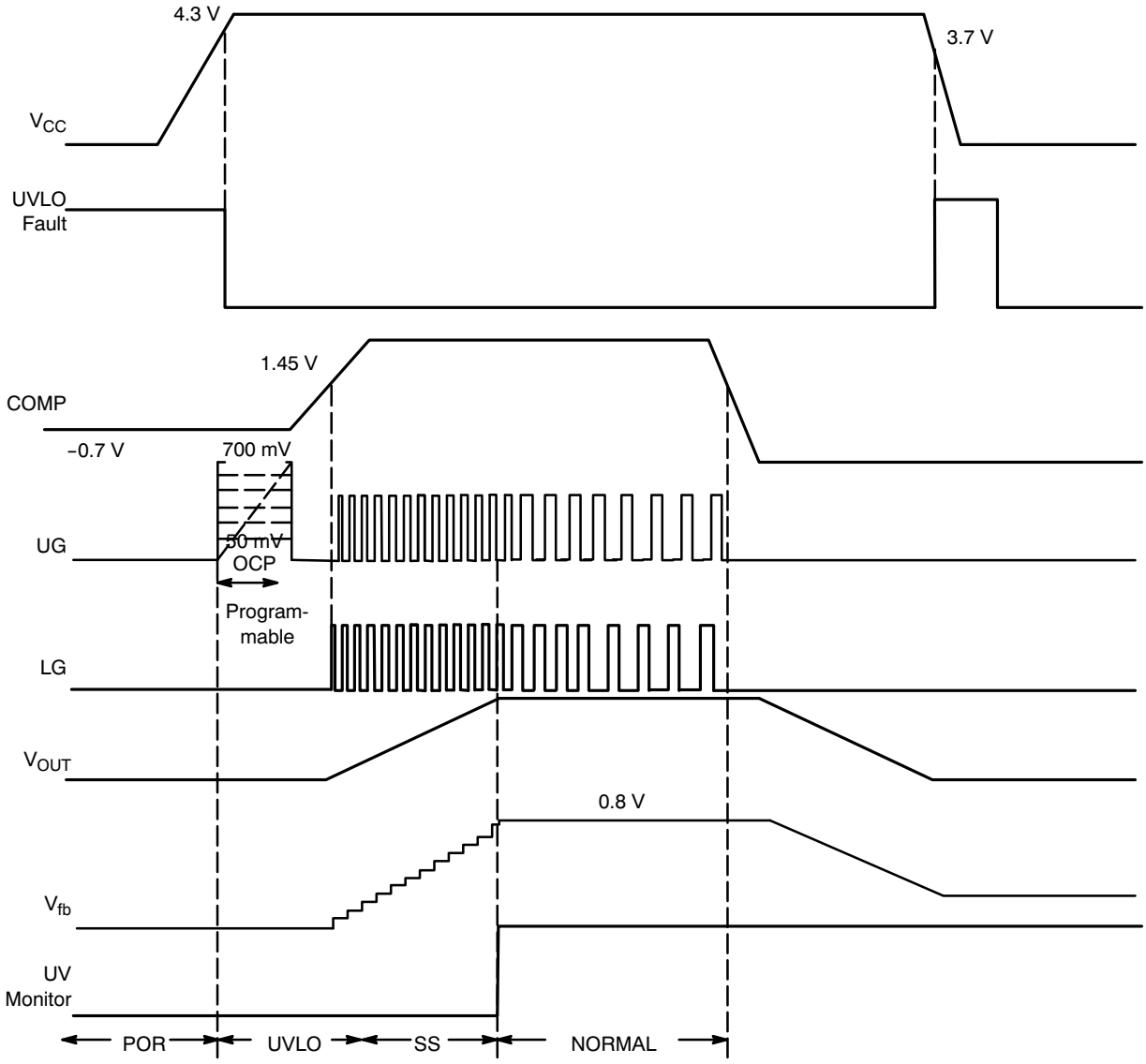


Figure 7. Typical Startup Sequence

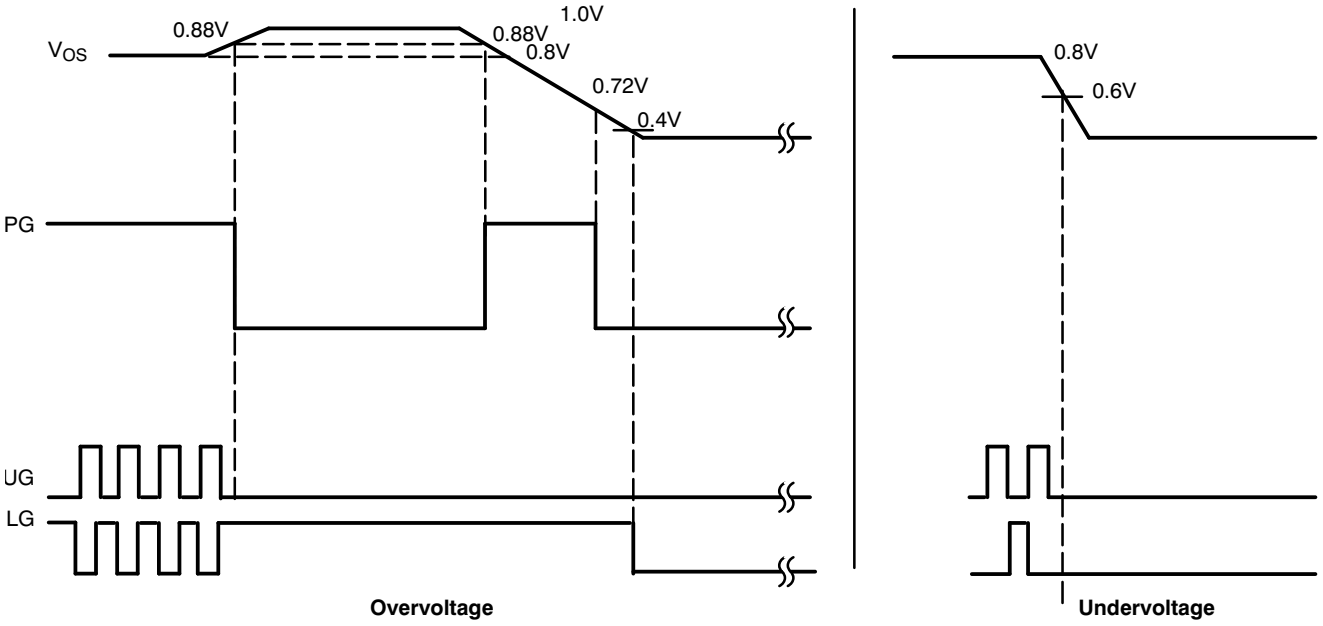


Figure 8. Typical Power Good Function

Feedback and Compensation

The NCP158x allows the output voltage to be adjusted from 0.8 V to 5.0 V via an external resistor divider network. The controller will try to maintain 0.8 V at feedback pin. Thus, if a resistor divider circuit was placed across the feedback pin to V_{OUT}, the controller will regulate the output voltage proportional to the resistor divider network in order to maintain 0.8 V at the FB pin. The same formula applies to the VOS pin and the controller will maintain 0.8 V at the VOS pin.

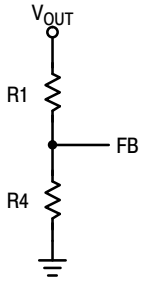


Figure 9.

The relationship between the resistor divider network above and the output voltage is shown in the following equation:

$$R_4 = R_1 \times \left(\frac{V_{REF}}{V_{OUT} - V_{REF}}\right)$$

The same formula can be applied to the feedback resistors at VOS.

$$R_9 = R_{10} \times \left(\frac{V_{REF}}{V_{OUT} - V_{REF}}\right)$$

Design Example

Voltage Mode Control Loop with TYPE III Compensation

Converter Parameters:

Input Voltage: V_{IN} = 5 V
Output Voltage: V_{OUT} = 1.65 V
Switching Frequency: 300 kHz
Total Output Capacitance: C_{OUT} = 3600 μF
Total ESR: ESR = 6 mΩ
Output Inductance: L_{OUT}: 1 μH
Ramp Amplitude: V_{RAMP} = 1.1 V

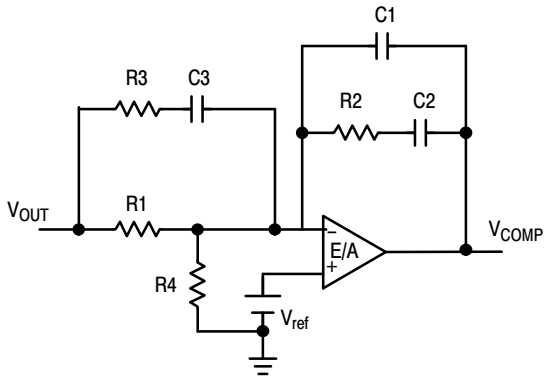


Figure 10.

a.. Set a target for the close loop bandwidth at $1/6^{th}$ of the switching frequency.

$F_{cross_over} := 50$ kHz

b.. Output Filter Double Pole Frequency

$$F_{lc} := \frac{1}{2 \cdot \pi \cdot \sqrt{L_{OUT} \cdot C_{OUT}}}$$

$$F_{lc} = 2.653\ \text{kHz}$$

c.. ESR Zero Frequency:

$$F_{ESR} := \frac{1}{2 \cdot \pi \cdot C_{OUT} \cdot C_{ESR}}$$

$$F_{ESR} = 7.368\ \text{kHz}$$

Step 1: Set a value for R1 between 2 kΩ and 5 kΩ

$$R1 := 4.12\ \text{k}\Omega$$

Step 2: Pick compensation DC gain (R2/R1) for desired close loop bandwidth.

$$V_{RAMP} := 1.1\ \text{V}$$

$$R2 := R1 \cdot \left(\frac{V_{RAMP}}{V_{IN}}\right) \cdot \left(\frac{F_{cross_over}}{F_{lc}}\right)$$

$$R2 = 17.085\ \text{k}\Omega$$

Step 3: Place 1st zero at half the output filter double pole frequency.

$$C2 := \frac{2 \cdot \sqrt{L_{OUT} \cdot C_{OUT}}}{R2}$$

$$C2 = 7.024 \times 10^{-3}\ \mu\text{F}$$

Step 4: Place 1st pole at ESR zero frequency.

$$C1 := \frac{C2}{C2 \cdot R2 \cdot 2 \cdot \pi \cdot F_{ESR} - 1}$$

$$C1 = 1.542 \times 10^{-3}\ \mu\text{F}$$

Step 5: Place 2nd zero at the output filter double pole frequency.

$$R3 := \frac{R1}{\frac{F_{SW}}{2 \cdot F_{lc}} - 1}$$

$$R3 = 74.169\ \Omega$$

Step 6: Place 2nd pole at half the switching frequency.

$$C3 := \frac{1}{\left(\pi \cdot R3 \cdot F_{SW}\right)}$$

$$C3 = 0.014\ \mu\text{F}$$

Step 7: R4 is sized to maintain the feedback voltage to V_{ref} = 0.8 V.

$$R4 := \frac{V_{REF} \cdot R1}{V_{OUT} - V_{REF}}$$

$$R4 = 3.878\ \text{k}\Omega$$

The Component values for Type III Compensation are:

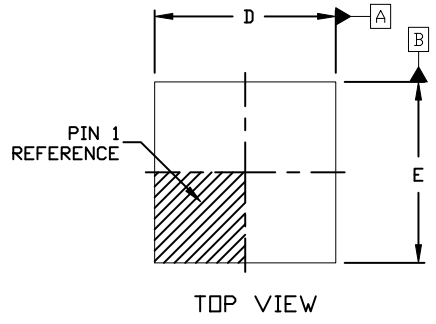
R1 = 4.12 kΩ
R2 = 17.085 kΩ
R3 = 74.169 Ω
R4 = 3.878 kΩ
C1 = 0.0015 μF
C2 = 0.007 μF
C3 = 0.014 μF

NOTE: Recommend to change values to industry standard component values.

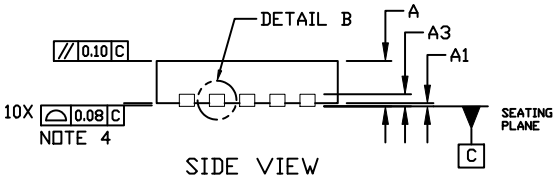
DFN10, 3x3, 0.5P
CASE 485C
ISSUE F

DATE 16 DEC 2021

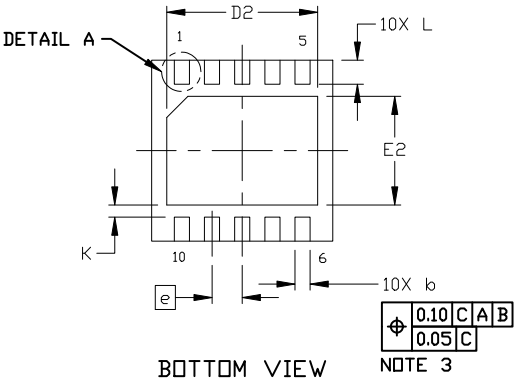
SCALE 2:1



TOP VIEW

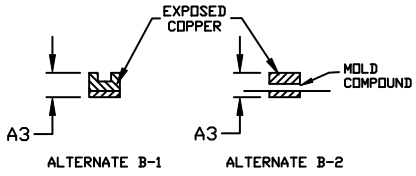


SIDE VIEW

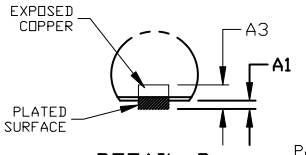


BOTTOM VIEW

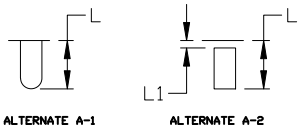
NOTES:
1. DIMENSION AND TOLERANCING PER ASME Y14.5, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL b MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASH MAY NOT EXCEED 30 MICRONS ONTO BOTTOM SURFACE OF TERMINAL.
6. FOR DEVICE OPN CONTAINING W OPTION, DETAIL A AND DETAIL B ALTERNATE CONSTRUCTIONS ARE NOT APPLICABLE. WETTABLE FLANK CONSTRUCTION IS DETAIL B AS SHOWN ON SIDE VIEW OF PACKAGE.



DETAIL B
ALTERNATE CONSTRUCTION

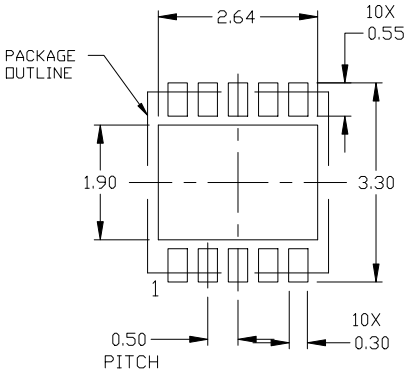


DETAIL B
WETTABLE FLANK
CONSTRUCTION



DETAIL A
ALTERNATE CONSTRUCTION

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	---	0.05
A3		0.20 REF	
b	0.18	0.23	0.30
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
E	2.90	3.00	3.10
E2	1.70	1.80	1.90
e		0.50 BSC	
K		0.20 REF	
L	0.30	0.40	0.50
L1	---	---	0.03



RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON03161D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**DFN10, 3X3 MM, 0.5 MM PITCH**		**PAGE 1 OF 1**

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