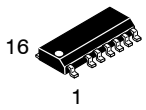
High Performance Current Mode Resonant Controller with Integrated High-Voltage Drivers

NCP13994



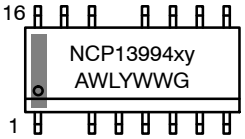
SOIC−16 NB MISSING PINS 2 AND 13
CASE 751DU

The NCP13994 is a high performance current mode controller for half bridge resonant converters. This controller implements 700 V gate drivers, simplifying layout and reducing external component count. The built−in Brown−Out input function eases implementation of the controller in all applications. In applications where a PFC front stage is needed, the NCP13994 features a dedicated output to drive the PFC controller. This feature together with quiet skip mode technique further improves light load efficiency of the whole application. The NCP13994 provides a suite of protection features allowing safe operation in any application. This includes: overload protection, over−current protection to prevent hard switching cycles, brown−out detection, line brown−out, line OVP, X2 cap discharge, open optocoupler detection, automatic dead−time adjust, over−voltage (OVP) and over−temperature (OTP) protections.

Features

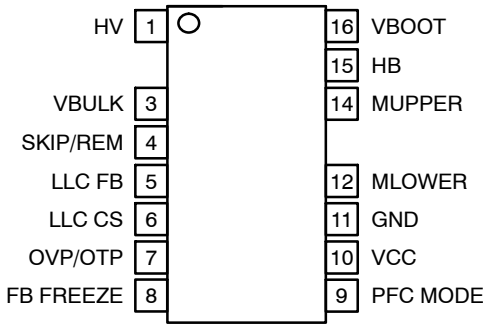
- Up to 700 V Operating Range for High Side Driver
- Up to 700 V Operating Range for HV Startup Current Source
- Line Brown−out and OVP Protections
- X2 Cap Discharge Function
- Clamped Output Drivers
- Up to 30 V Supply
- High−Frequency Operation from 20 kHz up to 750 kHz
- Current Mode Control Scheme
- Automatic Dead−time with Maximum Dead−time Clamp
- Enhanced Startup Sequence for Fast Resonant Tank Stabilization
- Light Load Operation Mode for Improved Efficiency
- Quiet Skip Operation Mode for Minimize Transformer Acoustic Noise
- Off−mode Operation for Extremely Low No−load Consumption
- Latched or Auto−recovery Overload Protection
- Latched or Auto−recovery Output Short Circuit Protection with Current Reduction
- Latched Input for Severe Fault Conditions, e.g. OVP or OTP
- Out of Resonance Switching Protection
- Open Feedback Loop Protection
- Precise Brown−out Protection
- PFC Stage Operation Control According to Load Conditions
- Startup Current Source with Extremely Low Leakage Current
- Dynamic Self−Supply (DSS) Operation in Off−mode or Fault Modes

MARKING DIAGRAM



NCP13994	= Device Code
xy	= Specific Device Option
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 45 of this data sheet.

Features (continued)

- Pin to Adjacent Pin / Open Pin Fail Safe
- This is a Pb−Free Device

Typical Applications

- Adapters and Offline Battery Chargers
- Flat Panel Display Power Converters
- Computing Power Supplies
- Industrial and Medical Power Sources

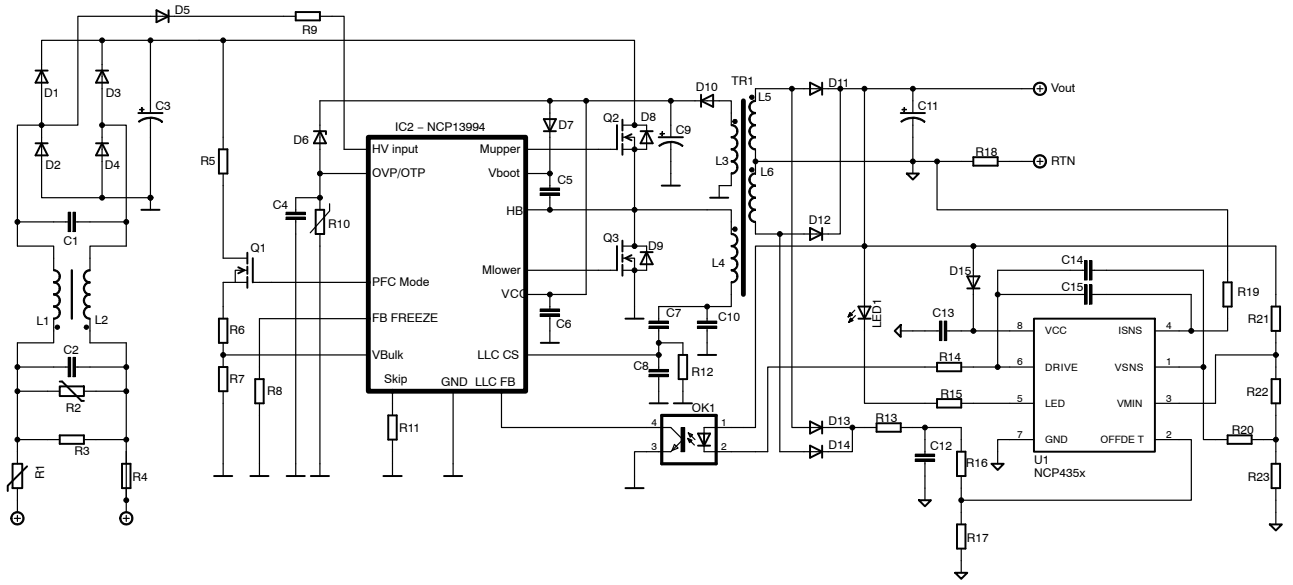


Figure 1. Typical Application Example without PFC Stage

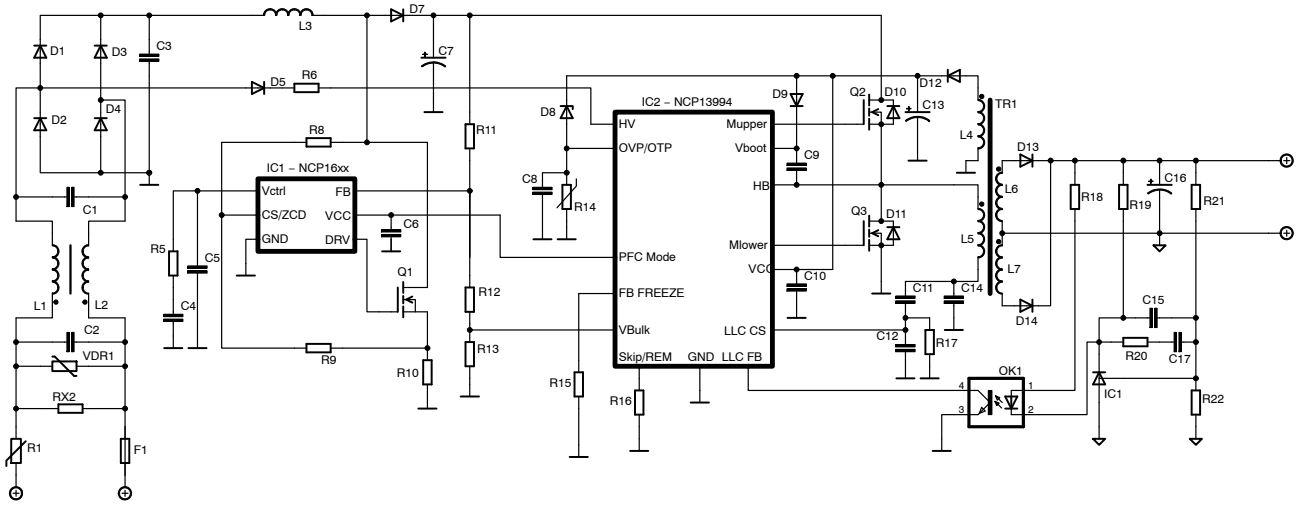


Figure 2. Typical Application Example with PFC Stage

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Function	Pin Description
1	HV	High−voltage startup current source input	Connects to rectified AC line or to bulk capacitor to perform functions of Start−up Current Source and Dynamic Self−Supply. Provides X2 cap discharge and line BO/OVP functions when connected to AC line.
2	NC	Not connected	Increases the creepage distance.
3	VBULK	Bulk voltage monitoring input	Receives divided bulk voltage to perform Brown−out protection.
4	SKIP/REM	Skip threshold adjust	Sets the skip in threshold via a resistor connected to ground. Controls off−mode operation for active−on version (version dependend).
5	LLC FB	LLC feedback input	Defines operating frequency based on given load conditions. Activates skip/LL mode operation under light load conditions. Activates off−mode operation for active −off version.
6	LLC CS	LLC current sense input	Senses divided resonant capacitor voltage to perform on−time modulation, out of resonant switching protection, over−current protection and secondary side short circuit protection.
7	OTP / OVP	Over−temperature and over−voltage protection input	Implements over−temperature and over−voltage protection on single pin.
8	FB FREEZE	Minimum internal FB level	Adjusts minimum internal FB level that can be reached during light load operation.
9	PFC MODE/SKIP	PFC and external HV switch control output	Provides supply or control voltage for PFC front stage controller. Sets the skip out threshold.
10	VCC	Supplies the controller	The controller supply pin.
11	GND	Analog ground	Common ground connection for adjust components, sensing networks and DRV output.
12	MLOWER	Low side driver output	Drives the lower side MOSFET
13	NC	Not connected	Increases the creepage distance
14	MUPPER	High side driver output	Drives the higher side MOSFET
15	HB	Half−bridge connection	Connects to the half−bridge point.
16	VBOOT	Bootstrap pin	The floating supply for the upper stage.

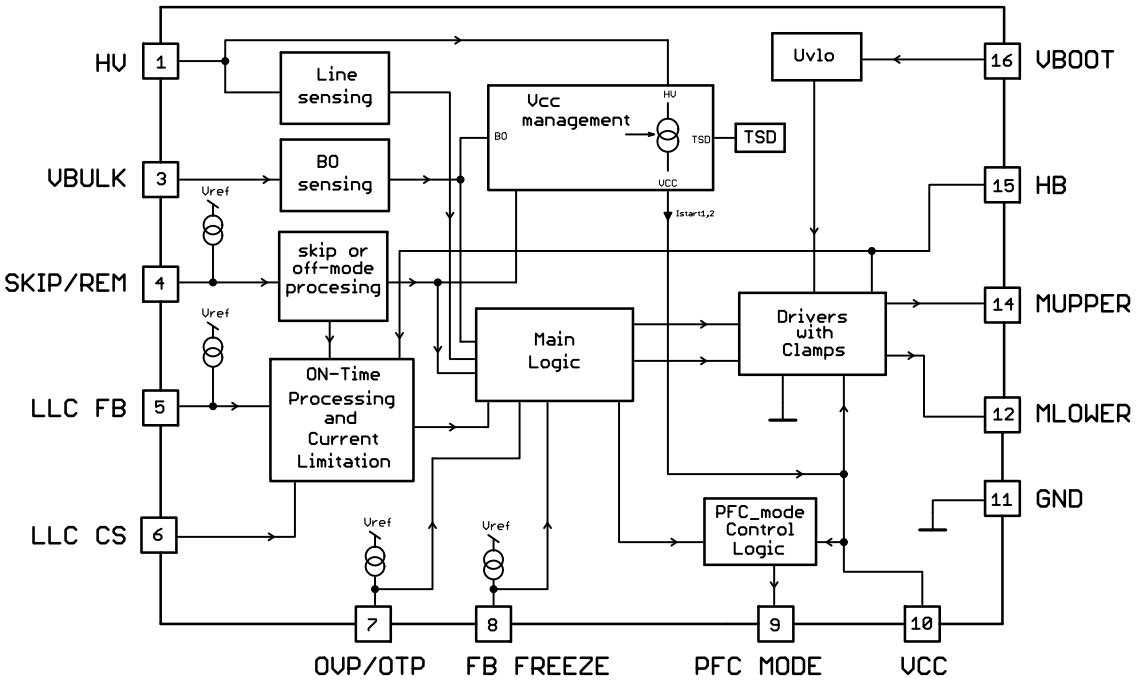


Figure 3. Internal Circuit Architecture

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{HV}	HV Startup Current Source HV Pin Voltage (Pin 1)	–0.3 to 700	V
$V_{BULK/PFC\ FB}$	VBULK Pin Voltage (Pin3)	–0.3 to 5.5	V
V_{SKIP}	SKIP/REM Pin Voltage (Pin 4)	–0.3 to 5.5	V
V_{FB}	LLC FB Pin Voltage (Pin 5)	–0.3 to 5.5	V
V_{CS}	LLC CS Pin Voltage (Pin 6)	–5 to 5	V
$V_{OVP/OTP}$	OVP/OTP Pin Voltage (Pin 7)	–0.3 to 5.5	V
$V_{P\ ON/OFF}$	FB FREEZE Pin Voltage (Pin 8)	–0.3 to 5.5	V
$V_{PFC\ MODE}$	PFC MODE Pin Output Voltage (Pin 9)	–0.3 to VCC + 0.3	V
V_{CC}	VCC Pin Voltage (Pin 10)	–0.3 to 30	V
V_{DRV_MLOWER}	Low Side Driver Output Voltage (Pin 12)	–0.3 to VCC + 0.3	V
V_{DRV_MUPPER}	High Side Driver Output Voltage (Pin 14)	VHB – 0.3 to VBOOT + 0.3	V
V_{HB}	High Side Offset Voltage (Pin 15)	VBoot –30 to VBoot +0.3	V
V_{BOOT}	High Side Floating Supply Voltage (Pin 16)	–0.3 to 730	V
$V_{Boot–VHB}$	High Side Floating Supply Voltage (Pin 15 and 16)	–0.3 to 30	V
dV/dt_{max}	Allowable Output Slew Rate on HB Pin (Pin 15)	100	V/ns
T_J	Junction Temperature	–50 to 150	°C
T_{STG}	Storage Temperature	–55 to 150	°C
$R_{\theta JA}$	Thermal Resistance Junction–to–air	130	°C/W
–	Human Body Model ESD Capability per JEDEC JESD22–A114F (Except Pins 14, 15, 16)	4	kV
–	Human Body Model ESD Capability per JEDEC JESD22–A114F (Pin 14, 15, 16)	2	kV
–	Charged–Device Model ESD Capability per JEDEC JESD22–C101E	1	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device contains latch–up protection and exceeds 100 mA per JEDEC Standard JESD78 (Except Pin 5 and Pin 8, Pin 5 – 50 mA, Pin 8 – 10 mA).

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{CC} = 12 V unless otherwise noted)

Symbol	Parameter	Pin	Min	Typ	Max	Unit
HV STARTUP CURRENT SOURCE						
V_{HV_MIN1}	Minimum Voltage for Current Source Operation (V_{CC} = V_{CC_ON} − 0.5 V, I_{START2} Drops to 95 %)	1	–	–	50	V
V_{HV_MIN2}	Minimum Voltage for Current Source Operation (V_{CC} = V_{CC_ON} − 0.5 V, I_{START2} Drops to 5 mA)	1	–	–	50	V
I_{START1}	Current Flowing Out of V_{CC} Pin (V_{CC} = 0 V)	1, 10	0.2	0.5	0.8	mA
I_{START2}	Current Flowing Out of V_{CC} Pin (V_{CC} = V_{CC_ON} −0.5 V)	1, 10	6	9	13	mA
I_{START_OFF}	Off−state Leakage Current (V_{CC} = 15 V)	1	–	–	25	μA
$T_{HV\_CS\_CLAMP}$	Temperature where I_{START2} Drops to 95% of I_{START2}	1	–	130	–	°C
SUPPLY SECTION						
V_{CC_ON}	Turn−on Threshold Level, V_{CC} Going Up (NCP13994AA) (NCP13994AC)	10	 15.2 11.4	 16 12	 16.8 12.6	V
V_{CC_OFF}	Minimum Operating Voltage after Turn−on	10	8.5	9	9.5	V
V_{CC_RESET}	V_{CC} Level at which the Internal Logic Gets Reset	10	5.8	6.5	7.2	V
$V_{CC\_INHIBIT}$	V_{CC} Level for I_{START1} to I_{START2} Transition	10	1.25	2.00	2.75	V
$I_{CC\_OFF-MODE}$	Controller Supply Current in Off−mode	10, 11	–	150	300	μA
$I_{CC\_SKIP-MODE}$	Controller Supply Current in Skip−mode, V_{CC} = 15 V, OVP/OTP Block De−biased During Skip Mode	10, 11	–	900	1400	μA
I_{CC_LATCH}	Controller Supply Current in Latch−off Mode	10, 11	–	150	300	μA
$I_{CC\_AUTOREC}$	Controller Supply Current in Auto−recovery Mode	10, 11	–	135	350	μA
$I_{CC\_OPERATION}$	Controller Supply Current in Normal Operation, f_{sw} = 100 kHz, C_{load} = 1 nF, V_{CC} = 15 V	10, 11	–	–	6.5	mA
$I_{CC\_LIGHTLOAD}$	Controller Supply Current in Normal Operation, fsw = 100 kHz, Cload 1 nF, VCC = 15 V	10, 11	–	–	4.5	mA
HV SENSE (EXCEPT NCP13994AC)						
V_{HV_UP}	Line Brown−In Threshold, V_{HV} Going Up	1	100	110	122	V
V_{HV_DOWN}	Line Brown−Out Thresholds, V_{HV} Going Down	1	93	103	114	V
t_{HV}	Timer Duration for Line Cycle Drop−out, (Note 2)	1	57	64	80	ms
V_{HV_OVP}	Line Overvoltage Threshold, V_{HV} Going Up	1	371	412	454	V
$V_{HV\_OVP\_HYST}$	Line Overvoltage Comparator Hysteresis, V_{HV} Going Down	1	15	20	25	V
$t_{HV\_OVP\_BLANK}$	Blanking Duration for Line Overvoltage Detection, (Note 2)	1	227	250	317	μs
X2 DISCHARGE (EXCEPT NCP13994AC)						
I_{DISCH}	X2 Discharge Current, V_{HV} = 45 V	1	3	4	5	mA
V_{HV_X2}	Comparator Hysteresis Observed at HV Pin	1	–	4	8	V
t_{SAMPLE}	HV Signal Sampling Period	1	–	1.0	–	ms
t_{X2_DET}	Timer Duration for No Line Detection, (Note 2)	1	90	100	127	ms
V_{X2_END}	HV Pin Voltage when X2 Discharging Process is Ended	1	20	30	40	V
BOOTSTRAP SECTION						
V_{BOOT_ON}	Startup Voltage on the Floating Section (Note 3)	16, 15	9.0	9.7	10.5	V
V_{BOOT_OFF}	Cutoff Voltage on the Floating Section	16, 15	8.0	8.7	9.5	V
I_{BOOT1}	Upper Driver Consumption, No DRV Pulses, V_{BOOT} = 12 V	16, 15	30	85	130	μA
I_{BOOT2}	Upper Driver Consumption, C_{load} = 1 nF between Pins 13 & 15 f_{sw} = 100 kHz, V_{BOOT} = 12 V, HB Connected to GND	16, 15	–	1.3	1.5	mA

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{CC} = 12 V unless otherwise noted) (continued)

Symbol	Parameter	Pin	Min	Typ	Max	Unit
HB DISCHARGER						
$I_{HB\_DISCHARGE1}$	HB Sink Current Capability V_{HB} = 30 V	15	–	6	10	mA
$I_{HB\_DISCHARGE2}$	HB Sink Current Capability V_{HB} = V_{HB_MIN}	15	1	6	9	mA
V_{HB_MIN}	HB Voltage @ $I_{DISCHARGE}$ Changes from 2 to 0 mA	15	–	–	20	V
$T_{HB\_DISCH\_CLAMP}$	Temperature where $I_{HB\_DISCHARGE1}$ Drops to 95% of $I_{HB\_DISCHARGE1}$	15	–	130	–	°C
DRIVER OUTPUTS						
t_r	Output Voltage Rise−time @ C_L = 1 nF, 10 − 90% of Output Signal	12, 14	–	–	50	ns
t_f	Output Voltage Fall−time @ C_L = 1 nF, 10 − 90% of Output Signal	12, 14	–	–	50	ns
R_{OH}	Source Resistance	12, 14	–	6	32	Ω
R_{OL}	Sink Resistance	12, 14	–	4	11	Ω
V_{DRVH_CLAMP}	Upper Driver Clamp Voltage, R_{DRV} = 33 kΩ, C_{load} = 220 pF	14, 15	12.5	14.5	17.5	V
V_{DRVL_CLAMP}	Lower Driver Clamp Voltage, R_{DRV} = 33 kΩ, C_{load} = 220 pF	12, 11	12.5	14.5	17.5	V
$I_{DRVSOURCE}$	Output High Short Circuit Pulsed Current V_{DRV} = 0 V, PW ≤ 10 μs GBD	12, 14	–	1	–	A
$I_{DRVSINK}$	Output High Short Circuit Pulsed Current V_{DRV} = VCC, PW ≤ 10 μs GBD	12, 14	–	1	–	A
$I_{HB\_CELL\_LEAK}$	Leakage Current on High Voltage Pins to GND	14, 15, 16	–	–	15	μA
dV/dt DETECTOR						
P_{dV/dt_th1}	Positive Slew Rate on V_{BOOT} pin above which is dV/dt_P Sensor Triggered, V_{HB} Rising Linearly	16	–	300	–	V/μs
N_{dV/dt_th1}	Negative Slew Rate on V_{BOOT} Pin above which is dV/dt_N Sensor Triggered, V_{HB} Falling Linearly	16	–	300	–	V/μs
P_{dV/dt_th2}	Positive Slew Rate on V_{BOOT} pin above which is dV/dt_P Sensor Triggered, V_{HB} Rising Linearly	16	–	100	–	V/μs
N_{dV/dt_th2}	Negative Slew Rate on V_{BOOT} pin above which is dV/dt_N Sensor Triggered, V_{HB} Falling Linearly	16	–	100	–	V/μs
OVP/OTP						
V_{OVP}	OVP Threshold Voltage ($V_{OVP/OTP}$ Going Up)	7	2.35	2.50	2.65	V
V_{OTP}	OTP Threshold Voltage ($V_{OVP/OTP}$ Going Down)	7	0.76	0.80	0.84	V
V_{OTP_HIGH}	OTP Threshold Voltage (OTP Going Up − Hysteretic Mode)	7	0.72	0.8	0.88	V
V_{OTP_LOW}	OTP Threshold Voltage (OTP Going Down − Hysteretic Mode)	7	0.45	0.5	0.55	V
R_{OTP}	OTP Resistance Threshold (Resistance is Going Down)	7	8.20	8.95	9.80	kΩ
R_{OTP}	OTP Resistance Threshold (Resistance is Going Down), T_j = 80°C	7	–	9	–	kΩ
R_{OTP}	OTP Resistance Threshold (Resistance is Going Down), T_j = 110°C	7	–	9.05	–	kΩ
I_{OTP}	OTP/OVP Pin Source Current for External NTC − During Normal Operation	7	81	90	99	μA
I_{OTP_BOOST}	OTP/OVP Pin Source Current for External NTC − During Startup	7	162	180	198	μA
t_{OVP_FILTER}	Internal Filter for OVP Comparator, (Note 2)	7	35	39	48	μs
t_{OTP_FILTER}	Internal Filter for OTP Comparator, (Note 2)	7	320	350	435	μs
t_{BLANK_OTP}	Blanking Time for OTP Input During Startup, (Note 2) (NCP1399AA) (NCP1399AC)	7	 3.6 14.4	 4 16	 5 20	ms
V_{CLAMP_OVP/OTP_1}	OVP/OTP Pin Clamping Voltage @ $I_{OVP/OTP}$ = 0 mA	7	1.1	1.2	1.3	V
V_{CLAMP_OVP/OTP_2}	OVP/OTP Pin Clamping Voltage @ $I_{OVP/OTP}$ = 1 mA	7	2.0	2.4	2.8	V

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{CC} = 12 V unless otherwise noted) (continued)

Symbol	Parameter	Pin	Min	Typ	Max	Unit
START−UP SEQUENCE						
$t_{1st\_MLOWER\_TON}$	Initial Mlower DRV On−time Duration, (Note 2) (NCP1399AA) (NCP1399AC)	12	 2.30 4.61	 2.56 5.12	 2.820 5.63	µs
$t_{1st\_MUPPER\_TON}$	Initial Mupper DRV On−time Duration, (Note 2) (NCP1399AA) (NCP1399AC)	14	 0.71 1.22	 0.79 1.36	 0.87 1.49	µs
$t_{TON\_SS\_INC}$	On−time Period Increment During Soft−start, (Note 2)	12, 14	18	20	22	ns
$N_{FB\_SS\_INC}$	Internal FB Ramp Increment During Soft Start	12, 14	−	7	−	−
$K_{FB\_SS\_INC}$	Soft−Start Increment Division Ratio, (Note 2)	12, 14	−	1	−	−
$t_{WATCHDOG}$	Time Duration to Restart IC if Start−up Phase is not Finished	12, 14	0.46	0.51	0.56	ms
$K_{1st\_MUPPER\_INC}$	First Mupper On−time Increment after Watchdog Elapses	14	−	0.125	−	−
FEEDBACK SECTION						
R_{FB}	Internal Pull−up Resistor on FB Pin	5	15	18	25	kΩ
R_{FB_SKIP}	Internal Pull−up Resistor on FB Pin at Skip Off−time	5	15	18	25	kΩ
K_{FB}	V_{FB} to Internal Current Set Point Division Ratio (NCP1399AA) (NCP1399AC)	5	 0.96 1.92	 1.00 2.00	 1.04 2.08	−
V_{FB}	Internal Voltage Reference on the FB Pin (NCP1399AA) (NCP1399AC)	5	 2.2 4.5	 2.5 4.9	 2.6 5.2	V
V_{FB_CLAMP}	Internal Clamp on FB Input of On−time Comparator Referred to External FB Pin Voltage (NCP1399AA) (NCP1399AC)	5	 2.15 4.3	 2.3 4.6	 2.45 4.9	V
V_{FB_OFFSET}	Internal FB Offset Voltage to Compensate Opto−coupler Saturation Level (NCP1399AA) (NCP1399AC)	5, 6	 190 81	 216 104	 242 127	mV
$V_{FB\_OFFSET\_COMP\_SS}$	V_{FB_OFFSET} Compensation During Soft Start	5, 6	−	0	−	mV
$V_{FB\_OFFSET\_COMP}$	V_{FB_OFFSET} Compensation During Normal Operation (NCP1399AA) (NCP1399AC)	5, 6	 115 −	 152 0	 185 −	mV
$LFF_{\_GAIN}$	Line Feed Forward Gain Applied on Internal FB ($V_{VBULK} > V_{BO}$) (NCP1399AA) (NCP1399AC)	3, 6	 − −	 0.25 0	 − −	V/V
CURRENT SENSE INPUT SECTION						
t_{CS_DELAY}	On−time Comparator Delay to Mupper Driver Turn Off V_{FB} = 2.5 V, V_{CS} Goes Up from −2.5 V to 2.5 V with Rising Edge of 100 ns	5, 6	−	−	110	ns
$I_{CS\_LEAKAGE}$	Current Sense Input Leakage Current for V_{CS} = ±3 V	6	−	−	±130	µA
t_{LEB}	Leading Edge Blanking Time of the On−time Comparator Output, (Note 2) (NCP1399AA) (NCP1399AC)	5, 6, 14	 360 396	 400 440	 440 484	ns

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{CC} = 12 V unless otherwise noted) (continued)

Symbol	Parameter	Pin	Min	Typ	Max	Unit
SKIP						
$t_{1st\_MLOWER\_SKIP}$	On−time Duration of 1st Mlower Pulse when FB Cross $V_{FB\_SKIP\_IN}$ + $V_{FB\_SKIP\_HYST}$ Threshold, (Note 2) (NCP1399AA) (NCP1399AC)	5, 12	 0.57 1.87	 0.64 2.08	 0.71 2.29	µs
$V_{1st\_MUPPER\_SKIP}$	Internal FB Level Reduction During 1st Mupper Pulse when FB Cross $V_{FB\_SKIP\_IN}$ + $V_{FB\_SKIP\_HYST}$ Threshold (Note 2) (NCP1399AA) (NCP1399AC)	5, 6, 14	 − −	 63 0	 − −	−
SKIP INPUT						
I_{SKIP_IN}	Internal Skip Pin Current Source (NCP1399AA) (NCP1399AC)	4	 18 45	 20 50	 22 55	µA
I_{SKIP_OUT}	Internal Skip Out Pin Current Source (NCP1399AA) (NCP1399AC)	9	 18 45	 20 50	 22 55	µA
$C_{SKIP\_LOAD\_MAX}$	Maximum Loading Capacitance for Skip Pin Voltage Filtering (Note 2)	4, 9	−	−	10	nF
QUIET−SKIP						
$V_{FB\_LL\_IN}$	Feedback Voltage Thresholds to Enter Light Load Mode (NCP1399AA) (NCP1399AC)	5	 0.97 −	 1.08 0	 1.19 −	V
$V_{FB\_LL\_OUT}$	Feedback Voltage Thresholds to Exit Light Load Mode (NCP1399AA) (NCP1399AC)	5	 1.02 −	 1.14 0	 1.25 −	V
$t_{LAST\_ML\_PATTERN}$	The Portion of Previous MU On−time that is Place for Last ML Pulse in Pattern	12	−	25	−	%
$t_{LAST\_ML\_SKIP}$	The Portion of Previous MU On−time that is Place for Last ML Pulse before the LL or Skip Mode is Activated (NCP1399AA) (NCP1399AC)	12	 − −	 150 50	 − −	%
t_{GEAR_UP}	Skip Burst Off−time Duration that is Needed to Increase Number of Skipped Valleys/Peaks between Following Patterns	12, 14	−	5	−	ms
t_{GEAR_DOWN}	Skip Burst On−time Duration that is Needed to Decrease Number of Skipped Valleys/Peaks between Following Patterns	12, 14	−	30	−	ms
t_{VALPK_WD}	Time Duration to Force Valley/Peak Count Logic if Valley or Peak is not Detected, (Note 2) (NCP1399AA) (NCP1399AC)	12, 14	 9.1 4.6	 10.2 5.12	 11.3 5.63	µs
t_{QS_timer}	Quiet Timer Duration (NCP1399AA) (NCP1399AC)	12, 14	 − −	 30 10	 − −	ms
N_{QS_1Q4}	Number of Patterns Adjustment when Bust Period is Shorter than 1/4 of QS_timer Duration	12, 14	−	2	−	−
N_{QS_2Q4}	Number of Patterns Adjustment when Bust Period is Longer than 1/4 and Shorter than 2/4 of QS_timer Duration	12, 14	−	1	−	−
N_{QS_3Q4}	Number of Patterns Adjustment when Bust Period is Longer than 2/4 and Shorter than 3/4 of QS_timer Duration	12, 14	−	0	−	−
N_{QS_4Q4}	Number of Patterns Adjustment when Bust Period is Longer than 3/4 and Shorter than 4/4 of QS_timer Duration (NCP1399AA) (NCP1399AC)	12, 14	 − −	 −2 −1	 − −	−
N_{QS_INF}	Number of Patterns Adjustment when Bust Period is Longer than QS_timer Duration (NCP1399AA) (NCP1399AC)	12, 14	 − −	 −4 −2	 − −	−

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{CC} = 12 V unless otherwise noted) (continued)

Symbol	Parameter	Pin	Min	Typ	Max	Unit
QUIET−SKIP						
$N_{PATTERN\_INIT}$	Initial Number of Patterns Placed when LL or Skip Mode is Activated	12, 14	–	1	–	–
N_{LL_BLANK}	Number of MU Pulses During which FB_LL_IN cmp is Blanked Once VFB > $V_{FB\_LL\_OUT}$ (NCP1399AA) (NCP1399AC)	14	 – –	 50 60	 – –	–
V_{CS_ZCD}	Voltage on CS in when Last ML is Terminated Earlier than Preselected Portion (NCP1399AA) (NCP1399AC)	6, 12	 −0.21 0.14	 −0.13 0.27	 −0.05 0.32	V
FB FREEZE INPUT						
I_{FB_FREEZE}	FB Freeze Pin Current Source	4	18	20	22	μA
$C_{FB\_FREEZE\_LOAD\_MAX}$	Maximum Loading Capacitance for FB Freeze Pin Voltage Filtering (Note 2)	4	–	–	10	nF
FAULTS AND AUTO−RECOVERY TIMER						
t_{TON_MAX}	Maximum On−time Clamp, (Note 2)	12, 14	8.6	9.6	10.6	μs
$N_{TON\_MAX\_COUNTER}$	Number of TON_MAX Events to Confirm Fault (NCP1399AA)	12, 14	–	2	–	–
V_{FB_FAULT}	FB Voltage when FB Fault is Detected (NCP1399AA) (NCP1399AC)	5	 2.21 4.42	 2.31 4.62	 2.45 4.89	V
$t_{FB\_FAULT\_TIMER}$	FB Fault Timer Duration, (Note 2) (NCP1399AA) (NCP1399AC)	–	 72 216	 80 240	 100 312	ms
V_{CS_FAULT}	CS Voltage when CS Fault is Detected (NCP1399AA) (NCP1399AC)	6	 2.2 2.28	 2.4 2.48	 2.6 2.68	V
N_{CS_FAULT}	Number of CS_fault cmp. Pulses to Confirm CS Fault	–	–	5	–	–
$K_{RC\_GAIN\_INC}$	Increment of Ramp Compensation Gain when VCS_FAULT is Reached (NCP1399AA) (NCP1399AC)	5, 6	 – –	 50 17	 – –	%
$N_{CS\_FAULT\_DEC}$	Number of Drive Pulses to Start Decrement of CS Fault Counter	5, 6	–	60	–	–
t_{DT_MAX}	Maximum Dead−time Value if No dV/dt Falling/Rising Edge is Received, (Note 2) (NCP1399AA) (NCP1399AC)	12, 14	 1350 720	 1500 800	 1650 880	ns
N_{DT_MAX}	Number of DT_MAX Events to Enters IC into Fault	12, 14, 16	–	–	–	–
t_{A-REC_TIMER}	Auto−recovery Duration (Common Timer for All Fault Condition), (Note 2) (NCP1399AA) (NCP1399AC)	–	 0.9 2.7	 1.0 3.0	 1.1 3.3	s
BROWN−OUT PROTECTION						
V_{BO}	Brown−out Turn−off Threshold	3	0.96	1.000	1.04	V
I_{BO_DOWN}	Brown−out Pull Down (Hysteresis) Current, (V_{VBULK/PFC_FB} < V_{BO}) (NCP1399AA) (NCP1399AC)	3	 – 4	 0 5	 – 6	μA
V_{BO_HYST}	Brown−Out Comparator Hysteresis	3	–	12	30	mV
$I_{BO\_LEAKAGE}$	Brown−Out Input Bias Current	3	–	–	100	nA
t_{BO_FILTER}	BO Filter Duration, (Note 2) (NCP1399AA) (NCP1399AC)	3	 451 46	 500 50	 628 65	μs

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{CC} = 12 V unless otherwise noted) (continued)

Symbol	Parameter	Pin	Min	Typ	Max	Unit
BROWN−OUT PROTECTION						
t_{BO_BLANK}	BO Blank Duration, (Note 2) (NCP1399AA) (NCP1399AC)	3	 1.8 9	 2.0 10	 2.2 11	ms
R_{BO_SW}	BO Pin Pull Down Switch On−state Resistance, V_{BO} = 1 V	3	0.7	1.1	2	Ω
$t_{BO\_SW\_ONESHOT}$	BO Pin Pull Down Switch On−state Duration (when Communication with PFC Controller Enabled) (NCP1399AA)	3	90	100	125	μs
RAMP COMPENSATION						
RC_{GAIN}	Ramp Compensation Gain (NCP1399AA) (NCP1399AC)	−	 83 56	 118 88	 156 127	mV/μs
t_{RC_SHIFT}	Ramp Compensation Time Shift	−	−	0.16	−	μs
TEMPERATURE SHUTDOWN PROTECTION						
T_{TSD_ENTER}	Temperature Shutdown T_J Going Up	−	−	124	−	°C
$T_{TSD\_RELEASE}$	Temperature Shutdown T_J Going Down (NCP1399AA) (NCP1399AC)	−	 − −	 101 109	 − −	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Guaranteed by design.
3. Minimal resistance connected in series with bootstrap diode is 3.3 Ω.

IC OPTIONS

Option	FB Mode	FB Fault	FB Fault at SS	FB Fault Peak	Cumulative FB Fault	CS Fault	CS Fault at SS	Cumulative CS Fault
NCP13994AA	Voltage	Auto−recovery	OFF	OFF	OFF	Auto−recovery	OFF	ON
NCP13994AC	Voltage	Auto−recovery	OFF	OFF	OFF	Auto−recovery	ON	OFF

Option	TON_MAX	OVP	OTP	OVP/OTP Bias at Skip	VCC_OFF Fault	Dead Time Control	Dead Time Fault	Dead Time Repeater
NCP13994AA	Auto−recovery	Auto−recovery	Auto−recovery	OFF	OFF	ZVS or DT_max	OFF	OFF
NCP13994AC	OFF	Latch	Auto−recovery	ON	OFF	ZVS or DT_max	OFF	OFF

Option	Line BO Status	Line OVP Status	X2 Cap. Discharger	Latch Release	BO Status	BO Skip Function	Dedicated Soft_start_seq	Start−up Watchdog
NCP13994AA	ON	ON	ON	X2 cap. disch.	ON	Switch	ON	ON with inc.
NCP13994AC	OFF	OFF	OFF	OFF	ON	OFF	ON	ON with inc.

Option	OCP_RC_INC	OCP_RC_INC at SS	Ramp Comp Status	Skip Mode	Quiet Skip Mode	ZCD at Quiet Skip	OFF−mode Status	PFCM Skip/ LL Status
NCP13994AA	ON	OFF	Without r. shift	Quiet Skip	Unipolar	ON	OFF	OFF
NCP13994AC	ON	OFF	Without r. shift	Quiet Skip	Unipolar	ON	OFF	OFF

TYPICAL CHARACTERISTICS

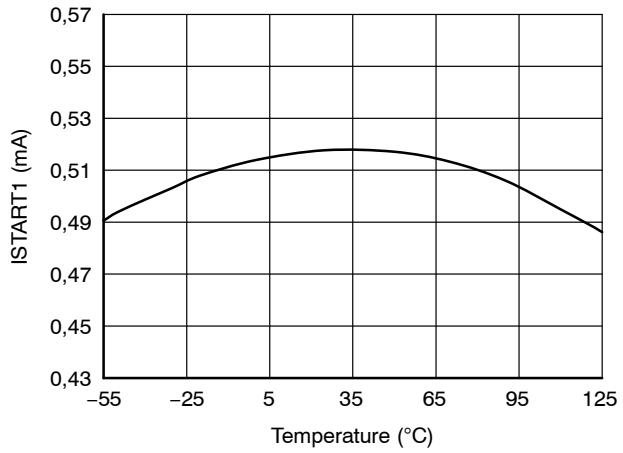


Figure 4. I_{START1} vs. Temperature

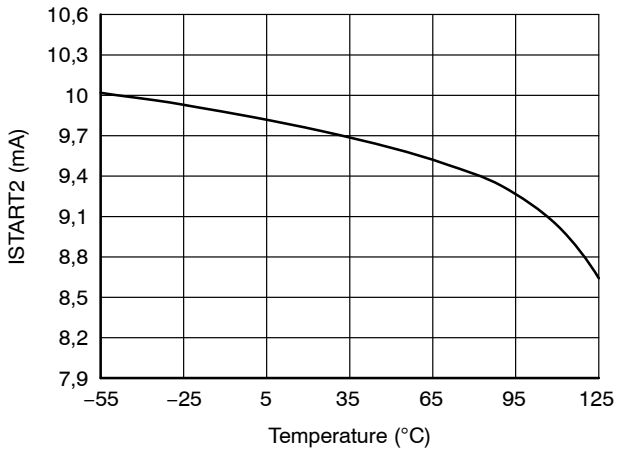


Figure 5. I_{START2} vs. Temperature

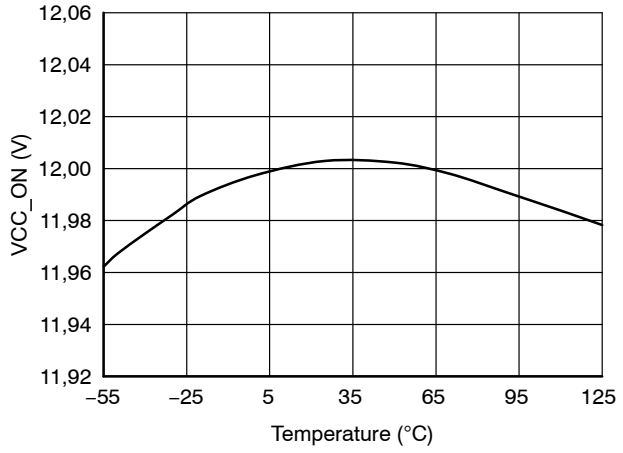


Figure 6. V_{CC_ON} vs. Temperature

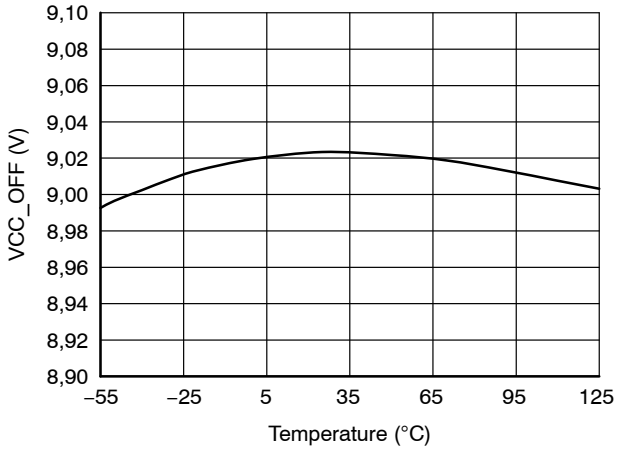


Figure 7. V_{CC_OFF} vs. Temperature

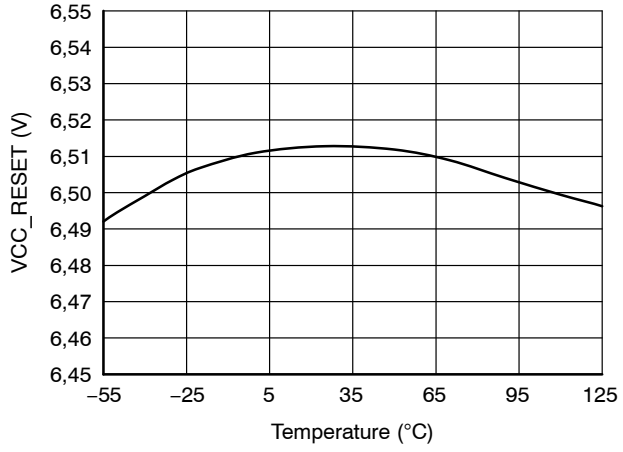


Figure 8. V_{CC_RESET} vs. Temperature

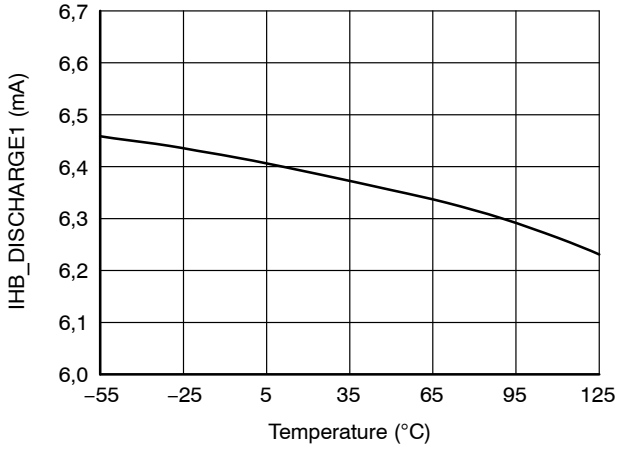


Figure 9. $I_{HB\_DISCHARGE1}$ vs. Temperature

TYPICAL CHARACTERISTICS (continued)

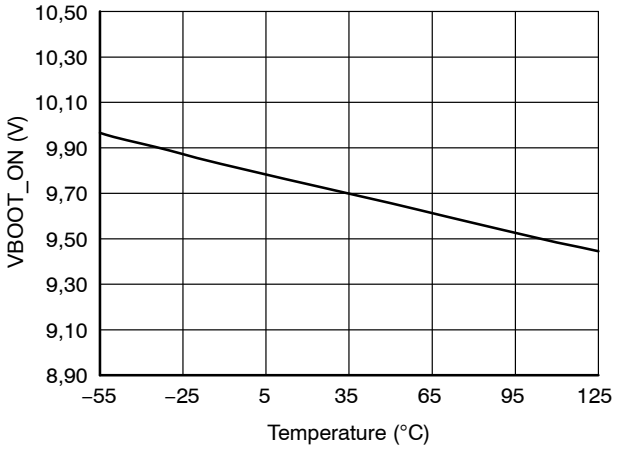


Figure 10. V_{BOOT_ON} vs. Temperature

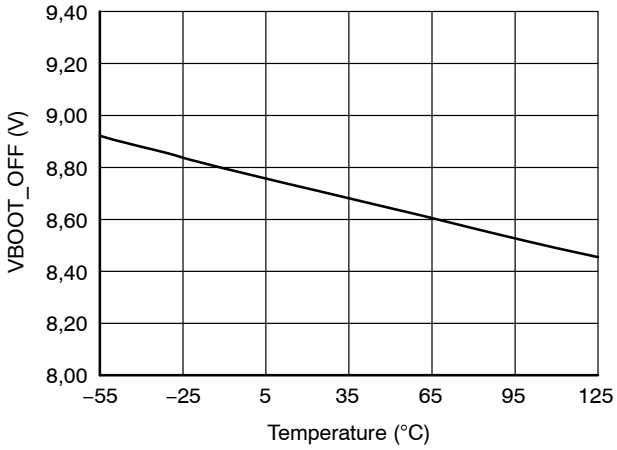


Figure 11. V_{BOOT_OFF} vs. Temperature

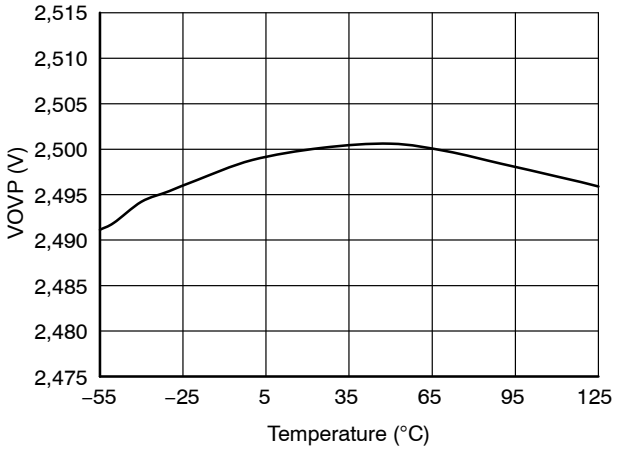


Figure 12. V_{OVP} vs. Temperature

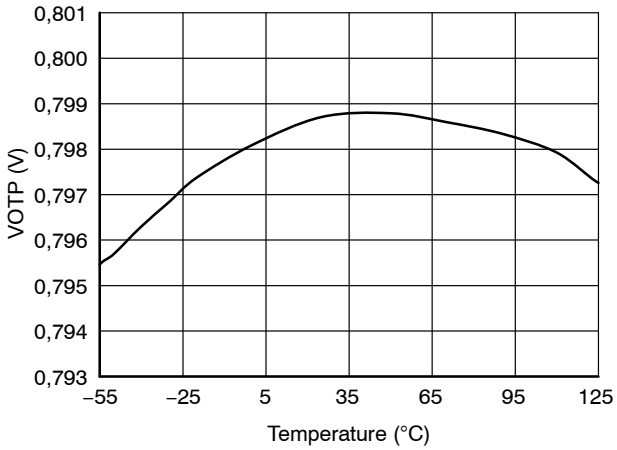


Figure 13. V_{OTP} vs. Temperature

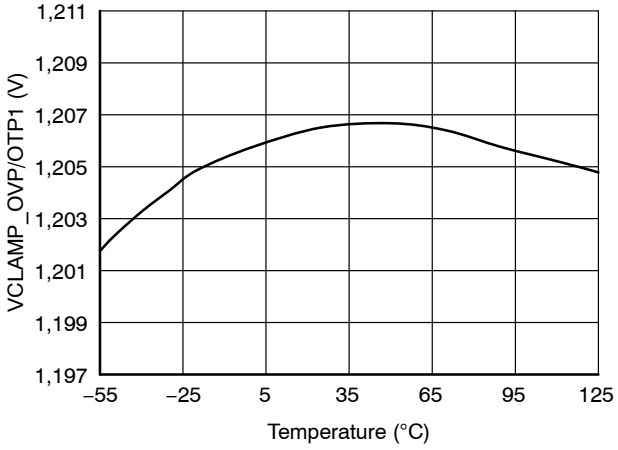


Figure 14. $V_{CLAMP\_OVP/OTP1}$ vs. Temperature

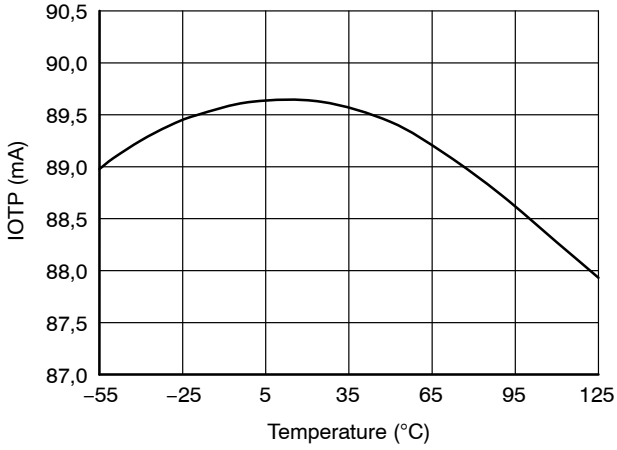


Figure 15. I_{OTP} vs. Temperature

TYPICAL CHARACTERISTICS (continued)

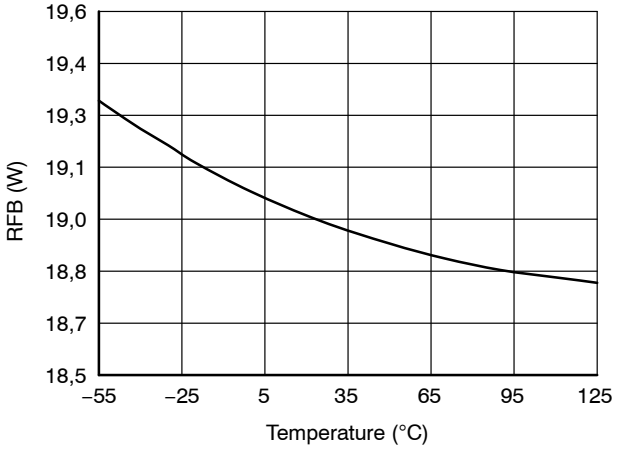


Figure 16. R_{FB} vs. Temperature

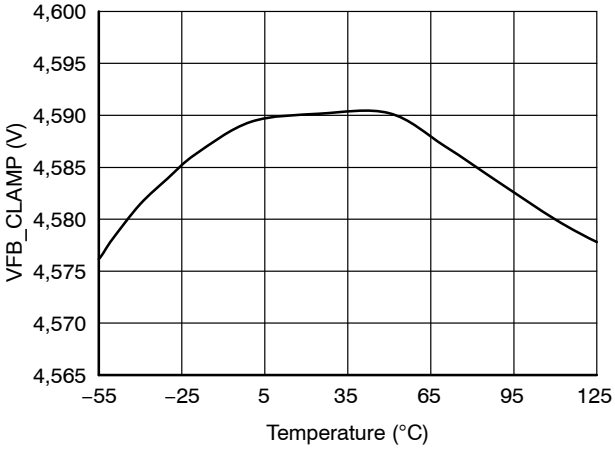


Figure 17. V_{FB_CLAMP} vs. Temperature

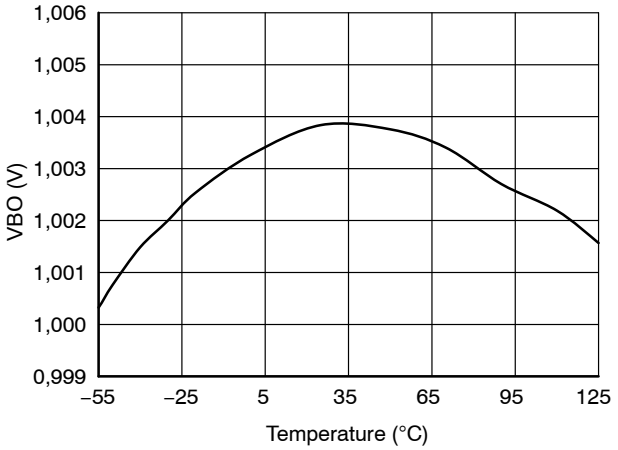


Figure 18. V_{BO} vs. Temperature

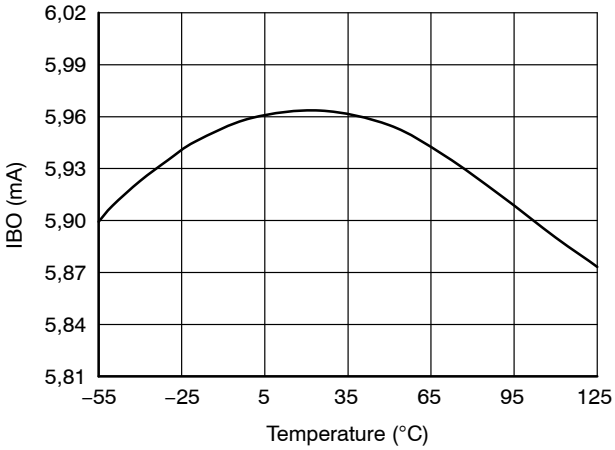


Figure 19. I_{BO} vs. Temperature

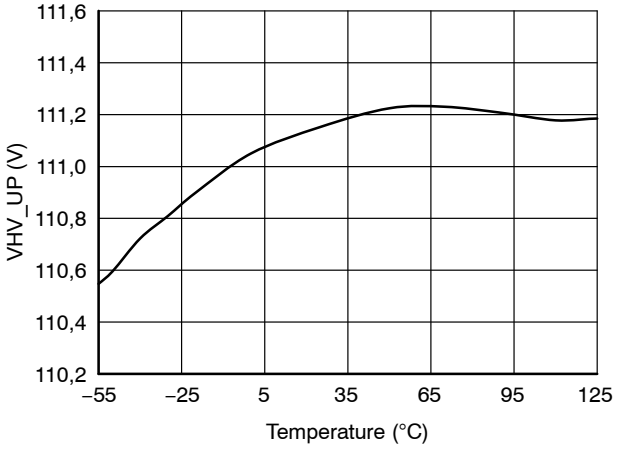


Figure 20. V_{HV_UP} vs. Temperature

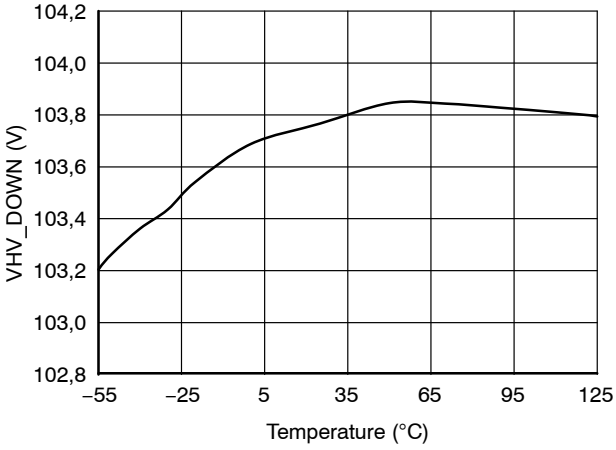


Figure 21. V_{HV_DOWN} vs. Temperature

VCC Management with High−voltage Startup Current Source

The NCP13994 controller features a HV startup current source that allows fast startup time and extremely low standby power consumption. Two startup current levels (I_{start1} and I_{start2}) are provided by the system for safety in case of short circuit between VCC and GND pins. In addition, the HV startup current source features a dedicated over−temperature protection to prevent IC damage for any failure mode that may occur in the application. The HV startup current source is primarily enabled or disabled based on V_{CC} level. The startup HV current source can be also enabled by BO_OK rising edge, auto−recovery timer end, off−mode and TSD end event. The HV startup current source charges the VCC capacitor before IC start−up.

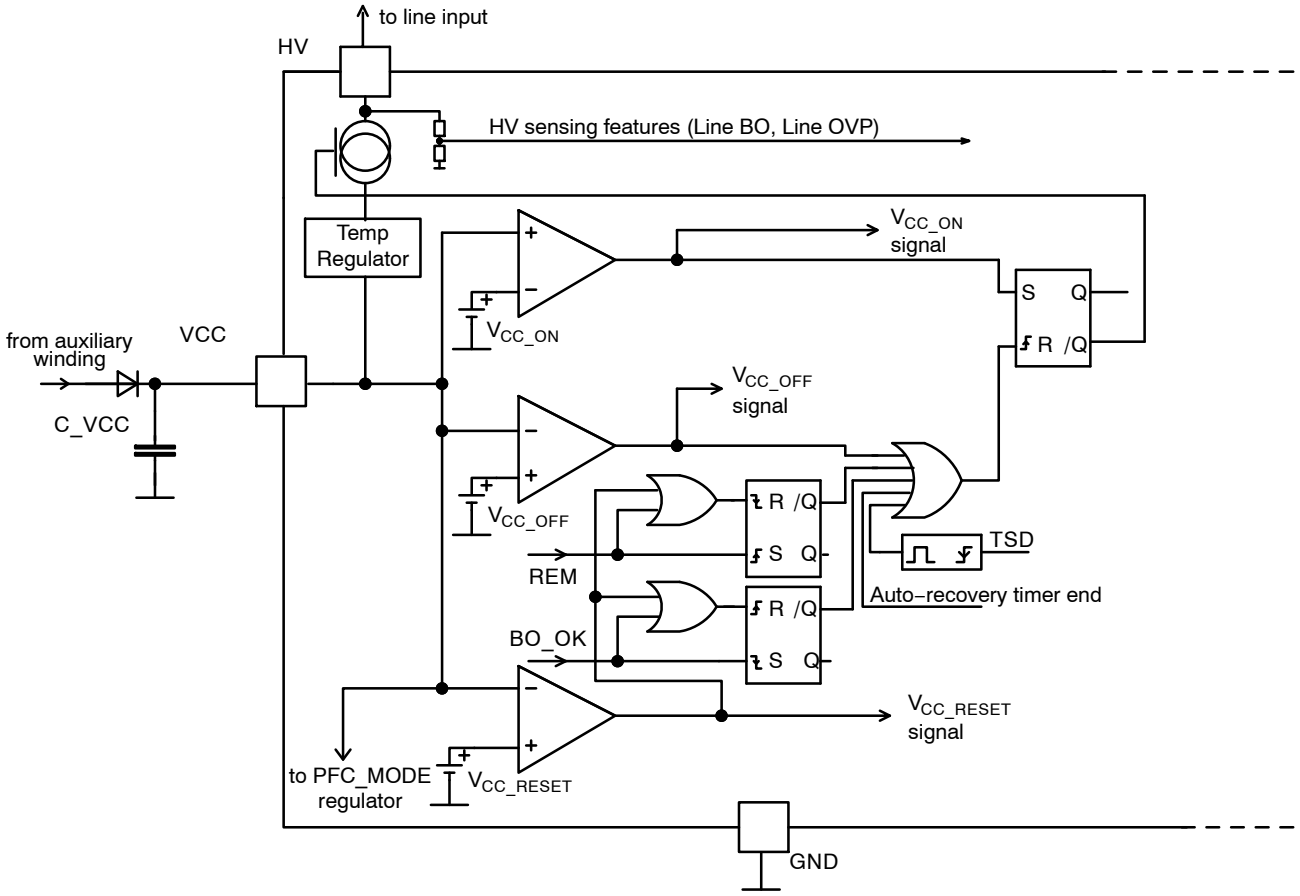


Figure 22. Internal Connection of the VCC Management Block

The NCP13994 controller disables the HV startup current source once the VCC pin voltage level reaches V_{CC_ON} threshold – refer to Figure 22. The application then starts operation and the auxiliary winding maintains the voltage bias for the controller during normal and skip−mode operating modes. The IC operates in so called Dynamic Self Supply (DSS) mode when the bias from auxiliary winding is not sufficient to keep the V_{CC} voltage above V_{CC_OFF} threshold (i.e. V_{CC} voltage is cycling between V_{CC_ON} and V_{CC_OFF} thresholds with no driver pulses on the output during positive V_{CC} ramp). The HV source is also operated in DSS mode when the low voltage controller enters off−mode or fault−mode operation. In this case the VCC pin voltage will cycle between V_{CC_ON} and V_{CC_OFF} thresholds and the controller will not deliver any driver pulse – waiting for return from the off−mode or latch mode operation. Please refer to figures Figure 53 through Figure 56 to find an illustration of the NCP13994 VCC management system under all operating conditions/modes.

The HV startup current source features an independent over−temperature protection system to limit I_{start2} current when the die temperature reaches $T_{HV\_CS\_CLAMP}$. At this temperature,I_{start2} will be progressively regulated to prevent the die temperature from rising above $T_{HV\_CS\_CLAMP}$.

Brown−out Protection − VBULK Input

Resonant tank of an LLC converter is always designed to operate within a specific bulk voltage range. Operation below minimum bulk voltage level would result in current and temperature overstress of the converter power stage. The NCP13994 controller features a VBULK input in order to precisely adjust the bulk voltage turn−ON and turn−OFF levels. This Brown−Out protection (BO) greatly simplifies application level design.

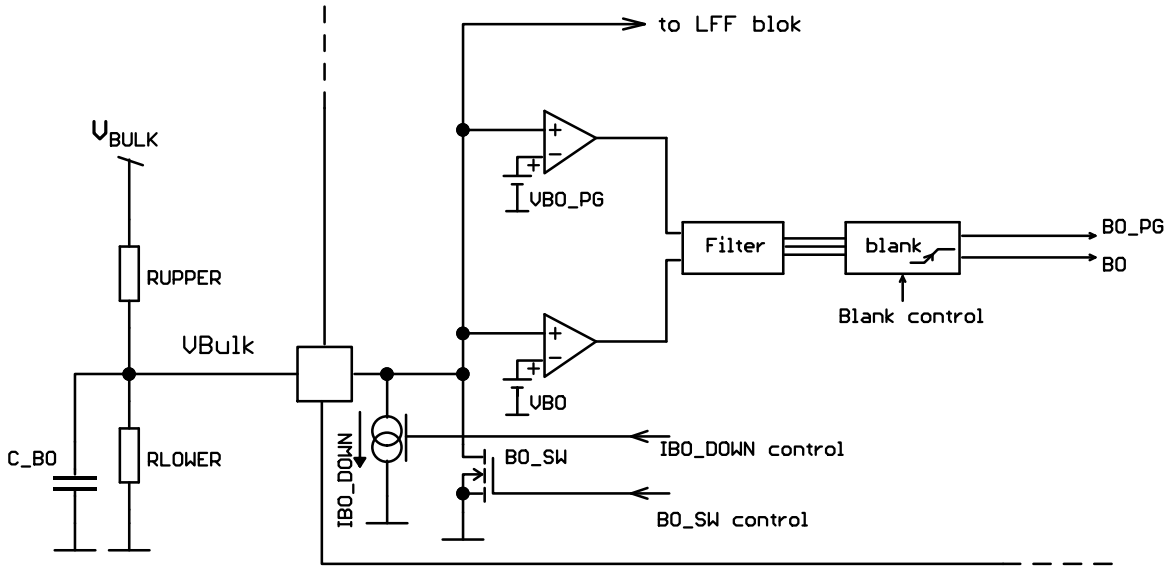


Figure 23. Internal Connection of the Brown−out Protection Block

The internal circuitry shown in Figure 23 allows monitoring the high−voltage input rail (V_{bulk}). A high−impedance resistive divider made of R_{upper} and R_{lower} resistors brings a portion of the V_{bulk} rail to the VBULK pin. The Current sink (I_{BO_DOWN}) is active below the *bulk voltage turn−on* level (V_{bulk_ON}). Therefore, the *bulk voltage* turn−on level is higher than defined by the division ratio of the resistive divider. To the contrary, when the internal BO_OK signal is high, i.e. the application is running, the I_{BO_DOWN} sink is disabled. The bulk voltage turn−off threshold (V_{bulk_OFF}) is then given by BO comparator reference voltage directly on the resistor divider. The advantage of this solution is that the V_{bulk_OFF} threshold precision is not affected by I_{BO_DOWN} (hysteresis) current sink tolerance.

The V_{bulk_ON} and V_{bulk_OFF} levels can be calculated using equations below:

The I_{BO_DOWN} is ON:

$$V_{BO} + V_{BOhyst} = V_{bulk\_ON} \cdot \frac{R_{lower}}{R_{lower} + R_{upper}} - I_{BO\_DOWN} \cdot \left(\frac{R_{lower} \cdot R_{upper}}{R_{Lowr} + R_{upper}} \right) \quad \text{(eq. 1)}$$

The I_{BO} is OFF:

$$V_{BO} = V_{bulk\_OFF} \cdot \frac{R_{lower}}{R_{lower} + R_{upper}} \quad \text{(eq. 2)}$$

One can extract R_{lower} term from equation 2 and use it in equation 1 to get needed R_{upper} value:

$$DR_{lower} = \frac{\frac{V_{bulk\_ON} \cdot V_{BO}}{V_{bulk\_OFF}} - V_{BO} - V_{BOhyst}}{I_{BO\_DOWN} \cdot \left(1 - \frac{V_{BO}}{V_{bulk\_OFF}}\right)} \quad \text{(eq. 3)}$$

$$R_{upper} = R_{lower} \cdot \frac{V_{bulk\_OFF} - V_{BO}}{V_{BO}} \quad \text{(eq. 4)}$$

Note that the VBULK pin is pulled down by an internal switch when the controller is in startup phase − i.e. when the V_{CC} voltage ramps up from $V_{CC} < V_{CC\_RESET}$ towards the V_{CC_OFF} level on the VCC pin. This feature assures that the VBULK pin voltage will not ramp up before the IC operation starts. The I_{BO_DOWN} hysteresis current sink is activated and BO discharge switch is disabled once the V_{CC} voltage crosses V_{CC_OFF} threshold. The VBULK pin voltage then ramps up naturally according to the BO divider information. The BO comparator then authorizes or disables the LLC stage operation based on the actual V_{bulk} level.

The low hysteresis current of the NCP13994 brown out protection system allows increasing the bulk voltage divider resistance and thus reduces the application power consumption during light load operation. On the other hand, the high impedance divider can be noise sensitive due to capacitive coupling to HV switching traces in the application. This is why a filter (t_{BO_FILTER}) is added after the comparator on Vbulk pin in order to increase the system noise immunity. Despite the internal filtering, it is also recommended to keep a good layout for BO divider resistors and use a small external filtering capacitor on the VBULK pin if precise BO detection wants to be achieved.

The bulk voltage divider can be disconnected by HV switch (controlled by signal from the PFC MODE pin) during off−mode operation. This technique further reduces the no−load power consumption down again since the power losses of voltage divider are not affected by the bulk voltage at all.

The NCP13994 is able to generate Power Good (PG) signal based on bulk capacitor voltage via BO_PG comparator sensing VBULK pin voltage.

The VBULK pin voltage is also used by Line Feed Forward block (LFF). Please refer to ON−time modulation and feedback loop block description for more information about LFF function.

The processed VBULK information are blanked when BO switch is activated or at specific events during bulk voltage modulation.

Please refer to Figure 53 through Figure 56 for an illustration of NCP13994 Brown−out protection system in all operating conditions/modes.

HV Sensing of Rectified AC Voltage

The NCP13994 features on its HV pin a true ac line monitoring circuitry. It includes a minimum start−up threshold, an auto−recovery line brown−out protection, line overvoltage protection and X2 capacitor discharge function. It is allowed only to work with an unfiltered, rectified ac input to ensure the X2 capacitor discharge function, which is described in following paragraph. The brown−out protection thresholds are internally selectable in specific steps, to fit most of the standard ac−dc conversion applications.

When the input voltage is below V_{HV_DOWN} for time longer then line brown−out timer duration (t_{HV}), a brown−out condition is detected, and the controller stops generate drives pulses. The HV current source maintains V_{CC} between V_{CC_ON} and V_{CC_OFF} levels until the input voltage is back above V_{HV_UP}.

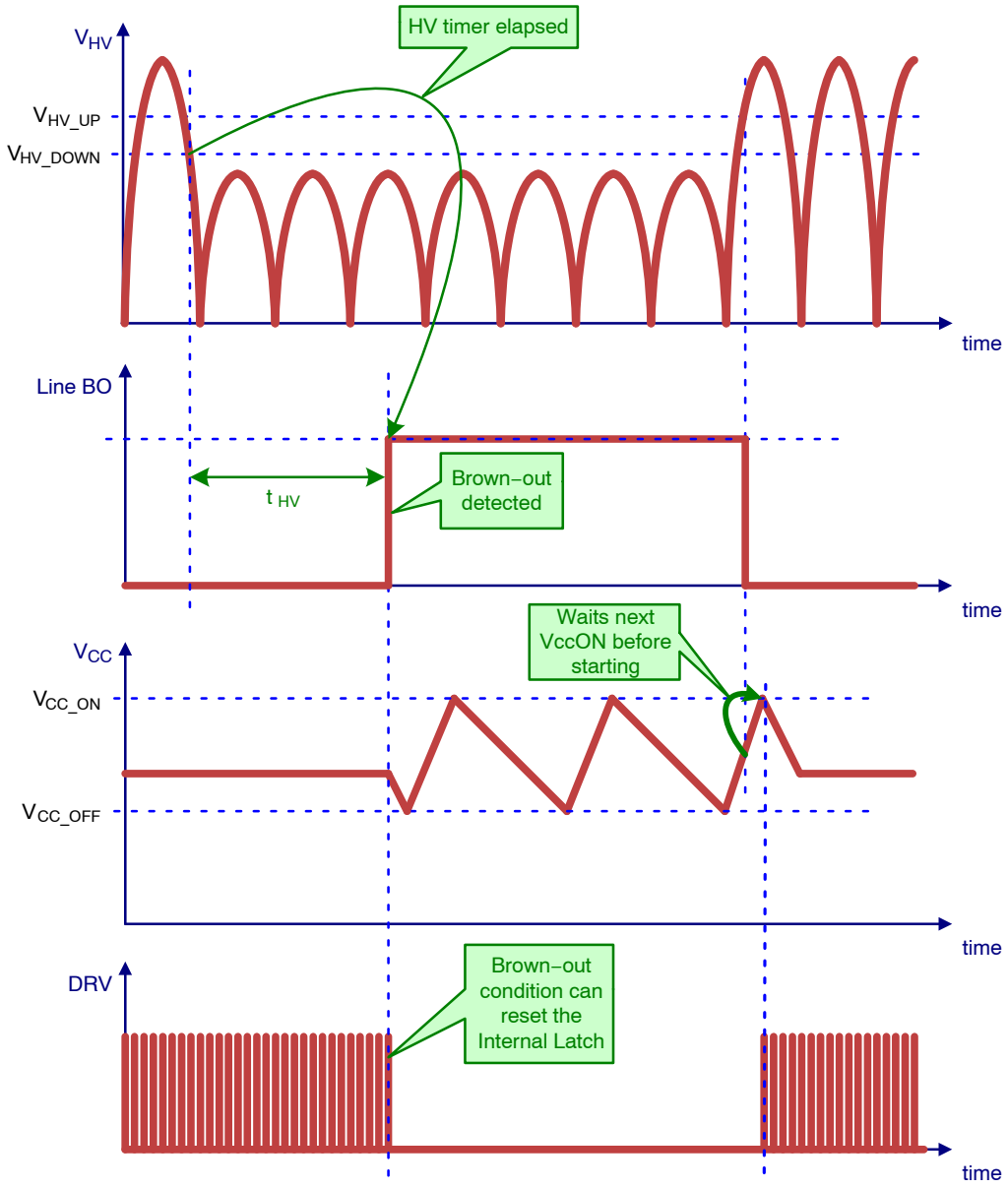


Figure 24. Ac Line Drop−out Timing Diagram

When V_{HV} crosses the V_{HV_UP} threshold, the controller starts when the V_{CC} crosses the next V_{CC_ON} event. When it crosses V_{HV_DOWN}, it triggers a timer of duration t_{HV}, this ensures that the controller doesn't stop in case of line cycle drop−out. The device restart is disabled when parasitic spike is induced at HV pin by the residual energy in the EMI filter immediately after the device stop. The device restart is allowed only when system detects positive slope of input signal for 2 ms (two sample clocks used at X2 cap discharge logic). The basic principle is shown at Figure 25 with block diagram at Figure 26.

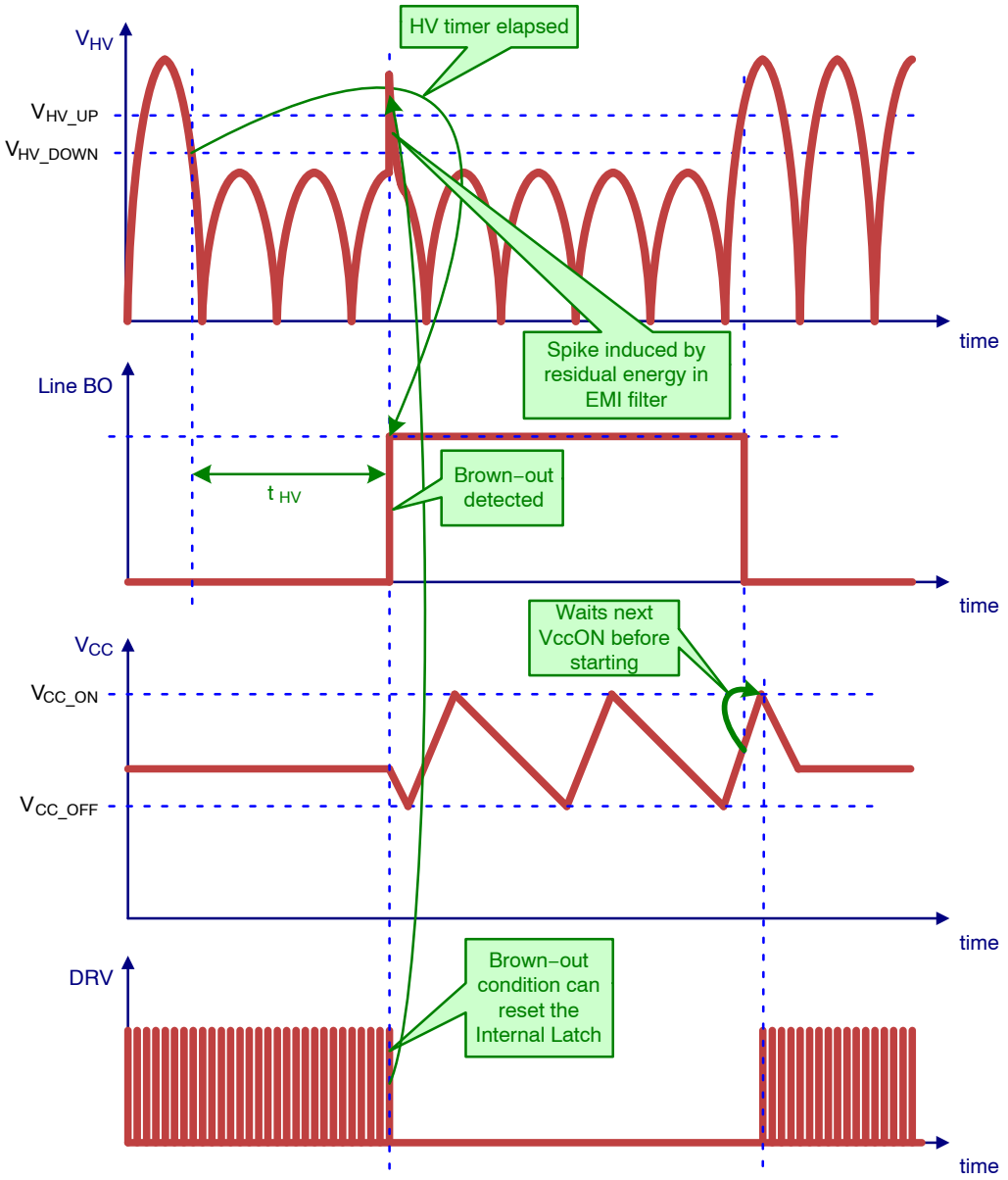


Figure 25. Ac Line Drop−out Timing Diagram with the Parasitic Spike

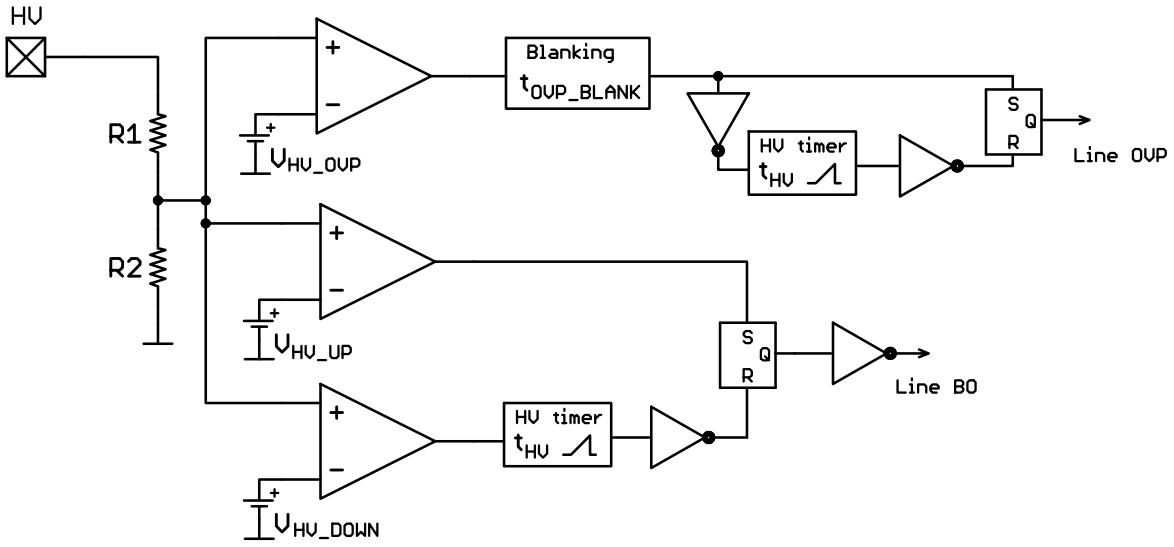


Figure 26. Brown−out and Line Overvoltage Detection Schematic

The same system is used for the Line OVP, except that this time the controller must not stop instantaneously when the input voltage goes above V_{HV_OVP}, in order to be insensitive to spikes and voltage surges shorter than t_{OVP_BLANK}. Therefore a blanking circuit is inserted after the output of the comparator.

When the overvoltage event occurs, Line OVP signal is set and controller stops generate pulses. When the overvoltage event finishes the timer with duration t_{HV} is reset and starts counting. The IC can starts after the timer elapses and all other start conditions are fulfil. The timer is paused and afterwards reset if new Line OVP event occur during the timer counting process as is shown at Figure 27.

When the Line OVP fault ends (the timer elapses) and the input voltage is below V_{HV_DOWN} the controller does not starts and waits for another Brown−in event as is shown at Figure 28.

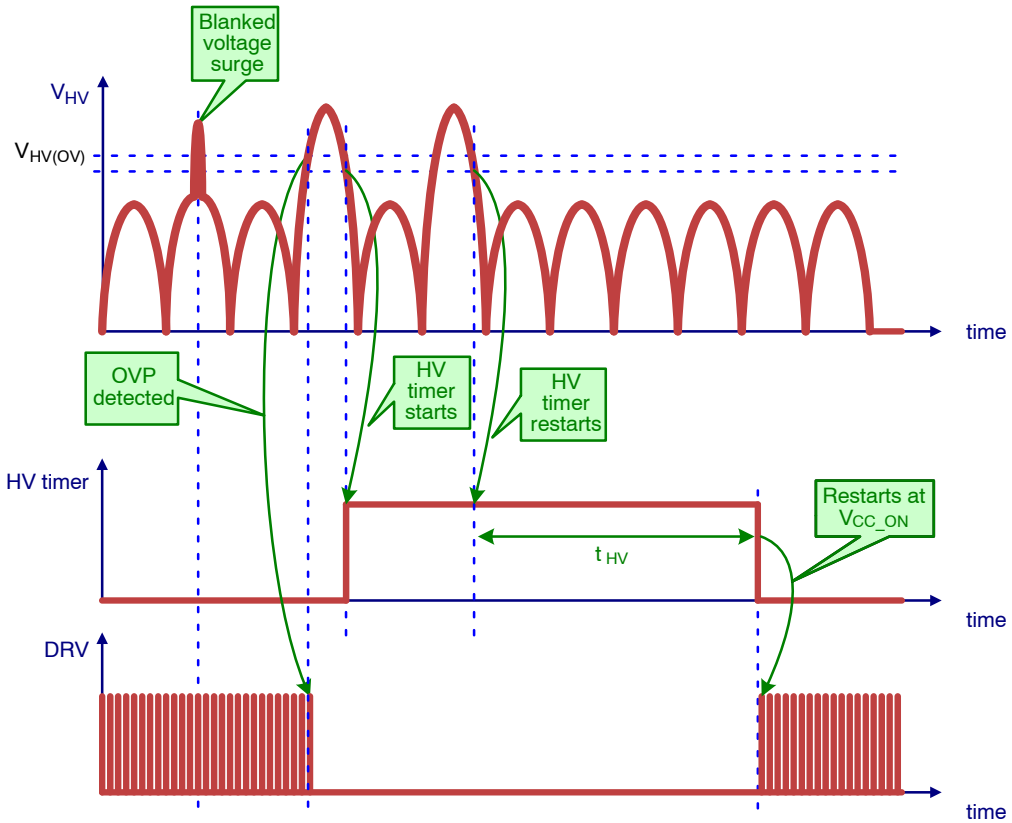


Figure 27. AC Input Line Overvoltage Timing Diagram

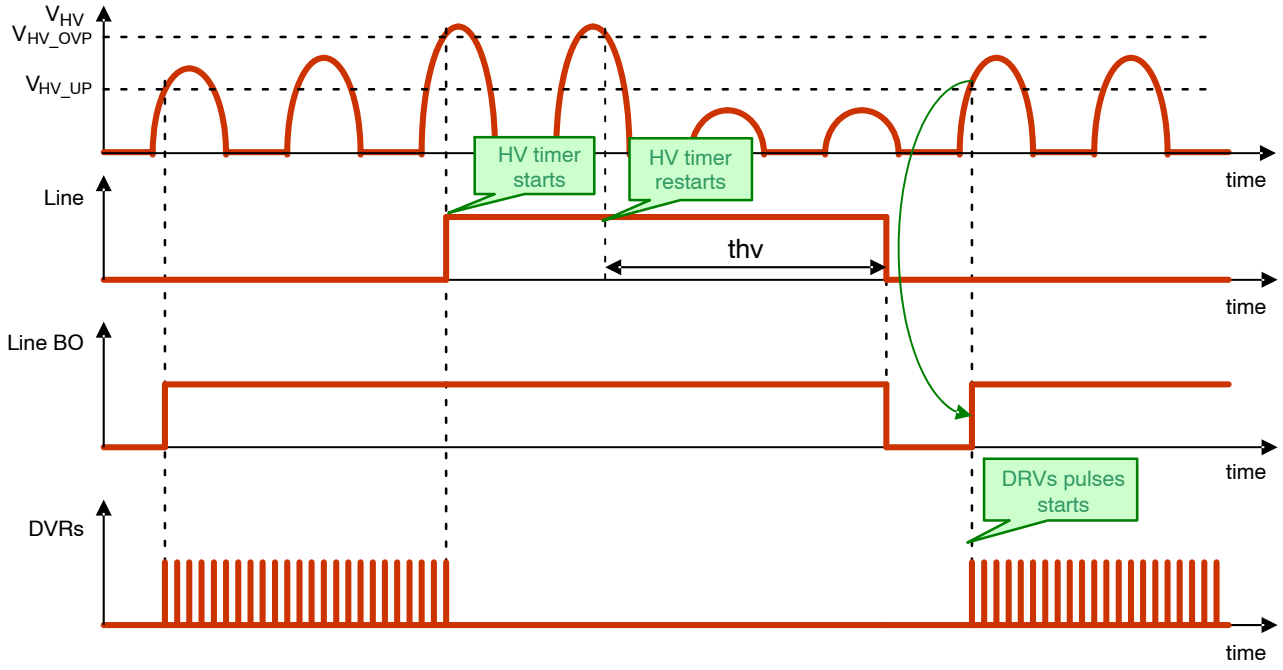


Figure 28. AC Input Line Overvoltage and Brown Out Common Timer Behavior Timing Diagram

X2 Cap Discharge Feature

This feature saves approximately 16 mW – 25 mW input power depending on the EMI filter X2 capacitors volume and it saves the external components count as well. The discharge feature is ensured via the start−up current source with a dedicated control circuitry for this function. The X2 capacitors are being discharged by current defined as I_{DISCH} when line disconnection is detected. The discharging current is lineary decreased based on HV pin voltage when the voltage decrease below about 40 V to allow higher value of external series resistor. The minimum discharging current is about 1 mA at V_{X2_END}.

There is used a dedicated structure called ac line unplug detector inside the X2 capacitor discharge control circuitry. See the Figure 29 for the block diagram for this structure and figures Figure 30, Figure 31, Figure 32 for the timing diagrams. The basic idea of ac line unplug detector lies in comparison of the direct sample of the high voltage obtained via the high voltage sensing structure with the delayed sample of the high voltage. The delayed signal is hold by the sample & hold structure.

The comparator used for the comparison of these signals is without hysteresis inside. The resolution between the slopes of the ac signal and dc signal is defined by the sampling time t_{SAMPLE} and additional internal offset V_{OS}. These parameters ensure the noise immunity. The additional offset is added to the image of the sampled HV signal and its analog sum is stored in the C_1 storage capacitor. If the voltage level of the HV sensing structure output crosses this level the comparator CMP output signal resets the detection timer (t_{X2_DET}) and positive slope of HV signal is detected. The negative slope is detected by similar way (the negative edge is detected for 10 ms from last detected positive edge only). The additional offset V_{OS} can be measured as the V_{HV_X2} on the HV pin. If the comparator output produces pulses it means that the positive or negative slope of input signal is present. If the comparator output stays at low or high level it means that the slope of input signal is lower than set resolution level. There is used the detection timer which is reset by any edge of the comparator output. If no edge comes before the timer elapses then only dc signal or signal with the small ac ripple is present at the HV pin. This type of the ac detector detects both positive and negative voltage slope, which fulfils the requirements for the ac line presence detection.

In case of the dc signal presence on the high voltage input, the direct sample of the high voltage obtained via the high voltage sensing structure and the delayed sample of the high voltage are equivalent and the comparator produces the low level signal. No edges are present at the output of the comparator, that's why the detection timer is not reset and dc detect signal appears.

The minimum detectable slope by this ac detector is given by the ration between the maximum hysteresis observed at HV pin $V_{HV\_X2,max}$ and the sampling time:

$$S_{min} = \frac{V_{HV\_X2,max}}{t_{SAMPLE}} \quad \text{(eq. 5)}$$

Than it can be derived the relationship between the detectable slope, the amplitude and frequency of the sinusoidal input voltage:

$$V_{max} = \frac{V_{HV\_X2,max}}{2 \cdot \pi \cdot f \cdot t_{SAMPLE}} \quad \text{(eq. 6)}$$

The X2 capacitor discharge feature is active under any controller operation mode to ensure SMPS users safety. The discharging process continues until the HV pin voltage dorops below V_{X2_END} level. *It is important to note that it is not allowed to connect HV pin to any dc voltage, e.g. directly to bulk capacitor.*

The controller operation is terminated and V_{CC} voltage is droping due to IC consumption during the X2 discharging process. The device start−up is blocked by the discharge sequence.

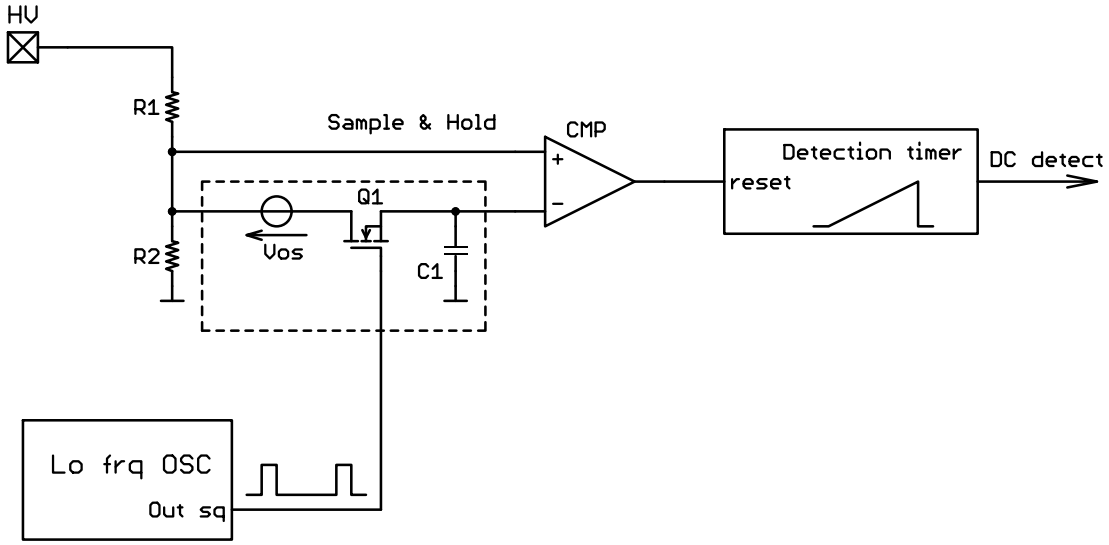


Figure 29. The Ac Line Unplug Detector Simplified Structure Used for X2 Capacitor Discharge System

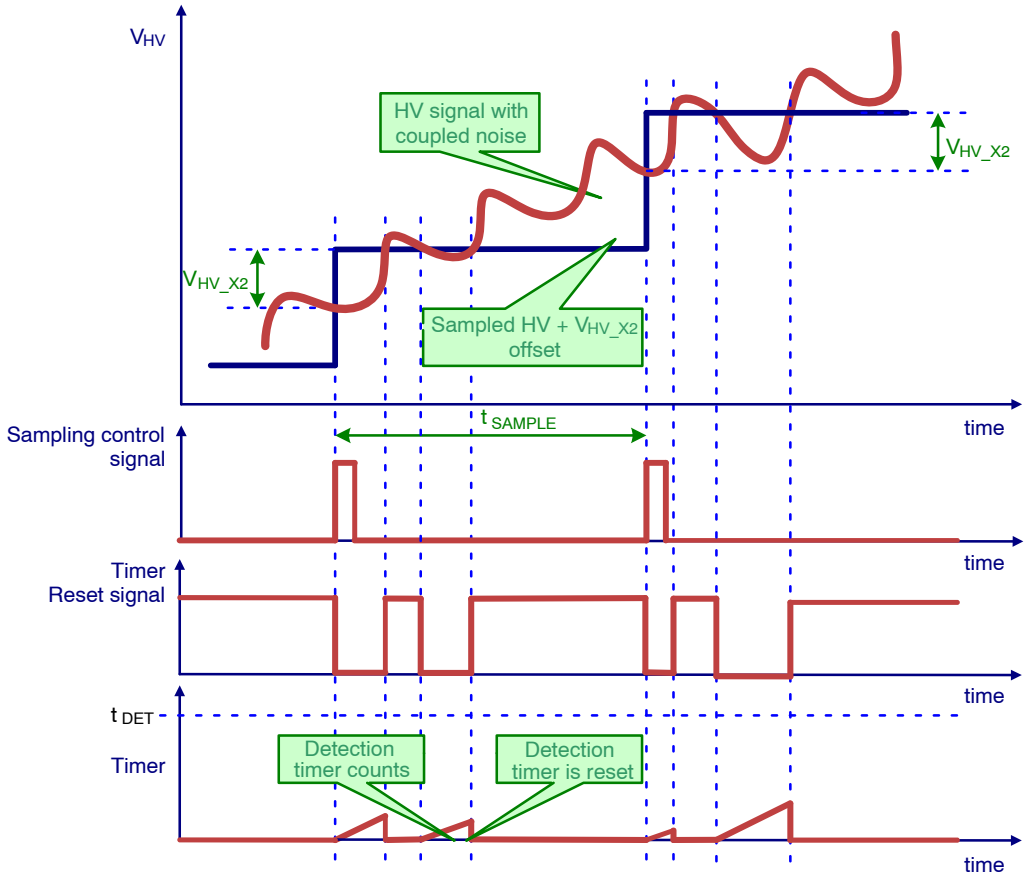


Figure 30. The Ac Line Unplug Detector Timing Diagram Detail with Noise Effects

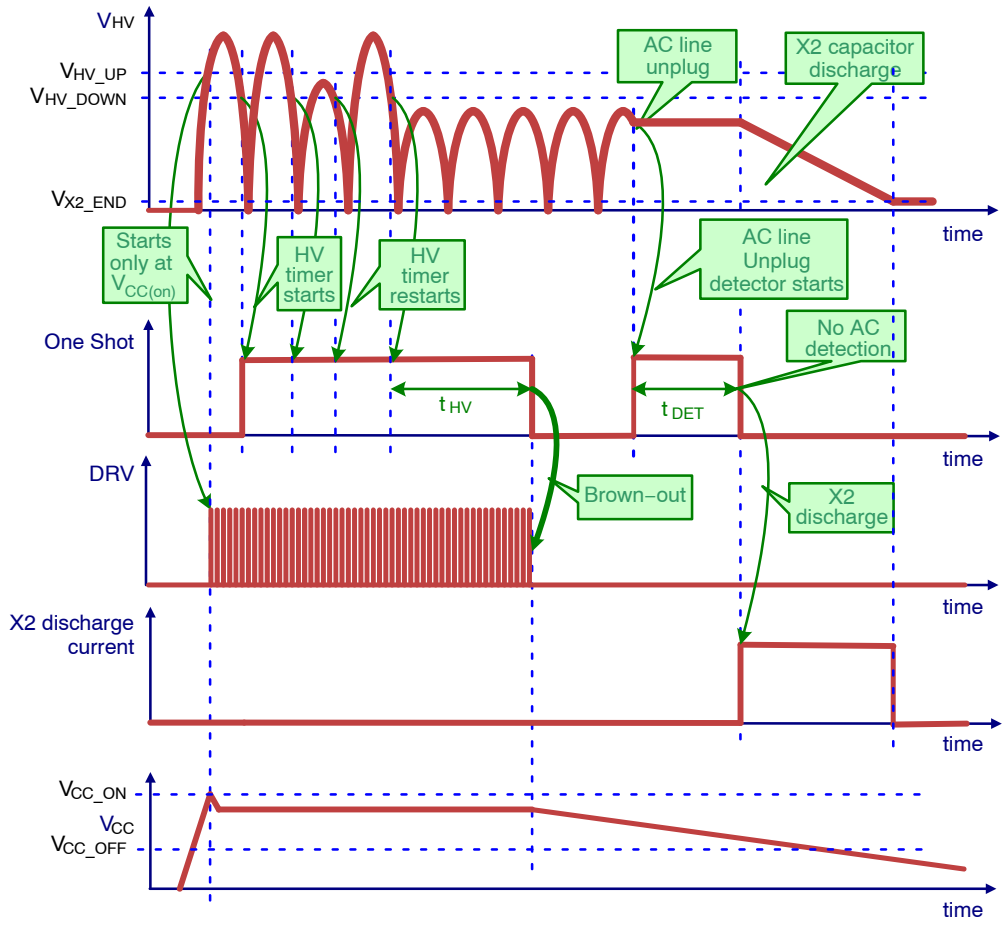


Figure 31. HV Pin Ac Input Timing Diagram with X2 Capacitor Discharge Sequence when the Application is Unplugged under Extremely Low Line Condition

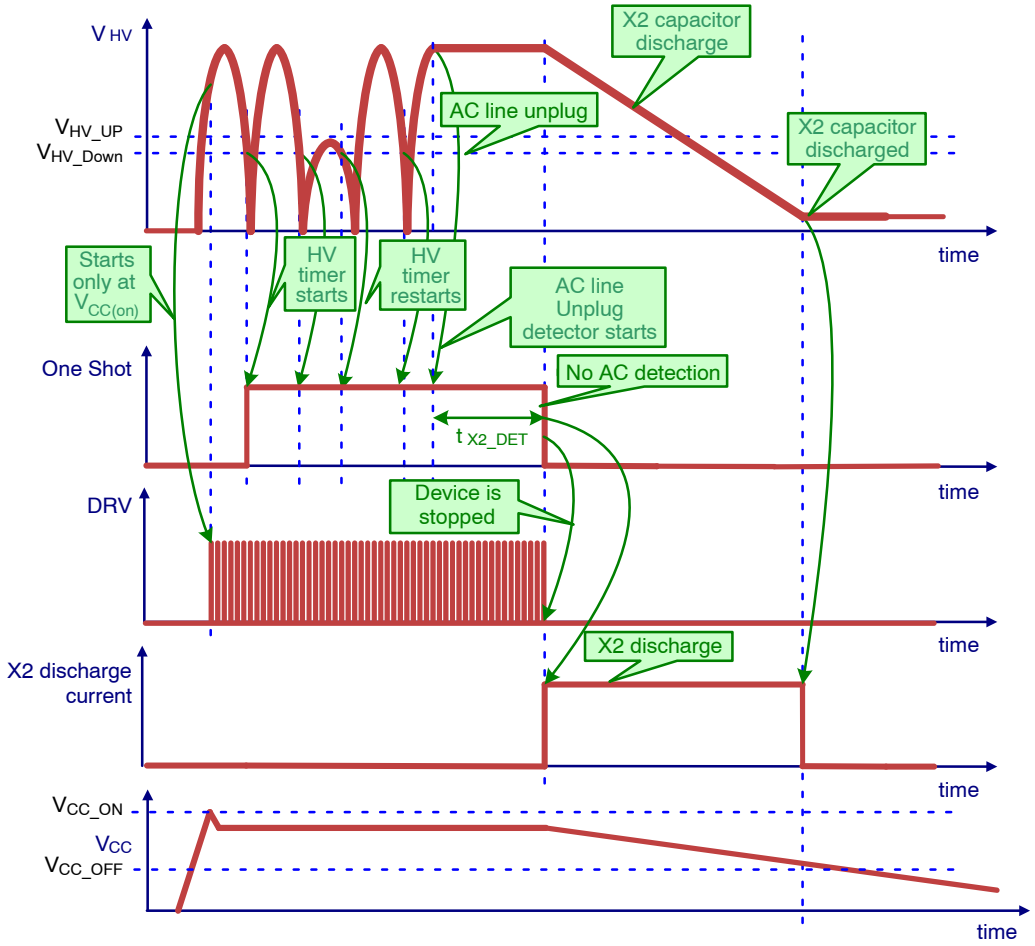


Figure 32. HV Pin Ac Input Timing Diagram with X2 Capacitor Discharge Sequence when the Application is Unplugged Under High Line Condition

Over−voltage and Over−temperature Protection

The OVP/OTP pin is a dedicated input to allow for a simple and cost effective implementation of two key protection features that are needed in adapter applications: over−voltage (OVP) and over−temperature (OTP) protections. Both of these protections can be either latched or auto−recovery − depending on the version of NCP13994. The OVP/OTP pin has two voltage threshold levels of detection (V_{OVP} and V_{OTP}) that define a no−fault window. The controller is allowed to run when OVP/OTP input voltage is within this working window. The controller stops the operation, after filter time delay, when the OVP/OTP input voltage is out of the no−fault window. The controller then either latches−off or or starts an auto−recovery timer − depending on the IC version − and triggered the protection threshold (V_{OTP} or V_{OVP}).

The internal current source I_{OTP} allows a simple OTP implementation by using a single negative temperature coefficient (NTC) thermistor. An active soft clamp composed from V_{clamp} and R_{clamp} components prevents the OVP/OTP pin voltage from reaching the V_{OVP} threshold when the pin is pulled up by the I_{OTP} current. An external pull−up current, higher than the pull−down capability of the internal clamp ($V_{CLAMP\_OVP/OTP}$), has to be applied to pull the OVP/OTP pin above V_{OVP} threshold to activate the OVP protection. The t_{OVP_FILTER} and t_{OTP_FILTER} filters are implemented in the system to avoid any false triggering of the protections due to application noise and/or poor layout.

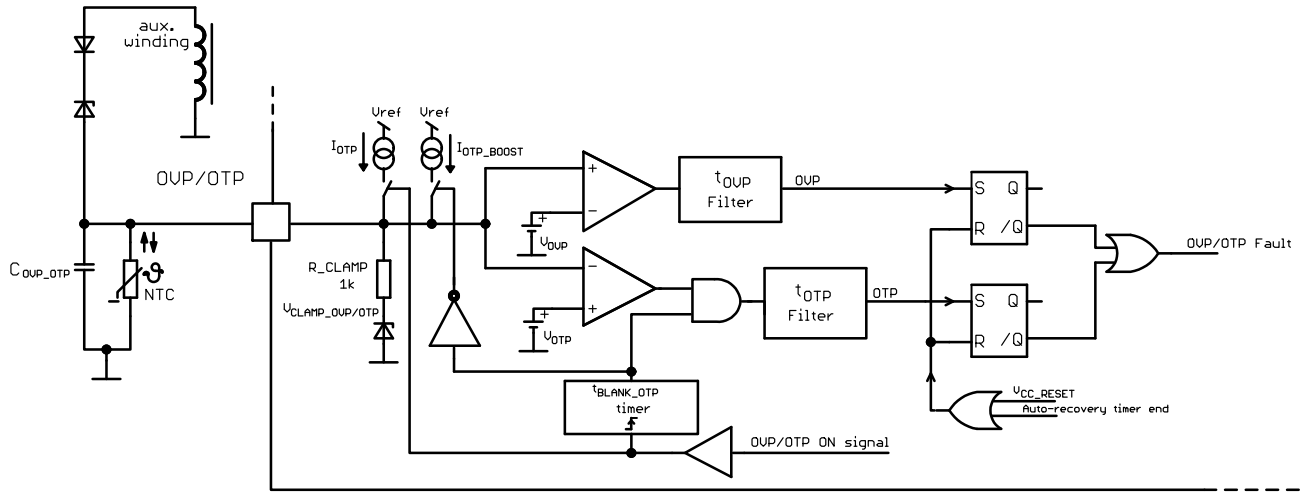


Figure 33. Internal Connection of OVP/OTP Input

The OTP protection could be falsely triggered during controller startup due to the external filtering capacitor charging current. Thus the t_{BLANK_OTP} period has been implemented in the system to overcome such behavior. The OTP comparator output is ignored during t_{BLANK_OTP} period. In order to speed up the charging of the external filtering capacitor C_{OVP_OTP} connected to OVP/OTP pin, the I_{OTP} current has been doubled to I_{OTP_BOOST}. The maximum value of filtering capacitor is 100 nF.

The OVP/OTP ON signal is set after the following events:

- the V_{CC} voltage exceeds the V_{CC_RESET} threshold during first start−up phase (after VCC pin voltage was below V_{CC_RESET} threshold)
- IC returns from non−switching states to switching state (like bulk BO, line BO, line OVP and VCC_OFF protections, auto−recovery...) except hysteretic mode of OTP protection

The I_{OTP} current source is disabled when:

- DRVs stop switching

IC option that keeps OVP/OTP block working during skip mode is also available. The IC consumption is increased for this version by OVP/OTP block bias.

OTP protection can operate (based on IC version) at hysteretic mode where DRVs are stopped when voltage on the pin drops below low threshold and operation is restarted once voltage on the pin increase above high threshold.

OTP condition is not process when IC restarted from off−mode state.

The latched OVP or OTP versions of NCP13994 enters latched protection mode when V_{CC} voltage cycles between V_{CC_ON} and V_{CC_OFF} thresholds and no pulses are provided by drivers. The controller VCC pin voltage has to be cycled down below V_{CC_RESET} threshold or appropriate conditions on HV pin have to occur in order to restart operation. This would happen when the power supply is unplugged from the mains.

Off−mode Control

The NCP13994 implements an ultra−low power consumption mode of operation called off−mode. The application output voltage is cycled between the nominal and lower levels that are defined by the secondary side off−mode controller (like NCP435x secondary off−mode controller). The output voltage is thus not regulated to nominal level but is always kept at a high enough voltage level to provide bias for the necessary circuits in the target application – for example this could be the case of microcontroller with very low consumption that handles VCC management in a notebook or TV. The no−load input power consumption could be significantly reduced when using described technique. The NCP13994 implements two different off−mode control system approaches:

- Active ON off−mode control
- Active OFF off−mode control

These two off−mode operation control techniques differ in the way the off−mode operation is started on the primary side controller. Both of these methods are described separately hereinafter.

Active ON Off−mode Control

The NCP13994 device family could use a SKIP/REM pin only for off−mode operation control– i.e. the pin is internally connected to the Active ON off−mode control block and the skip mode threshold level is not adjustable externally. The skip mode comparator threshold can be adjusted only internally (by IC option) in this option. The SKIP/REM pin when used for off−mode control allows the user to activate the ultra−low consumption mode during which the IC consumption is reduced to only very low HV pin leakage current ($I_{HV\_OFF-MODE}$) and very low VCC pin consumption ($I_{CC\_OFF-MODE}$). The off−mode is activated when SKIP/REM pin voltage exceeds V_{REM_OFF} threshold. Normal operating mode is resumed when SKIP/REM pin voltage drops below V_{REM_ON} threshold – refer to Figure 34 for an illustration.

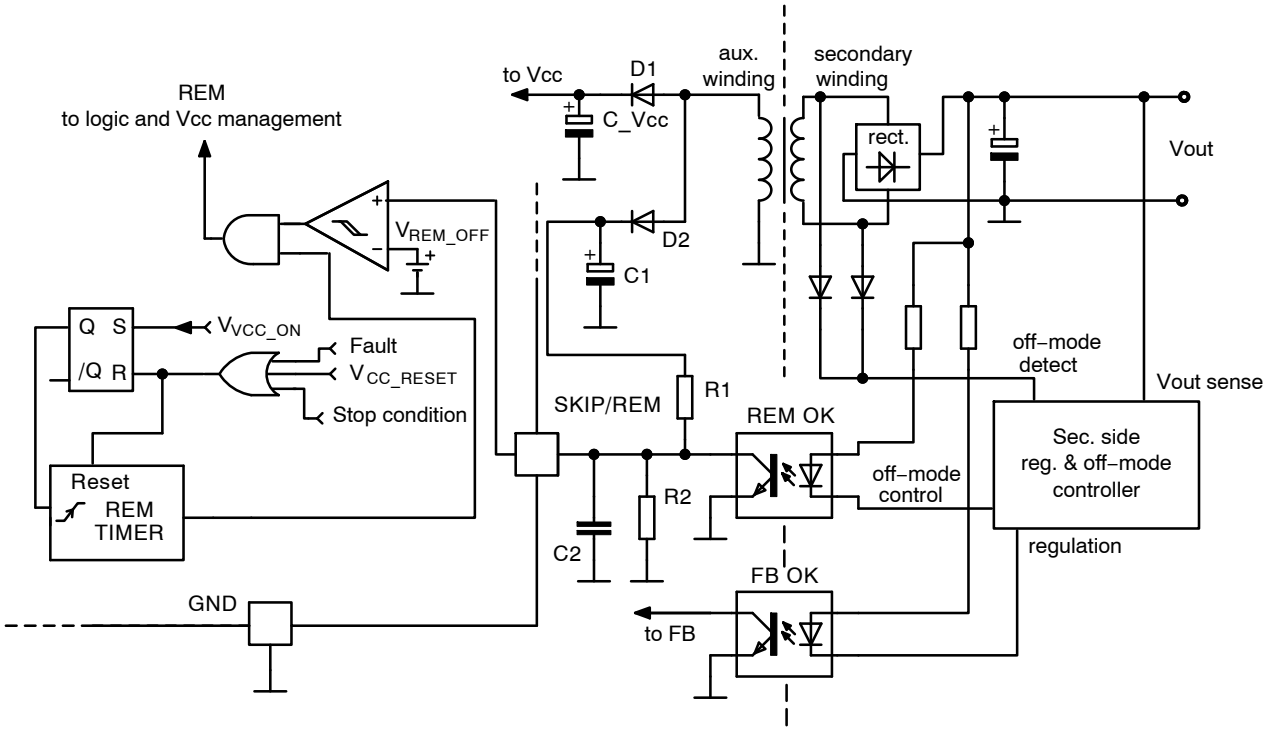


Figure 34. SKIP/REM Input Internal Connection – Active ON Version

The off−mode operation is activated by the secondary side off−mode controller. The auxiliary bias for primary side off−mode control is provided by a circuit composed from components D_2, C_1, R_1, R_2 and C_2. The SKIP/REM pin is pulled up by this auxiliary supply circuit once the REM optocoupler (REM OK) is released. The application then operates in off−mode until the secondary side off−mode controller activates the REM optocoupler or until the auxiliary bias on C_1 is lost. Normal operation mode is then recovered via power stage startup. The application is thus switching between ON−mode and OFF−mode states when off−mode control is implemented. The OFF mode period last significantly longer time (tens of seconds or more) compared to the secondary capacitor refilling period (few tens of milliseconds) – this explains why the no−load input power consumption can be drastically reduced. The auxiliary off−mode supply capacitor C1 can stay charged while the secondary bias is lost – this can happen during overload or other fault mode conditions. A REM TIMER is thus implemented in the system to allow fast application restart in such cases. The controller blanks the SKIP/REM input information for t_{REM_TIMER} time during controller restart so that the secondary side bias can be restored and the secondary off−mode controller can activate the REM optocoupler. This REM TIMER blank sequence is activated each time the VCC pin voltage reaches V_{CC_ON} threshold – except in the situation when after IC left off−mode operation by standard way and V_{CC} is restored – i.e. when the REM optocoupler is activated by the secondary off−mode controller. The controller is active for very short time during no−load conditions − just during the time needed to re−fill the secondary side capacitors to the nominal output voltage level. In this case we do not use REM TIMER because it would increase the no−load power consumption by forcing the application to run for a longer time than necessary.

The bias on VCC pin needs to be assured when off−mode operation takes place. The auxiliary winding is no more able to provide any bias thus the HV startup current source is operated in DSS mode – i.e. the VCC pin voltage is cycling between V_{CC_ON} and V_{CC_OFF} thresholds. This approach keeps IC biasing in order to memorize the current operation sate.

Active OFF Off−mode Control

The NCP13994 device family could use LLC FB pin voltage information for off−mode operation detection – refer to Figure 35. The SKIP/REM pin is internally connected to the skip mode block in this case and serves as a $V_{FB\_SKIP\_IN}$ threshold voltage adjust pin. The secondary off−mode controller reuses the LLC stage regulation optocoupler in order to reduce total system cost. The off−mode operation is initiated once the LLC FB pin is pulled down below $V_{FB\_REM\_OFF}$ threshold followed by the VCC pin voltage drop below V_{CC_OFF} threshold. The opto−coupler has to be active at all time the application is held in off−mode. No biased is then provided by the secondary off−mode controller during normal operation – this is why this approach is called Active OFF off−mode operation. The application no−load input power consumption is slightly higher compared to Active ON off−mode solution, previously described, because the opto−coupler needs to be biased during off mode operation.

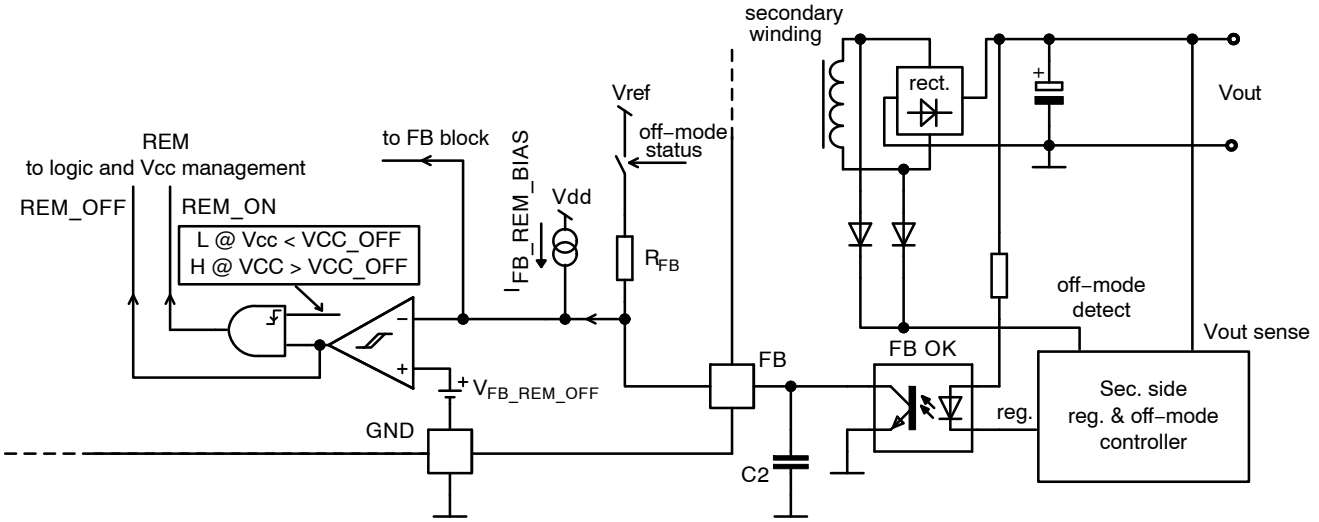


Figure 35. Active OFF Off−mode Internal Detection Based on the LLC FB Pin Voltage

The controller monitors the LLC FB pin voltage level and restarts via regular startup sequence (including VCC pin voltage ramp−up to V_{CC_ON} level and soft−start) once the FB pin is released by the secondary off−mode controller.

The HV startup current source is working in DSS mode during application off−mode operation – i.e. the VCC pin voltage is cycling between V_{CC_ON} and V_{CC_OFF} thresholds. This approach keeps IC biased so that the actual operation sate is memorized. The LLC FB pin pull−up resistor is disconnected and off−mode pull up current source $I_{FB\_REM\_BIAS}$ is activated when off−mode operation is activated in order to reduce IC power consumption and also needed current for opto−coupler driving from secondary side.

Please refer to Figure 56 for an illustration on how the NCP13994 off−mode system works under all operating conditions/modes.

PFC MODE Output

The NCP13994 has PFC MODE pin that can be used to control aditional circuit based on actual application operating state – please refer to Figure 36. The PFC MODE output pin can be used for two main purposes:

1st to control the PFC front stage controller operation

2nd to control PG optocoupler based on bulk capacitor voltage

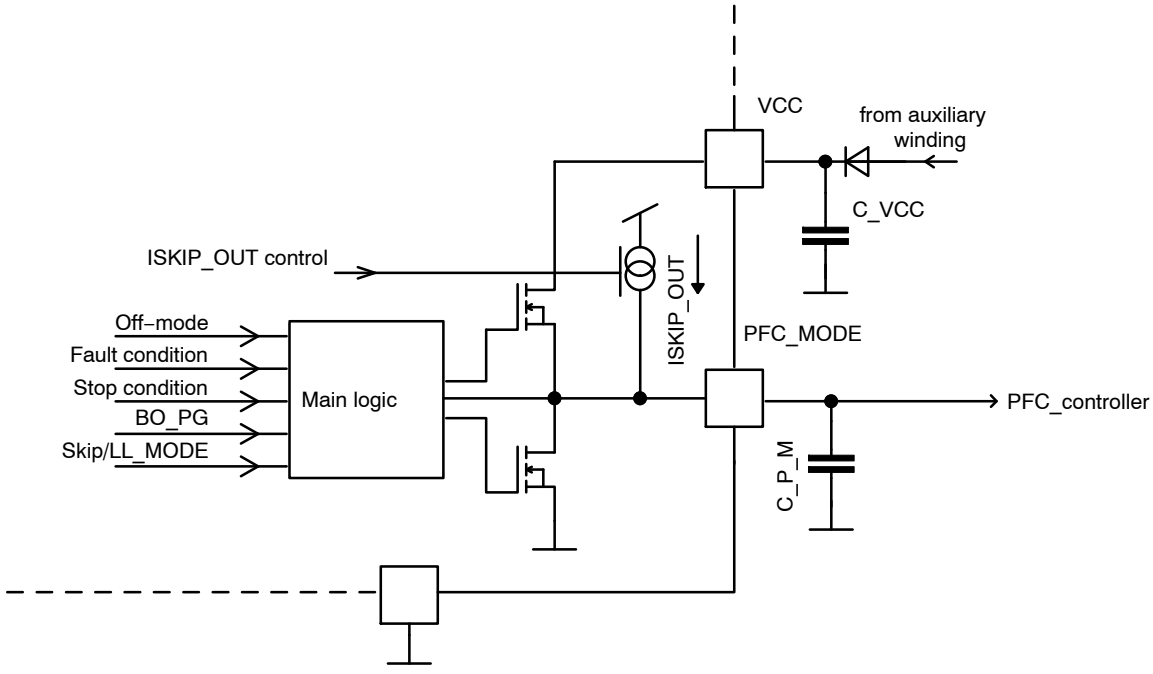


Figure 36. Internal Connection of the PFC MODE Block

There are three possible states of the PFC MODE output that can be placed by the controller based on the application operating conditions:

a. The PFC MODE output pin is pulled−down by an internal MOSFET switch before controller startup. This technique ensures minimum VCC pin current consumption in order to ramp V_{CC} voltage in a short time from the HV startup current source. This approach speeds up the startup and restart time of an SMPS. The PFC MODE output pin is also pulled−down in off−mode, protection mode and at stop conditions (except BO event via VBULK pin) during which the HV startup current source is operated in DSS mode. Application power consumption is reduced in above cases. The pull−down switch can be activate also in skip or light load mode (depends on IC version)

b. Second possible state of PFC MODE output is regulated voltage. The two regulated levels V_{REG1} and V_{REG2} are available. Regulation level V_{REG1} is present on the output during normal operation and IC can switch to V_{REG2} during skip or light−load modes. The purpose of switching between two voltage levels is to fully bias PFC controller during normal operation and keep limited bias (just below PFC controller VCC_off level) to keep PFC controller internal blocks biased with reduced consumption of PFC controller.

c. The PFC MODE can be also at High Z state during skip or light load mode to keep remaining charge of PFC controller VCC capacitor. The combination of High Z state with pull−down switch can be used to control Power Good (PG) opto−coupler.

The pin n.9 can be used for skip_out threshold level definition when PFC_MODE functions are not required or during application debugging.

Please refer to Figure 53 through Figure 56 for an illustration of NCP13994 PFC operation control.

ON−time Modulation and Feedback Loop Block

The NCP13994 on−time modulation uses current mode control scheme that ensures best transient response performance and provides inherent cycle−by−cycle over−current protection feature in the same time. The current mode control principle used in this device can be seen in Figure 37.

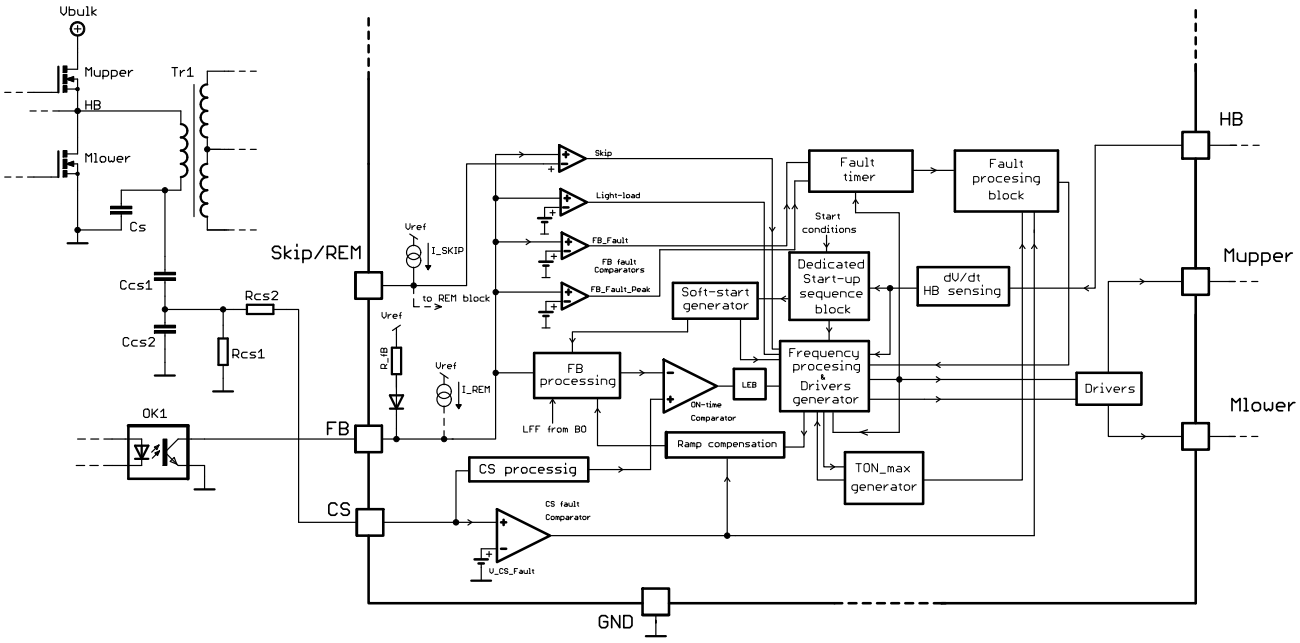


Figure 37. Internal Connection of the NCP13994 Current Mode Control Scheme

The basic principle of current mode control scheme implementation lies in the use of an ON−time comparator that defines upper switch on−time by comparing voltage ramp, derived from the current sense input voltage, to the divided or not divided feedback pin voltage. The upper switch on−time is then re−used for low side switch conduction period. The switching frequency is thus defined by the actual primary current and output load conditions. Digital processing with 10 ns minimum on−time resolution is implemented to ensure high noise immunity. The ON−time comparator output is blanked by the leading edge blanking (t_{LEB}) after the Mupper switch is turned−on. The ON−time comparator LEB period helps to avoid false triggering of the on−time modulation due to noise generated by the HB pin voltage transition.

The voltage signal for current sense input is prepared externally via natural primary current integration by the resonant tank capacitor Cs. The resonant capacitor voltage is divided down by capacitive divider (Ccs1, Ccs2, Rcs1, Rcs2) before it is provided to the CS input. The capacitive

divider division ratio, which is fully externally adjustable, defines the maximum primary current level that is reached in case of maximum feedback voltage – i.e. the capacitive divider division ration defines the maximum output power of the converter for given bulk voltage. The CS pin is a bipolar input where an input voltage swing is restricted to ±5 V. The CS pin signal is also used for secondary side short circuit detection – please refer to chapter dedicated to short circuit protection.

A fixed voltage offset is internally process to the FB pin signal in order to assure enough voltage margin for operation the feedback opto−coupler – the FB opto−coupler saturation voltage is ~0.15 V (depending on type). However, the CS pin useful signal for frequency modulation swings from 0 V, so current mode regulation would not work under light load conditions if no offset would be added.

The second input signal for the on−time comparator is derived from the FB pin voltage. This internal FB pin signal is also used for the following purposes: skip mode operation detection, Light−load mode detection, off−mode detection and overload / open FB pin fault detection. The detailed description of these functions can be found in each dedicated chapters. The internal pull−up resistor assures that the FB pin voltage increases when the opto−coupler LED becomes less biased – i.e. when output load is increased. The higher FB pin voltage implies a higher reference level for on−time comparator i.e. longer Mupper switch on−time and thus also higher output power. The FB pin features a precise voltage clamp which limits the internal FB signal during overload and startup. The FB pin signal passes through the FB processing block before it is brought to the ON−time comparator input. The FB processing block scales the FB signal down by a K_{FB} ratio in order to limit the CS input dynamic voltage range and apply ramp compensation signal (to ensure stability of the current mode control scheme), FB freeze or LFF. The processed internal FB signal could be overridden by a Soft−start generator output voltage during device starts−up.

The actual operating frequency of the converter is defined based on the CS pin and FB pin input signals. The maximum output power of the converter, under given input voltage, is limited by maximum internal FB voltage clamp that is reached when opto−coupler provides no current. The maximum output power limit is bulk voltage dependent due to changing ratio between magnetizing and load primary current components. Line Feed Forward (LFF) system is implemented in the controller to compensate for maximum output power clamp variation. The LFF signal that is apply to internal FB voltage is VBULK pin voltage proportional. The different input voltage sensed by VBULK pin creates change on internal FB signal. The Mupper switch on−time is thus changed to represent similar FB pin voltage at constant load across different input voltage. The LFF signal is provided only when BO pin voltage exceeds BO_OK threshold voltage.

Please refer to Figure 38 and below description for better understanding principle of the NCP13994 frequency modulation system.

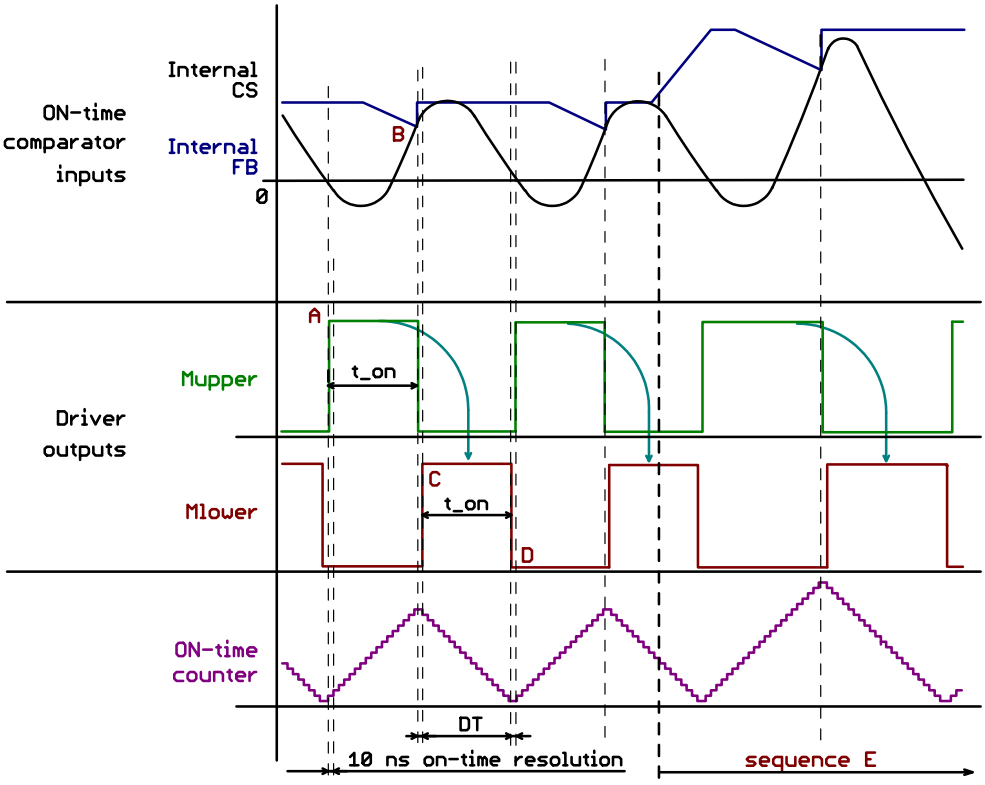


Figure 38. NCP13994 On−time Modulation Principle

The Mupper switch is activated by the controller after dead−time (DT) period elapses in point *A*. The frequency processing block increments the ON−time counter with 10 ns resolution until the internal CS signal crosses the internal FB set point for the ON−time comparator in point *B*. A DT period is then introduced by the controller to avoid any shoot−through current through the power stage switches. The DT period ends in point *C* and the controller activates the Mlower switch. The ON−time processing block decrements the ON_time counter down until it reaches zero. The Mlower switch is then turned−OFF at point *D* and the DT period is started. This approach results in perfect duty cycle symmetry for Mlower and Mupper switches. The Mupper switch on−time naturally increases and the operating frequency drops when the FB pin voltage is increased, i.e. when higher current is delivered by the converter output – sequence *E*.

The resonant capacitor voltage and thus also CS pin voltage can be out of balance in some cases – this is the case during transition from full load to no−load operation when skip mode is not used or adjusted correctly. The current mode operation is not possible in such case because the ON−time comparator output stays active for several switching cycles. Thus a special logic has been implemented in NCP13994 in order to repeat the last valid on−time until the current mode operation recovers – i.e. until the CS pin signal balance is restored by the system.

Overload and Open FB Protections

The overload protection and open FB pin detection are implemented via FB pin voltage monitoring in this controller. The FB fault comparator is triggered once the FB pin voltage reaches the V_{FB_FAULT} level. The fault timer is then enabled – refer to Figure 39. The time period to the FB fault event confirmation is defined by the preselected $t_{FB\_FAULT\_TIMER}$ parameter. The fault timer is reset once the FB fault condition diminishes or timer counts down when cumulative option is selected. The speed of timer counting when timer counts up and down can be different. A digital noise filter has been added after the FB fault comparator to overcome false triggering of the FB fault timer due to possible noise on the FB input.

When FB pin voltage reaches $V_{FB\_FAULT\_PEAK}$ level (FB fault peak function is selected) the FB fault timer duration is reduced – i.e. the timer is speed up by multiplication $K_{FB\_PEAKFT\_MULT}$.

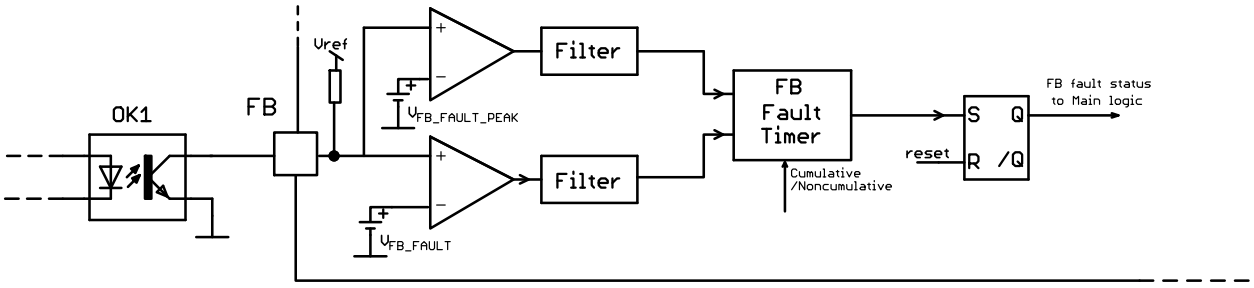


Figure 39. Internal FB Fault Management

The controller disables driver pulses and enters protection mode once the FB fault event is confirmed by the FB fault timer. Latched or auto−recovery operation is then triggered – depends on selected IC option. The controller adds an auto−recovery off−time period (t_{A-REC_TIMER}) and restarts the operation via soft start in case of auto−recovery option. The application temperature runaway is thus avoided in case of overload while the automatic restart is still possible once the overload condition disappears. The IC with latched FB fault option stays latched−off, supplied by the HV startup current source working in DSS mode, until the V_{CC_RESET} threshold is reached on the VCC pin or Line event is detected by HV pin – i.e. until user unplug power supply from the mains.

Please refer to Figure 53 and Figure 54 for an illustration of the NCP13994 FB fault detection block.

Secondary Short Circuit Detection with Primary and Secondary Current Reduction

The protection system described previously, implemented via FB pin voltage level detection, prevents continuous overload operation and/or open FB pin conditions. The primary current is naturally limited by the NCP13994 on−time modulation principle in this case. But the primary current increases when the output terminals are shorted. The NCP13994 controller will maintain zero voltage switching operation in such case, however high currents will flow through the power MOSFETS, transformer winding and secondary side rectification. The NCP13994 implements a dedicated secondary side short circuit protection system that will shut down the controller much faster than the regular FB fault event in order to limit the stress of the power stage components. The CS pin signal is monitored by the dedicated CS fault comparator − refer to Figure 37. The CS fault counter is incremented each time the CS fault comparator is triggered. The controller enters auto−recovery or latched protection mode (depending on IC option) in case the CS fault counter overflows refer to Figure 40. The CS fault counter is then reset once the CS fault comparator is inactive for at least $N_{CS\_FAULT\_DEC}$ Mupper upcoming pulses. This digital filtering improves CS fault protection system noise immunity.

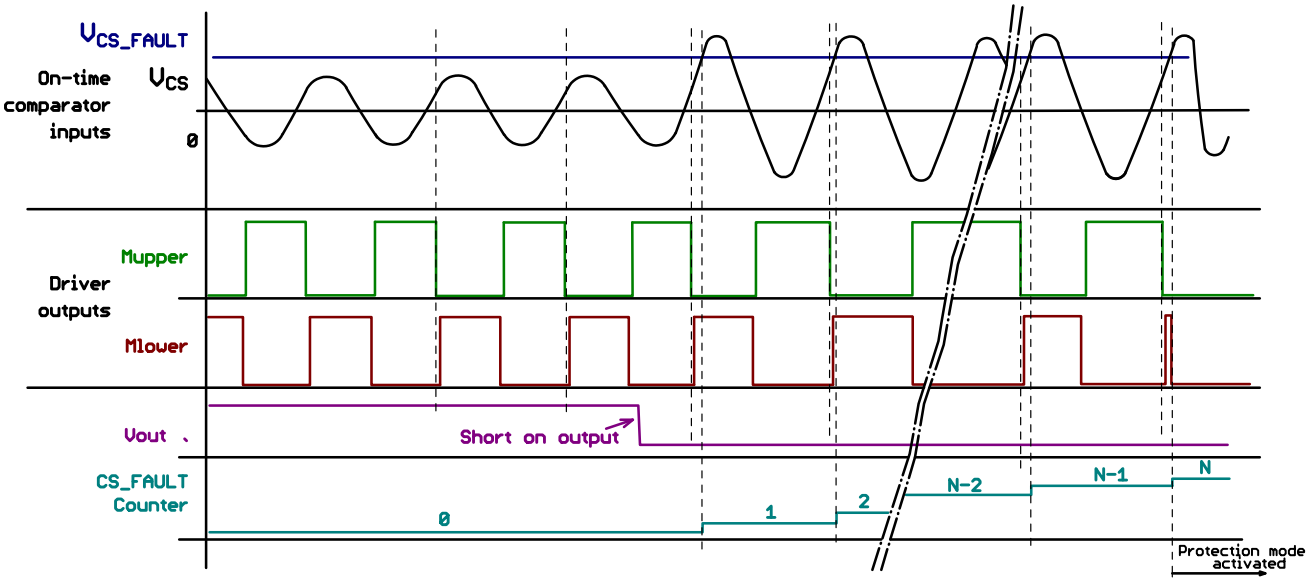


Figure 40. NCP13994 CS Fault Principle

The CS fault comparator event increases Ramp compensation (RC) gain by an increment $K_{RC\_GAIN\_INC}$ that is a portion of selected nominal RC gain. The RC gain is reduced to nominal level by a decrement when event of CS fault cmp. is not present for $N_{CS\_FAULT\_DEC}$ Mupper driver pulses. The decrement that is equal to increment is then placed at each followed Mupper driver pulse until RC gain reach nominal value or new CS fault cmp. event is detected.

Dedicated Startup Sequence and Soft−Start

Hard switching conditions can occur in a resonant SMPS application when the resonant tank operation is started with 50 % duty cycle symmetry – refer to Figure 41**.** This hard switching appears because the resonant tank initial conditions are not optimal for the clean startup.

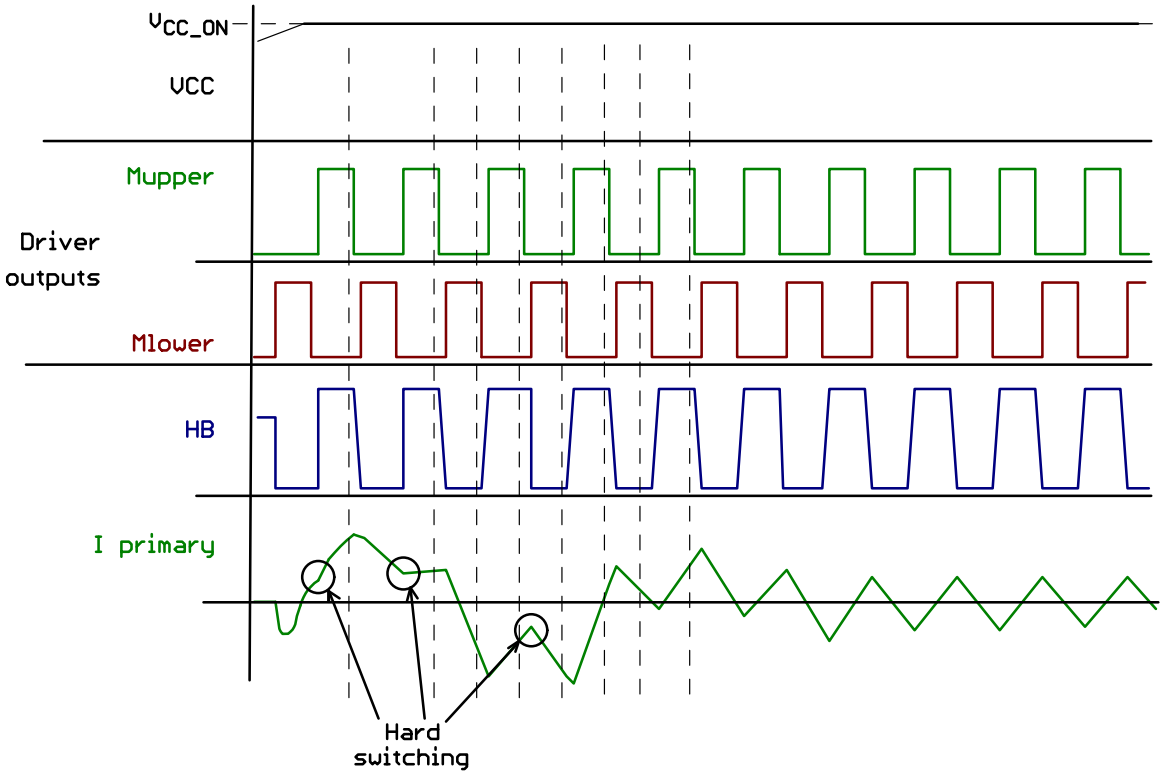


Figure 41. Hard Switching Cycle Appears in the LLC Application when Resonant Tank is Excited by 50 % Duty Cycle During Startup

The initial resonant capacitor voltage level can differ depending on how long delay was placed before application operation restart. The resonant capacitor voltage is close to zero level when application restarts after very long delay – for example several seconds, when the resonant capacitor is discharged by leakage to the power stage. However, the resonant capacitor voltage value can be anywhere between Vbulk and 0 V when the application restarts operation after a short period of time – like during periodical SMPS turn−on/off. Another factor that plays significant role during resonant power supply startup is the actual load impedance seen by the power stage during the first pulses of startup sequence. This impedance is not only defined by resonant tank components but also by the output loading conditions and actual output voltage level. The load impedance of resonant tank is low when the output is loaded and/or the output voltage is low enough to made secondary rectifies conducting during first switching cycles of startup phase. The resonant frequency of the resonant tank is given by the resonant capacitor capacitance and resonant inductance – note that the magnetizing inductance does not participate in resonance in this case. However, if the application starts−up when the output capacitors is charged and there is no load connected to the output, the secondary rectification diodes is not conducting during each switching cycle of startup sequence and thus the resonant frequency of resonant tank is affected also by the magnetizing inductance. In this case, the resonant frequency is much lower than in case of startup into loaded/discharged output.

These facts show that a clean, hard switching free and parasitic oscillation free, startup of an LLC converter is not an easy task, and cannot be achieved by duty cycle imbalance and/or simple resonant capacitor pre−charge to Vbulk/2 level. These methods only work in specific startup conditions.

This explains why the NCP13994 implements a proprietary startup sequence – see Figure 42 and Figure 43. The resonant capacitor is discharged down to V_{HB_MIN} before any application restart – except when restarting from skip mode.

Figure 42. Initial Resonant Capacitor Discharge before Dedicated Startup Sequence is Placed

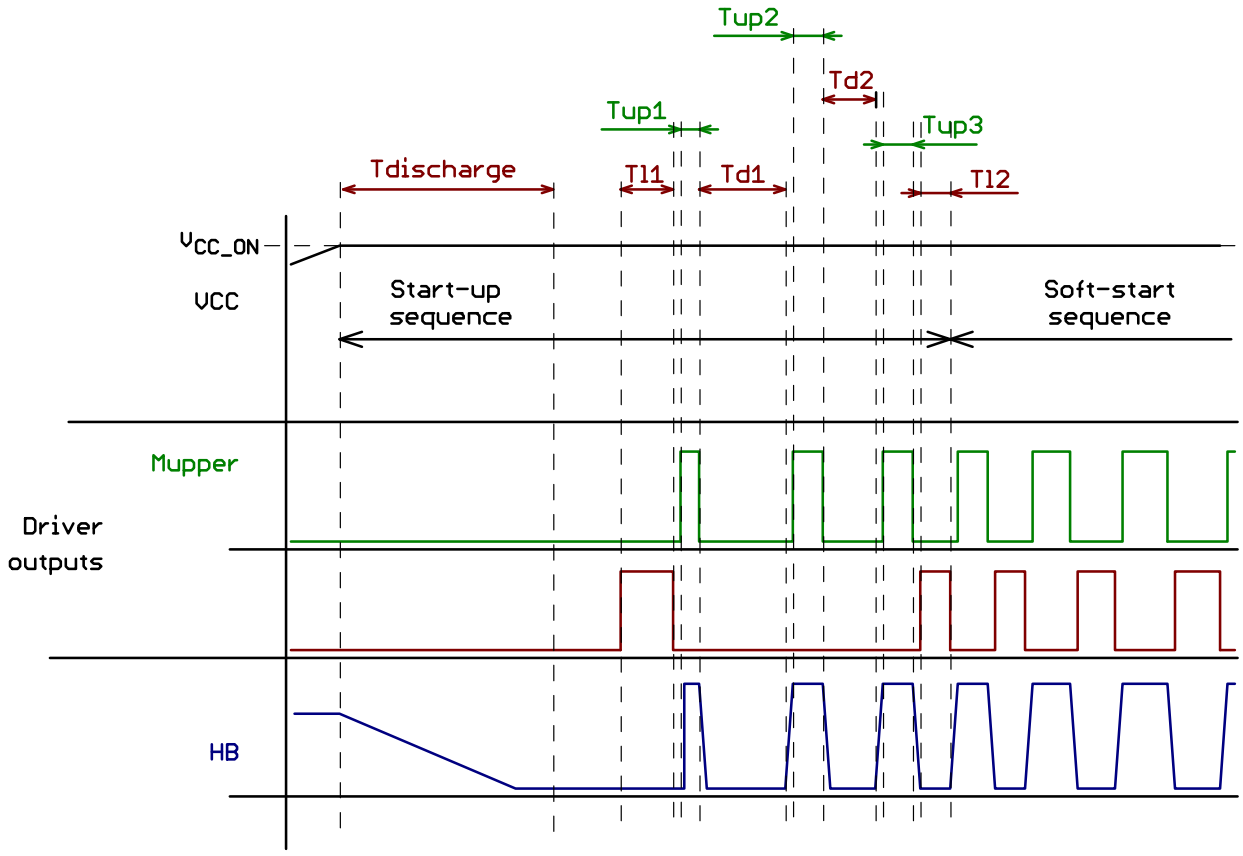


Figure 43. Dedicated Startup Sequence Detail

The resonant capacitor discharging process is simply implemented by activating an internal current limited switch connected between the HB pin and IC ground – refer to Figure 42. This technique assures that the resonant capacitor energy is dissipated in the controller without ringing or oscillations that could swing the resonant capacitor voltage to a positive or negative level. The controller detects that the discharge process is complete via HB pin voltage level monitoring. The discharge switch is disabled once the HB pin voltage drops below the V_{HB_MIN} threshold.

The dedicated startup sequence continues by activation of the Mlower driver output for Tl1 period (refer to Figure 43). This technique ensures that the bootstrap capacitor is fully charged before the first high−side driver pulse is introduced by the controller. The first Mupper switch on−time Tup1 period is fixed and depends on the application parameters. This period can be adjusted internally – various IC options are available. The Mupper switch is released after T_{up1} period and it is not followed by the Mlower switch activation. The controller waits for a new ZVS condition for Mupper switch instead and measures actual resonant tank conditions this way. The Mupper switch is then activated again after the Mlower blank period is used for measurement purposes. The second Mupper driver conduction period is then dependent on the previously measured conditions:

a. The Mupper switch is activated for 3/2 of previous Mupper conduction period in case the measured time between previous Mupper turn−off event and upper ZVS condition detection is equal or higher than two times of the the previous Mupper pulse conduction period
b. The Mupper switch is activated for previous Mupper conduction period in case the measured time between previous Mupper turn−off event and upper ZVS condition detection is lower than two times of previous Mupper pulse conduction period
c. ZVS condition is not detected due to low or no positive voltage swing on HB pin. Internal logic is waiting for ZVS information without any time limitation – i.e. stuck state. The stuck state can be interrupted by IC reset (via V_{CC_RESET} threshold) or by startup watchdog timer.

The startup period then depends on the previous condition. Another blank Mlower switch period is placed by the controller in case condition a) occurred. A normal Mlower driver pulse, with DC of 50 % to previous Mupper DRV pulse, is placed in case condition b) is fulfilled.

The dedicated startup sequence is placed after the resonant capacitor is discharged (refer to Figure 42 and Figure 43) in order to exclude any hard switching cycles during the startup sequence. The first Mupper switch cycle in startup phase is always non−ZVS cycle because there is no energy in the resonant tank to prepare ZVS condition. However, there is no energy in the resonant tank at this time,

there is also no possibility that the power stage MOSFET body diodes conducts any current. Thus the hard commutation of the body diode cannot occur in this case.

The IC will not start and provide regular driver output pulses until it is placed into the target application, because the startup sequence cannot be finished until HB pin signal is detected by the system. The IC features a startup watchdog timer ($t_{WATCHDOG}$) which restarted a dedicated startup sequence periodically in case the IC is powered without application (during bench testing) or in case the startup sequence is not finished correctly. The first Mupper on−time duration is automatically incremented when IC is restarted by the startup watchdog (depends on IC option). The increment is a portion of selected first Mupper duration and the first Mupper on−time duration can be incremented up to two times of preselected first Mupper duration. The IC will provide the first Mlower and first Mupper DRV pulses with a $t_{WATCHDOG}$ off−time in−between startup attempts.

Soft−start

The dedicated startup sequence is complete when condition b) from previous chapter is fulfilled and the controller continues operation with the soft−start sequence. A fully digital non−linear soft−start sequence has been implemented in NCP13994 using a soft−start counter and D/A converter that are gradually incremented by the Mlower driver pulses. A block diagram of the NCP13994 soft−start system is shown in Figure 44.

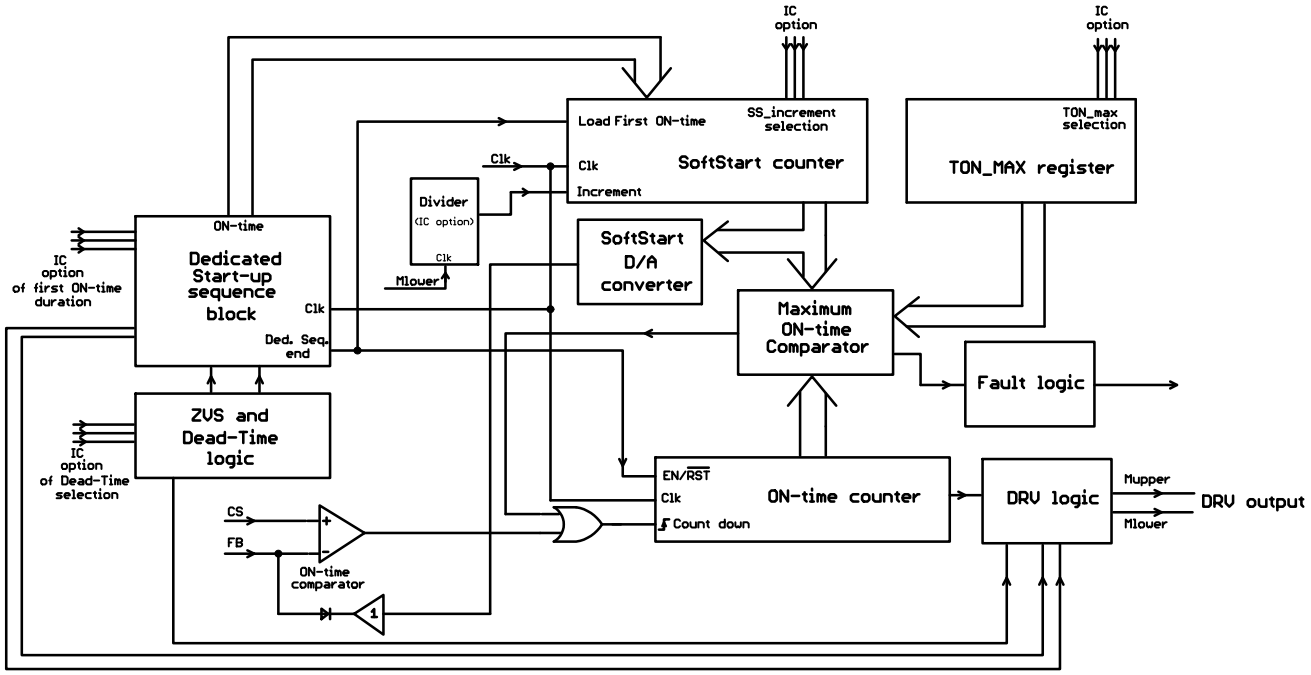


Figure 44. Soft−start Block Internal Implementation

The soft−start block subsystems and operation are described below:

1. The *Soft−Start counter* is a unidirectional counter that is loaded with the last Mupper on−time value that is reached at the dedicated startup sequence end (i.e. during condition b occurrence explained in previous chapter). The on−time period used in the initial period of the soft−start sequence is affected by the first Mupper on−time period selection and the dedicated startup sequence processing. The Soft−Start counter counts up from this initial on time period to its maximum value which corresponds to the IC maximum on−time (t_{TON_MAX}). The Soft−Start counter is incremented by the soft−start increment number ($t_{TON\_SS\_INC}$) during each Mlower switch on−time period. The soft−start start increment, selectable via IC option, thus affects the soft−start time duration. The Mlower clock signal for the Soft−Start counter can be divided down by the SS clock divider ($K_{FB\_SS\_INC}$) in case the soft−start period needs to be prolonged further – this can be also done via IC option selection. The Soft−Start period is terminated (i.e. the counter is loaded to its maximum) when the FB pin voltage drops below $V_{FB\_SKIP\_IN}$ level or FB pin detect that application is under regulation.
2. The *ON−time counter* is a bidirectional counter that is used as a main system counter for on−time modulation during soft−start, normal operation or overload conditions. The ON−time counter counts−up during Mupper switch conduction period and then counts down to zero – defining Mlower switch conduction period. This technique assures perfect 50 % duty cycle symmetry for both power switches as afore mentioned. The ON−time counter count−up mode can be switched to the count−down

mode by either of two events: *1st* when the ON−time counter value reaches the maximum on−time value (t_{TON_MAX}) or *2nd* when the actual Mupper on−time is terminated based on the current sense input information – i.e. by ON−time comparator.

4. The *Maximum ON−time comparator* compares the actual ON−time counter value with the maximum on−time value (t_{TON_MAX}) and activates the latch (or auto−recovery) protection mode once IC detect requested number of TON_MAX events. The minimum operating frequency of the controller is defined the same way. The Maximum ON−time comparator reference is loaded by the Soft−Start counter value on each switching cycle during soft−start. The Maximum ON−time fault signal is ignored during Soft−Start operation. The converter Mupper switch on−time (and thus operating frequency) is thus defined by the Soft−Start counter value indirectly – via Maximum ON−time comparator. The Mupper switch on−time is increased until the Soft−Start counter reaches t_{TON_MAX} period and Maximum on−time protection is activated, or until ON−time comparator takes action and overrides the Maximum ON−time comparator.
5. The *Soft−Start D/A converter* generates a soft−start voltage ramp for ON−time comparator input synchronously with Soft−Start counter incrementing. The internal FB signal for ON−time comparator input is artificially pulled−down and then ramped−up gradually when soft−start period is placed by the system – refer to Figure 45. The FB loop is supposed to take over at certain point when regulation loop is closed and output gets regulated so that soft−start has no other effect on the on−time modulation. The Soft−Start counter continues counting−up until it reaches its maximum value which corresponds to the IC maximum on−time value – i.e. the IC minimum operating frequency. The Soft−Start period is terminated (i.e. counter is loaded to its maximum) when the FB pin voltage drops below $V_{FB\_SKIP\_IN}$ level. The D/A converter output evolve accordingly to the Soft−Start counter as it is loaded from its output data bus.

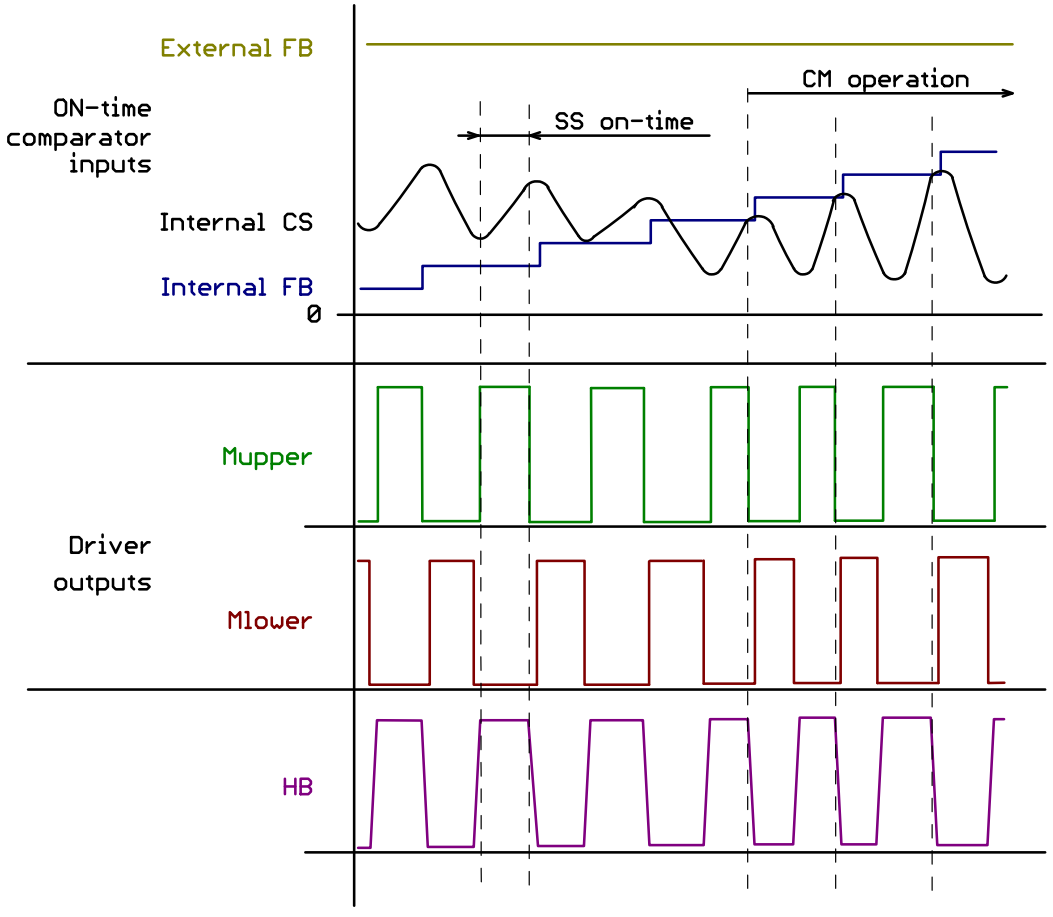


Figure 45. Soft Start Behavior

The Controller Operation During Soft−start Sequence Evolves as Follows:

The Soft−Start counter is loaded by last Mupper on−time value at the end of the dedicated startup sequence. The ON−time counter is released and starts count−up from zero until the value that is equal to the actual Soft−Start counter state. The Mupper switch is active during the time when ON−time counter counts−up. The Maximum ON−time comparator then changes counting mode of the ON−time comparator from count−up to count−down. A dead−time is placed and the Mlower switch is activated till the ON−time counter reaches zero value. The Soft−Start counter is incremented by selected increment during corresponding Mlower on−time period so that the following Mupper switch on−time is prolonged automatically – the frequency thus drops naturally. Because the operating frequency of the controller drops and Mlower DRV signal is used as a clock source for the Soft−start counter, the soft−start speed starts to decrease on each (or on each N−th) Mlower driver pulse (where N is defined by $K_{FB\_SS\_INC}$) of switching cycle. So we have non−linear soft−start that helps to speed up output charging in the beginning of the soft−start operation and reduces the output voltage slope when the output is close to the regulation level. The output bus of the Soft−Start counter addresses the D/A converter that defines the ON−time comparator reference voltage. This reference voltage thus also increases non−linearly from initial zero level until the level at which the current mode regulation starts to work. The on−time of the Mupper and Mlower switch is then defined by the ON−time comparator action instead of the Maximum ON−time comparator. The soft−start then continues until the regulation loop is closed and the on−time is fully controlled by the secondary regulator. The Soft−Start counter then continues in counting and saturates at its maximum possible value which corresponds to IC minimum operating frequency. The maximum on−time fault detection system is enabled when Soft−Start counter value is equal to t_{TON_MAX} value.

The previous on−time repetition feature, described above in the ON−time modulation and feedback loop chapter, is disabled in the beginning of soft start period. This is because the ON−time comparator output stays high for several cycles of soft start period – until the current mode regulation takes over. The previous on−time repetition feature is enabled once the current modulation starts to work fully, i.e. in the time when the ON−time comparator output periodically drops to low state within actual Mupper switch on−time period. Typical startup waveform of the LLC application driven by NCP13994 controller can be seen in Figure 46.

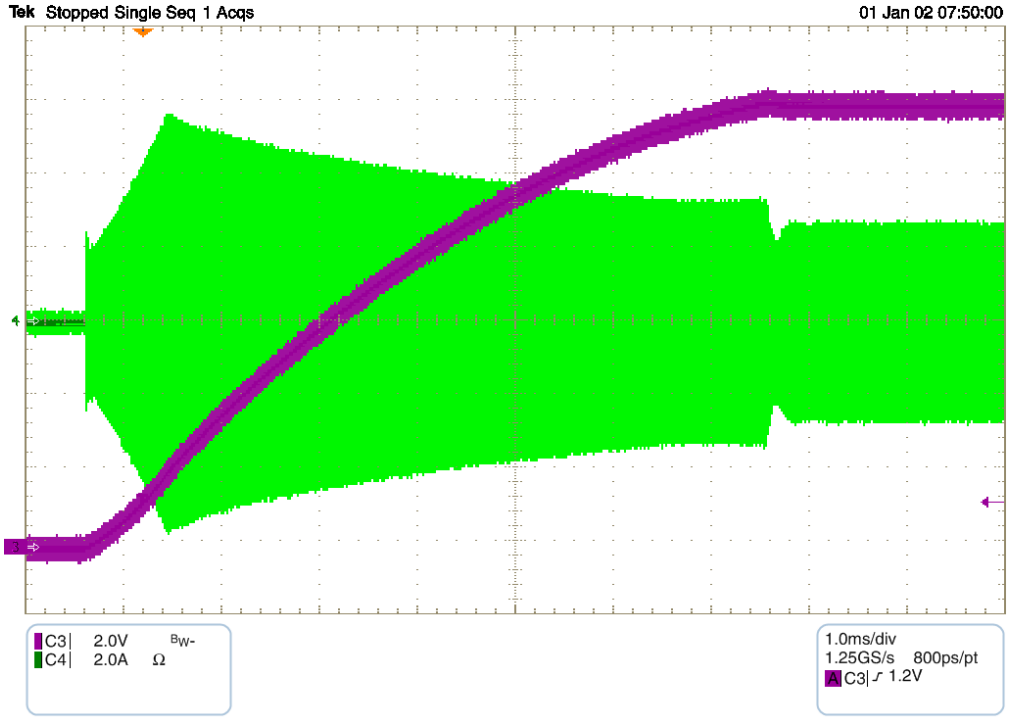


Figure 46. Application Startup with NCP13994 − Primary Current − Green, V_{out} − Magenta

Skip Mode Operation

Then NCP13994 implements proprietary light load and quiet skip mode operating techniques that improve light load efficiency, reduce no−load power consumption and significantly reduce acoustic noise. Controller uses 50 % duty cycle symmetry under full and medium load conditions. Normal current mode frequency modulation takes place during this operating mode – refer to on−time processing section of this datasheet. The 50 % duty cycle symmetry operating mode is replaced by continues operation with minimum switching patterns repeated after controlled amount of off−time when load is decreased below preselected level. Zero voltage switching technique is still present for the power switches to achieve high light load efficiency. Quiet skip mode operation is initiated when load drops further and FB voltage drops below another FB threshold that is user adjustable on the skip pin. The frequency of skip burst is regulated by internal digital controller around preselected quiet skip frequency clamp in order to reduce acoustic noise. The skip frequency then drops to very low values during no−load conditions. Refer to Figure 47, Figure 48 and Figure 49 for typical application waveforms during light load and quiet skip mode operating modes.

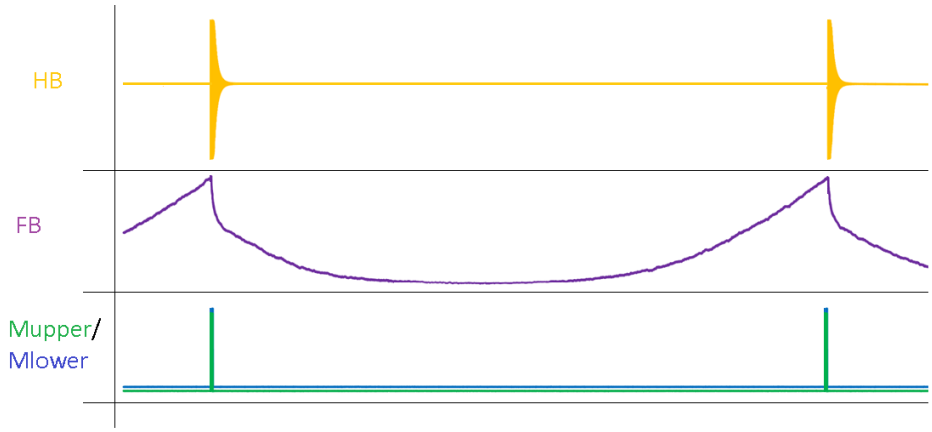


Figure 47. No−load Operation

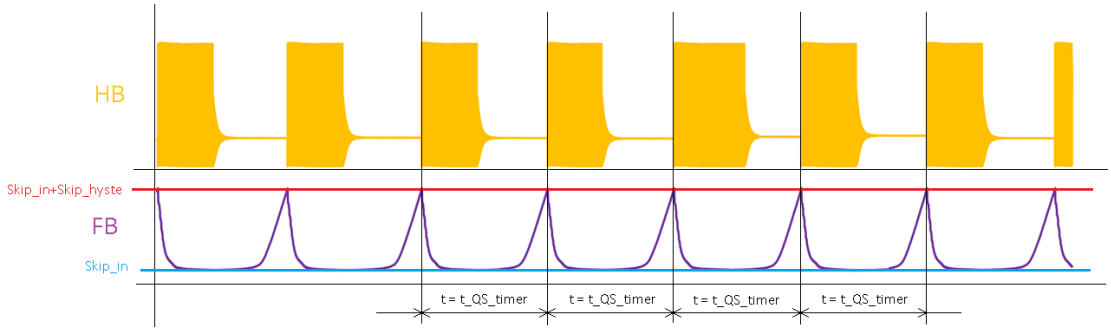


Figure 48. Quiet Skip Mode Operation

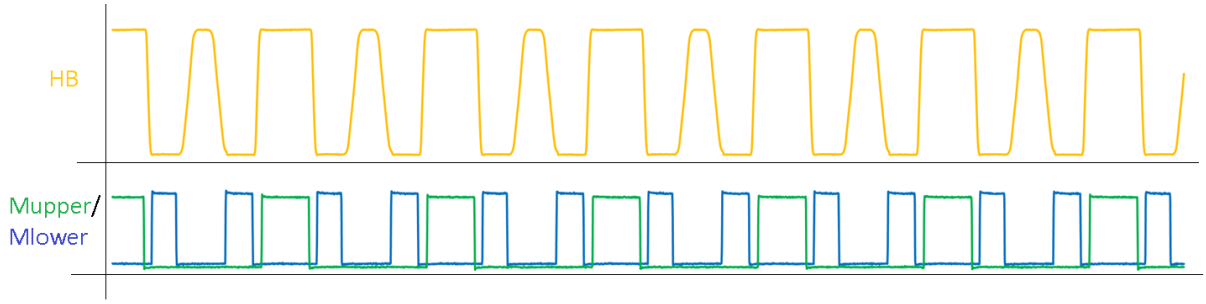


Figure 49. Light−load Operation

The High Voltage Half−bridge Driver

The driver features a traditional bootstrap circuitry, requiring an external high voltage diode with resistor in series for the capacitor refueling path. Minimum series resistor Rboot value is 3.3 Ω. Figure 50 shows the internal architecture of the drivers section. The device incorporates an upper UVLO circuitry that makes sure enough V_{GS} is available for the upper side MOSFET. The output drivers are clamped to specific value to protect MOSFET gates when VCC/VBOOT is higher than 20 V.

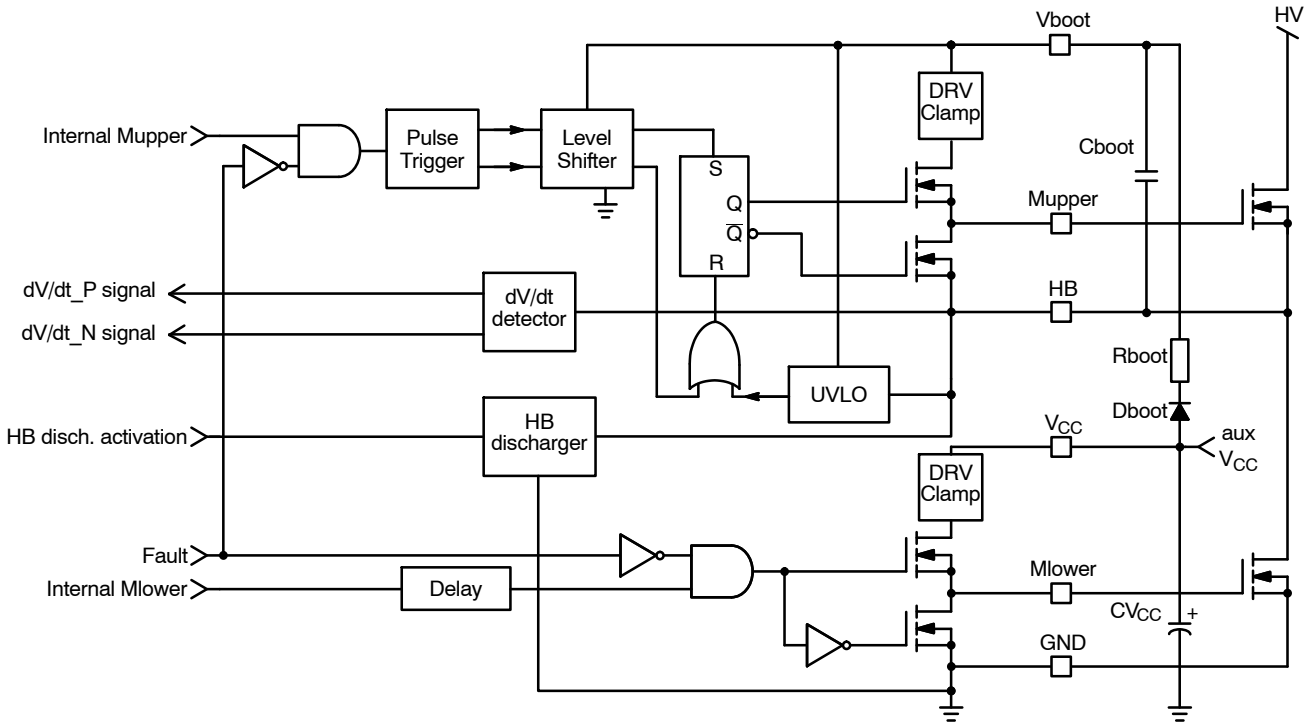


Figure 50. The NCP13994 Internal DRVs Structure

The internal dV/dt sensor detects the HB pin voltage transitions in order to setup the optimum DT period – please refer to Dead−Time chapter. The internal HV discharge switch is connected to the HB pin and discharges resonant capacitor before application startup. The current through the switch is regulated to $I_{HB\_DISCHARGE1}$ level until the V_{HB_MIN} threshold voltage is reached on the HB pin. The discharge system assures always the same startup conditions for application – regardless of previous operating state. The HB pin discharge current sink features an independent over−temperature protection which limits its input current in case the discharger temperature exceeds $T_{HB\_DISCH\_CLAMP}$ to avoid damage to the HB discharger silicon structure.

As stated in the maximum ratings section, the floating portion can go up to 730 VDC on the BOOT pin. This voltage range makes the IC perfectly suitable for offline and lighting applications.

Automatic Dead−time Adjust

The dead−time period between the Mupper and Mlower drivers is always needed in half bridge topologies to prevent any cross conduction through the power stage MOSFETs that would result in excessive current, high EMI noise generation or total destruction of the application. Fixed dead−time period is often used in the resonant converters because this approach is simple to implement. However, this method does not ensure optimum operating conditions in resonant topologies because the magnetizing current is changing with line and load conditions. The optimum dead−time, under a given operating conditions, is equal to the time that is needed for bridge voltage to transition between upper and lower states and vice versa – refer to Figure 51.

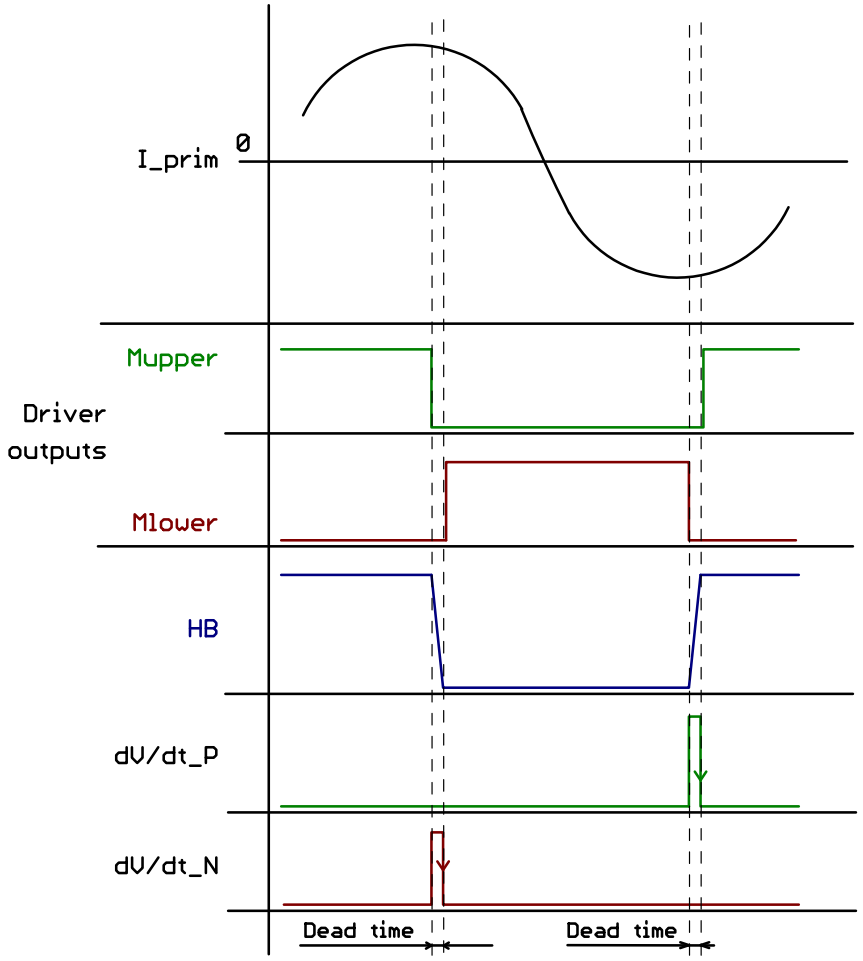


Figure 51. Optimum Dead−time Period Adjust

The MOSFET body diode conduction time is minimized when optimum dead−time period is used which results in maximum efficiency of a resonant converter power stage. There are several methods to determine the optimum dead−time period or to approximate it (for example using auxiliary winding on main transformer or modulating dead−time period with operating frequency of the converter). These approaches however require a dedicated pin for nominal dead−time adjust or auxiliary winding voltage sensing. The NCP13994 uses a dedicated method that senses the HB pin voltage internally and adjusts the optimum dead−time period with respect to the actual operating conditions of the converter. The high−voltage dV/dt detector, connected to the HB pin, delivers two internal digital signals that are indicating Mupper to Mlower and Mlower to Mupper transitions that occur on the HB and VBOOT pins after the corresponding MOSFET switch is turned−off. The controller enables the opposite MOSFET in the power stage once the corresponding dV/dt sensor output provides information about HB (or VBOOT) pin transition ends.

The ZVS transition on the bridge pin (HB) could take a longer time or even does not finish in some cases – for example with extremely low bulk voltage or when some critical failure occurs. This situation should not occur normally in correctly designed application because several other protections would prevent such a situation. The NCP13994 implements maximum DT period clamp that limits driver's off−time period to the t_{DT_MAX} value. The corresponding MOSFET driver is forced to turn−on by the internal logic regardless of missing dV/dt sensor signal. This situation does not occur during normal operation and will be considered a fault state by the device. There are several possibilities on how the controller continues operation after this event occurrence – depending on the IC option:

1. The opposite MOSFET switch is forced to turn−on when t_{DT_MAX} period elapses and no fault is generated
2. The controller is latched−off in case the ZSV condition is not detected within selected t_{DT_MAX} period
3. The controller stops operation and restarts operation after auto−recovery period in case the ZSV condition has not been detected within the selected t_{DT_MAX} period

A DT fault counter option is available. Selected number (N_{DT_MAX}) or DT fault events have to occur in order to confirm DT fault in this case.

A fixed DT option is also available for this device. The internal dV/dt sensor signal is not used for this device option and the t_{DT_MAX} period is used as a regular DT period instead. The DT fault detection is disabled in this case.

Temperature Shutdown

The NCP13994 includes a temperature shutdown protection. When the temperature rises above the upper threshold, the controller stops switching instantaneously, and goes into the off−mode with extremely low power consumption. The V_{CC} supply is maintained (by operating the HV start−up in DSS mode) in order to memorize the TSD event information. When the temperature falls below the lower threshold, the full restart (including soft−start) is initiated by the controller. The HV startup current source features an independent over−temperature protection which limits its output current in case the DIE temperature exceeds TSD to avoid damage to the HV startup silicon structure.

Recommended Layout

The correct layout is key step towards to reliable operation of designed application. The recommended layout of NCP13994 controller is illustrated on Figure 52. The most important part of layout is connection of the GND path.

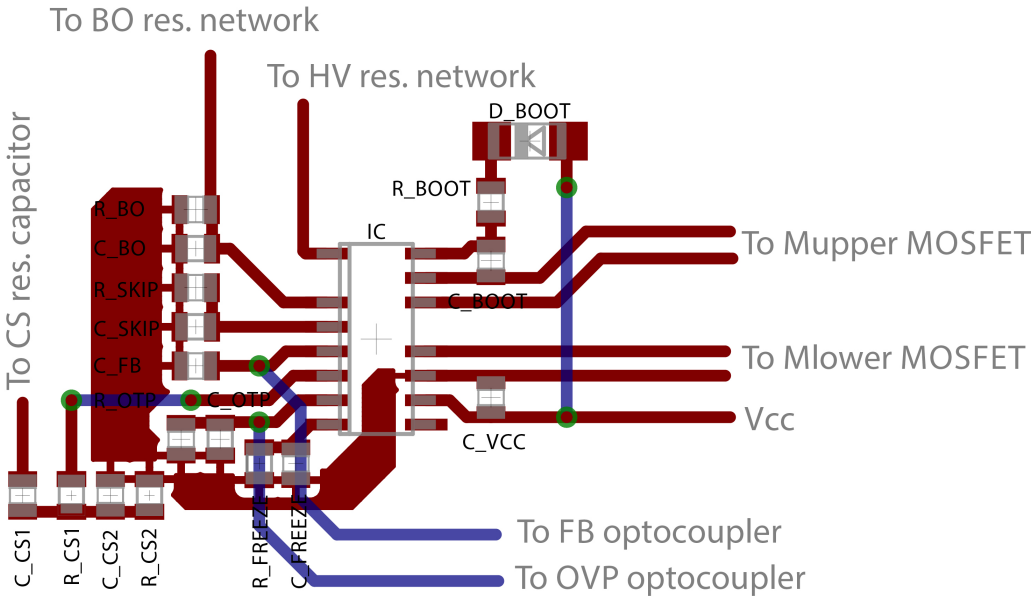


Figure 52. Recommended Layout

APPLICATION INFORMATION

Controller Operation Sequencing of NCP13994 LLC Controller

The paragraphs below describe controller operation sequencing under several typical cases as well as transitions between them.

Application Start, Brown−out Off and Restart, OVP/OTP Latch and then Restart – Figure 53

Application is connected to the mains at point *A* thus the HV input of the controller becomes biased. The HV startup current source starts charged VCC capacitor until V_{CC} reaches V_{CC_ON} threshold.

The all analog blocks are enabled at V_{CC_RESET} threshold. A START_BLANK is activated at V_{CC_RESET} threshold also to ensure that the internal blocks are fully biased and stabilized to correctly process conditions/faults before IC start. The VCC pin voltage reached V_{CC_ON} threshold in point *B*. The PFC front stage is activated via PFC MODE pin that change status at mentioned threshold. The IC DRVs were not enabled after first V_{CC_ON} threshold in this case as the voltage on VBULK is not enough high. The IC keeps all internal blocks biased and operates in the DSS (Dynamic Self−Supply) mode as long as the stop conditions is still present.

The BO_OK condition is received (voltage on VBULK reach V_{BO} level affected by hysteresis) at point *C*. The IC activates the startup current source to refill VCC capacitor in order to assure sufficient energy for a new startup. The VCC capacitor voltage reaches V_{CC_ON} level again. The DRVs are enabled and the application is started because there is no faults or stop condition at that time.

Line and also bulk voltage drops at point *D* so the BO_OK signal become low (voltage on VBULK drops below V_{BO} level). The LLC DRVs are disabled as well as OVP/OTP block bias. The PFC MODE output stay high to keep the PFC controller biased, so the BO block still monitors the bulk voltage. The controller activates the HV startup current source into DSS mode to keep enough VCC voltage for operation of all blocks that are active while the IC is waiting for BO_OK condition.

The line voltage and thus also bulk voltage increase at point *E* so the Brown−out block provide the BO_OK signal once the V_{BO} (with hysteresis) level is reached. The startup current source is activated after BO_OK signal is received to charge the VCC capacitor for a new restart. The analog blocks are enabled (biased) including START_BLANK period at time when BO_OK signal is received.

The V_{CC_ON} level is reached in point *F*. The controller restores operation via the regular startup sequence and soft−start after all startup condition are fulfil (no fault or stop condition detected and VCC is higher when V_{CC_ON} threshold).

The application then operates normally until the OVP/OTP input is pulled−up at point *G*. The controller then enters latch−off mode in which all blocks are disabled. The VCC management controls the HV startup in DSS mode in order to keep enough VCC level to hold the latch−up state memorized while the application remains plugged−in to the mains.

The power supply is removed from the mains at point *H* and the VCC voltage drops down below V_{CC_RESET} level thus the controller is released from latch. A new application start occurs when the user plugs the application the mains again.

Application Start, Brown−out Off and Restart, Output Short Fault with Auto−recovery Restart – Figure 54

Operating waveforms descriptions for this figure is similar to one for Figure 53 from point *A* till point *G*.

The LLC converter operation is stopped in point *G* because the controller detects an overload condition (short circuit event in this case as the Vout drops abruptly). The controller disables almost all blocks. The HV startup DSS operation is initiated in order to keep enough VCC level for all internal blocks that need to be biased. Internal auto−recovery timer counts down the recovery delay period t_{A-REC_TIMER}.

The auto−recovery restart delay period lapses at point *H*. The HV startup current source is activated to recharge VCC capacitor before a new restart and all block are enabled with START_BLANK period.

The V_{CC_ON} threshold is reached in point *I*. The controller restores operation via the regular startup sequence and soft−start after all startup condition are fulfil (no fault or stop condition detected and VCC is higher when V_{CC_ON} threshold). The LLC converter operation is enabled, including a dedicated startup and soft−start period. The output short circuit is removed in between thus the Vout ramped−up and the FB loop took over during the LLC converter soft−start period.

Startup, Skip−mode Operation, Low Line Detection and Restart into Skip−mode – Figure 55

Application is connected to the mains at point *A* thus the HV input of the controller becomes biased. The HV startup current source starts charged VCC capacitor until V_{CC} reaches V_{CC_ON} threshold.

The all analog blocks are enabled at V_{CC_RESET} threshold. A START_BLANK is activated at V_{CC_RESET} threshold also to ensure that the internal blocks are fully biased and stabilized to correctly process conditions/faults before IC start. The VCC pin voltage reached V_{CC_ON} threshold in point *B*. The PFC front stage is activated via PFC MODE pin that change status at mentioned threshold. The IC DRVs were not enabled after first V_{CC_ON} threshold in this case as the voltage on VBULK is not enough high. The IC keeps all internal blocks biased and operates in the DSS (Dynamic Self−Supply) mode as long as the stop conditions is still present.

The controller authorizes DRVs at point *C* as there are no faults conditions present. The load current is reduced thus the FB loop reduces the primary controller FB pin voltage.

The load diminished further and the FB skip threshold is reached in point *D*. The controller turns−off all the blocks that are not essential for the controller operation during skip−mode – i.e. all blocks except FB block and VCC management. This technique is used to minimize the device consumption when there are no driver pulses during skip−mode operation. The output voltage then drops naturally and the FB loop reflects this change into the primary FB pin voltage that increases accordingly. The auxiliary winding is refilling VCC capacitor during each skip burst thus the controller is supplied from the application during the skip mode operation.

The controller FB skip−out threshold is reached in point *E*; the controller enables all blocks and LLC DRVs to refill the output capacitor. The controller did not activate the HV startup current source because there is enough voltage present on the VCC pin during skip mode. The OTP blank periods is activated at the beginning of the skip burst to mask possible OTP faults.

NOTE: The VCC capacitor needs to be chosen with a value high enough to ensure that V_{CC} will not drop below the V_{CC_OFF} level during skip mode. The device would enters into off−mode (refer to Figure 38) when appropriate off−mode is enabled.

The line voltage drops in point *F*, but the bulk voltage is dropping slowly as there is nearly no consumption from the bulk capacitor during skip mode – only some refilling bursts are provided by the controller. The application thus continues in skip mode operation for several skip burst cycles.

The bulk voltage level less than V_{BO} threshold is detected by the controller in point **G** during one of the skip burst pulses. The controller thus disabled DRVs and enters DSS mode of operation in which the OVP/OTP block is disabled and the controller is waiting for BO_OK event. The PFC MODE provides the V_{PFCM_REG1} voltage in this case to allow the PFC stage to refill bulk capacitors.

The line voltage is increased at point *H* thus the controller receives the BO_OK signal. The startup current source is activated after BO_OK signal is received to charge the VCC capacitor for a new restart. The analog blocks are enabled (biased) including START_BLANK period at time when BO_OK signal is received.

The V_{CC_ON} level is reached in point *I*. The controller restores operation via the regular startup sequence and soft−start after all startup condition are fulfil (no fault or stop condition detected and VCC is higher when V_{CC_ON} threshold). The application then enters skip mode again as the load current is low.

Start−up, Normal Operation, Transition to Off−mode Operation and Output Re−charge in Off−mode – Figure 38

Operating waveforms descriptions for this figure are the same as for Figure 55 from point *A* until point *C* – Please refer to Figure 55 for details regarding operation between these time events.

The secondary controller activates off−mode operation by pulling FB pin below $V_{FB\_REM\_OFF}$ level, thus the IC goes into skip−mode for long time at point *D*. The controller turns−off all the blocks that are not essential for controller operation during skip−mode – i.e. all blocks except FB and VCC management blocks. This technique is used to minimize device consumption when there are no driver pulses during skip−mode operation.

The V_{CC} drops naturally by IC consumption below V_{CC_OFF} threshold at point *E* – i.e. the off−mode is confirmed. The controller turns−off all the blocks that are not essential for controller operation during off−mode – i.e. all blocks including FB block and big portion of the VCC management. This technique is used to minimize device consumption when there are no drive pulses during off−mode operation. The output voltage is then dropped naturally due to secondary controller and resistive dividers consumption. The primary controller is supplied from the HV startup current source that operates in DSS mode.

The secondary controller interrupts off−mode operation by releasing the opto−coupler and allowing the voltage on FB pin to ramp−up by the internal pull−up current source at point *F*. The controller activates the HV startup current source and recharges the VCC capacitor to prepare enough V_{CC} voltage for a new startup.

The V_{CC} voltage reaches V_{CC_ON} threshold at point *G* and the LLC converter starts (including soft−start).

The output voltage is ramped up while the FB loop is not closed yet as the V_{OUT} is still below regulation level. The output voltage then reaches regulation level and the FB pin voltage drops abruptly on the primary – hitting the FB skip−in threshold at point *H*. The LLC drivers are thus disabled by the skip comparator. The FB then increases naturally – calling for new skip burst (refer to skip mode operation description in previous text).

The secondary controller activates off−mode operation by pulling−down FB pin and V_{CC} voltage naturally drops below V_{CC_OFF} threshold. The primary controller enters off−mode operation again at point *I*.

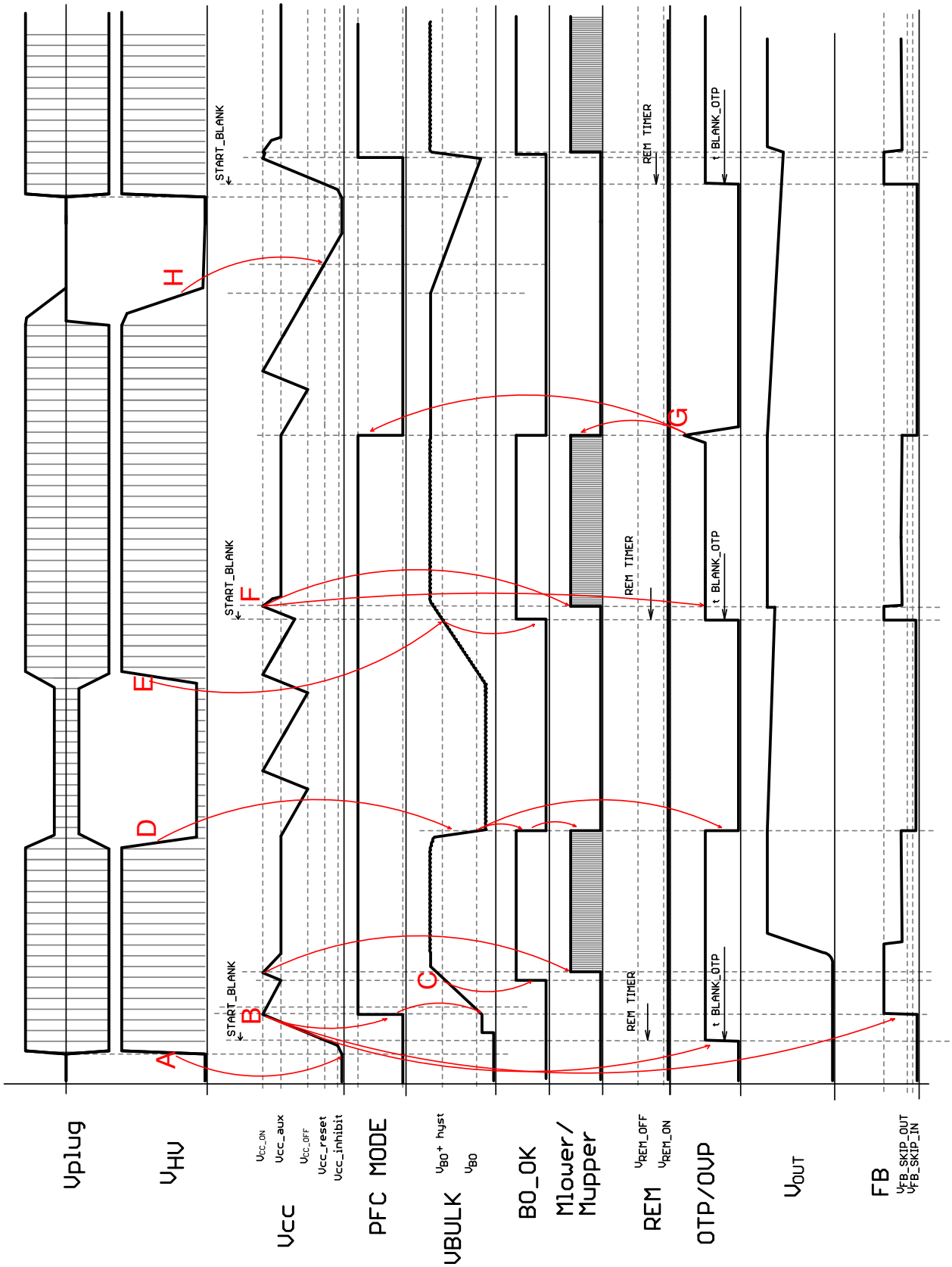


Figure 53. Application Start, Brown−out Off and Restart, OVP/OTP Latch and then Restart

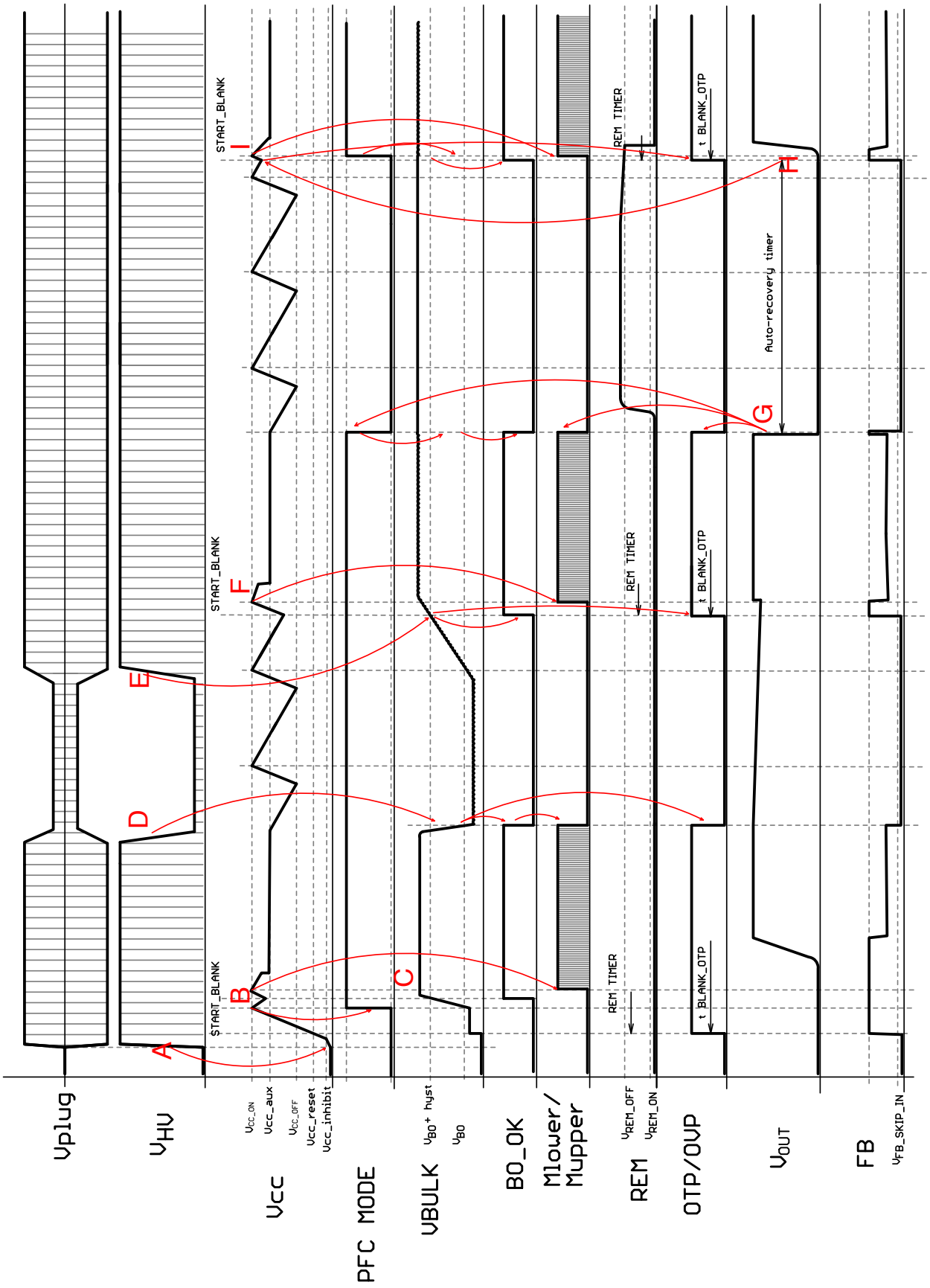


Figure 54. Application Start, Brown−out Off and Restart, Output Short Fault with Auto−recovery Restart

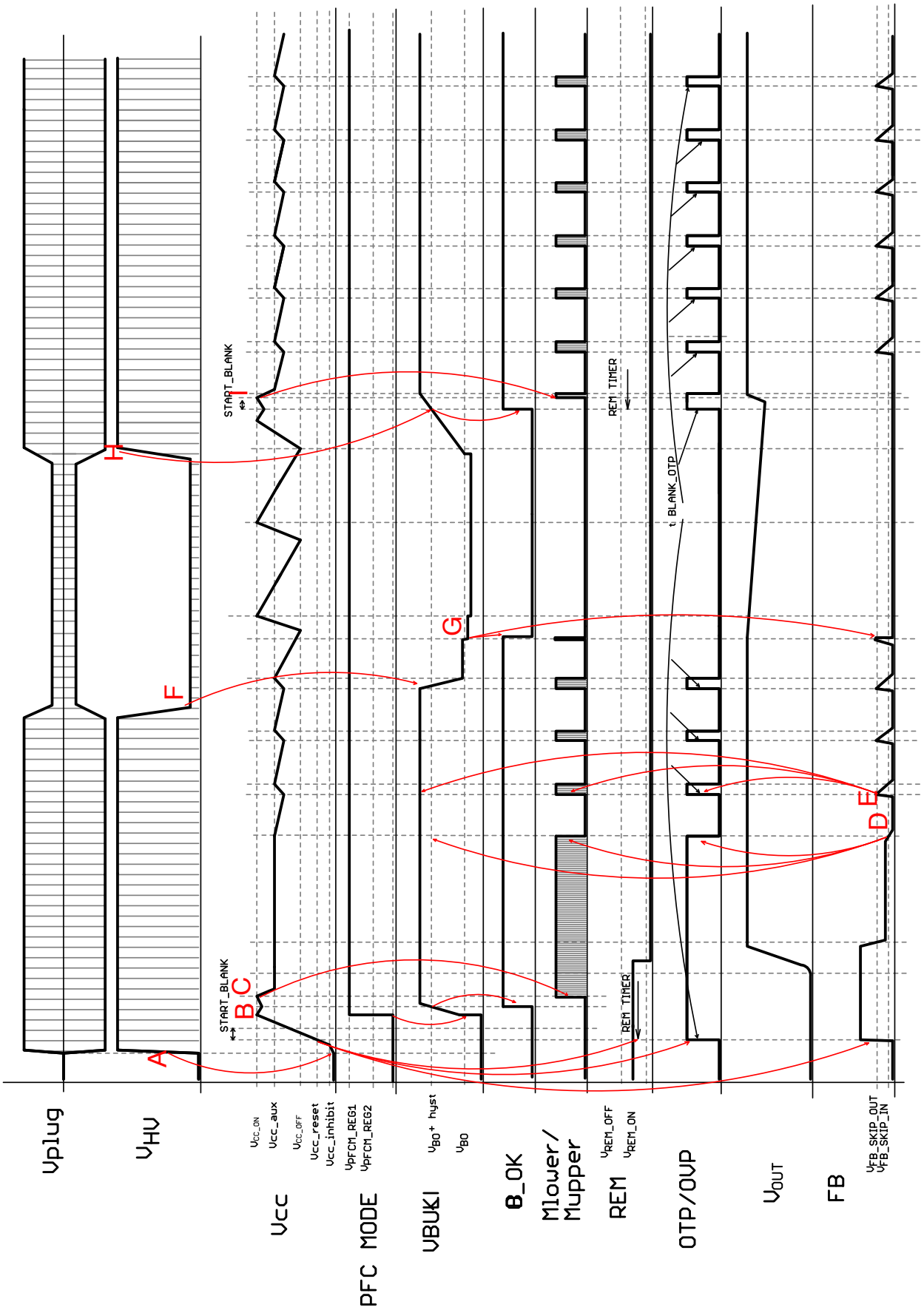


Figure 55. Startup, Skip−mode Operation, Low Line Detection and Restart into Skip

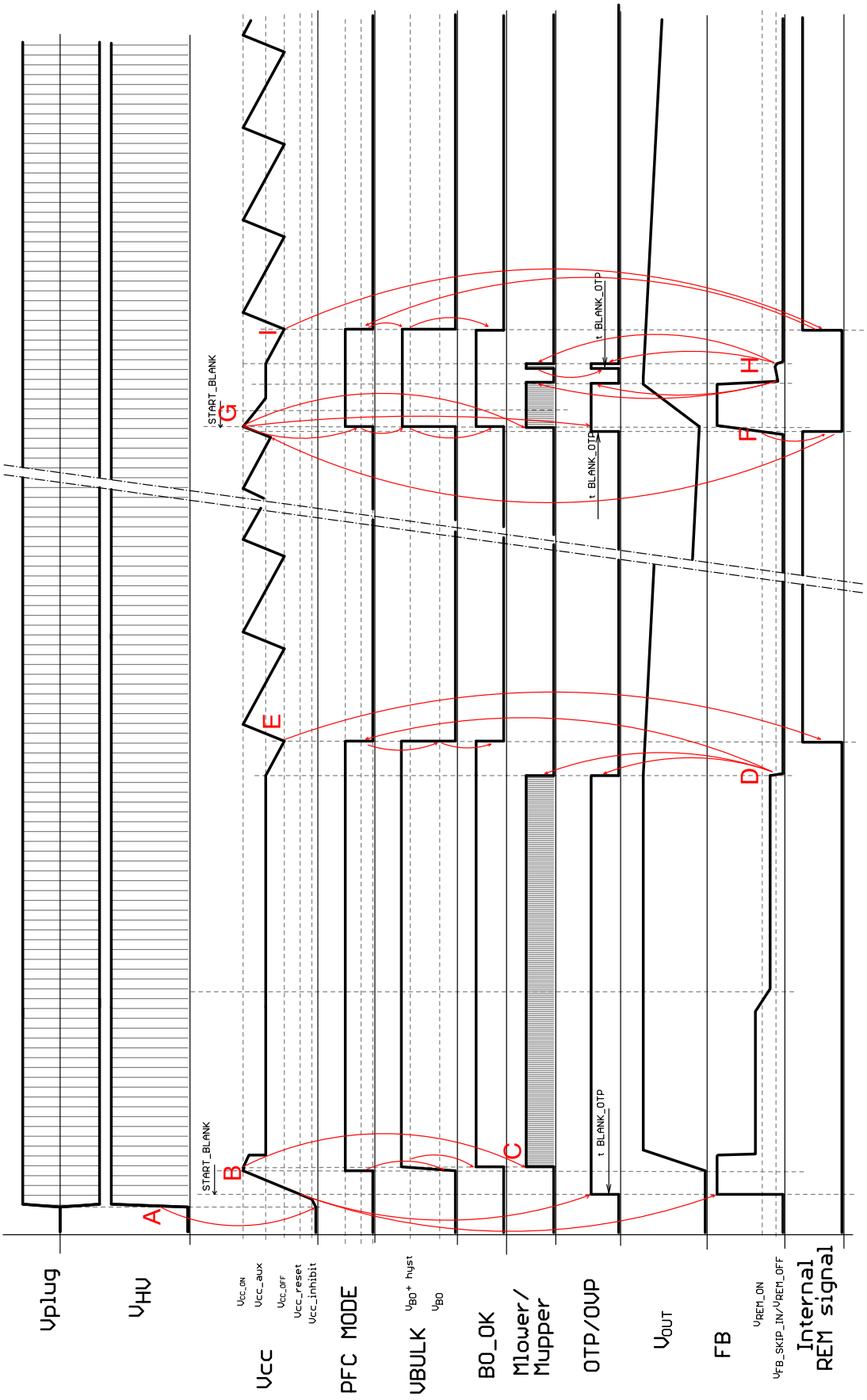


Figure 56. Start−up, Normal Operation, Transition to Off−Mode Operation and Output Re−charge in Off−mode

ORDERING INFORMATION

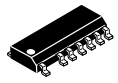
Device	Package Marking	Package Type	Shipping†
NCP13994AADR2G	NCP13994AA	SOIC−16 NB MISSING PINS 2 AND 13 (Pb−Free)	2,500 / Tape & Reel
NCP13994ACDR2G	NCP13994AC	SOIC−16 NB MISSING PINS 2 AND 13 (Pb−Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

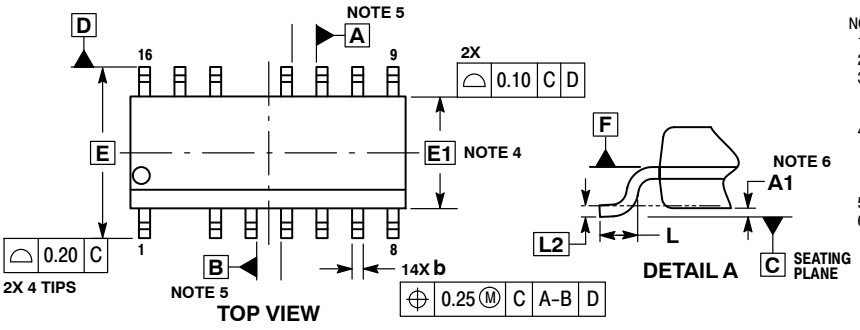
SOIC−16 NB MISSING PINS 2 AND 13

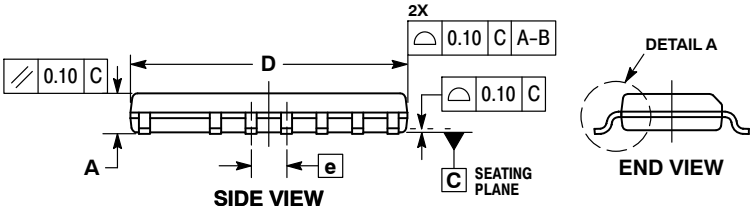
CASE 751DU
ISSUE O

DATE 18 OCT 2013



SCALE 1:1

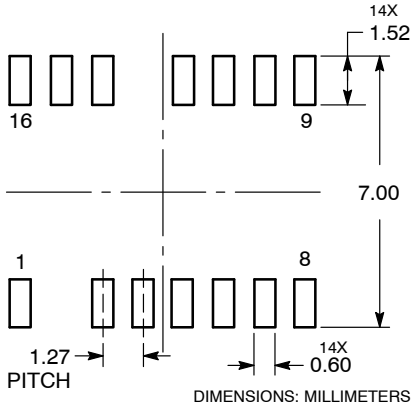




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

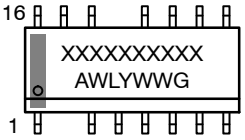
	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
b	0.35	0.49
c	0.17	0.25
D	9.80	10.00
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L2	0.203 BSC	

RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

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DESCRIPTION:	SOIC−16 NB MISSING PINS 2 AND 13	PAGE 1 OF 1

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