NCP1249

High-Voltage Current-Mode PWM Controller Featuring Peak Power Excursion and Extremely Low Stand-by Power Consumption

ON Semiconductor®

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The NCP1249 is a highly integrated high−voltage PWM controller capable of delivering a rugged and high performance offline power supply with extremely low no−load consumption. With a supply range up to 30 V, the controller hosts a jittered 65−kHz switching circuitry operated in peak current mode control. When the power on the secondary side starts to decrease, the controller automatically folds back its switching frequency down to a minimum level of 26 kHz. As the power further goes down, the part enters skip cycle while freezing the peak current setpoint.

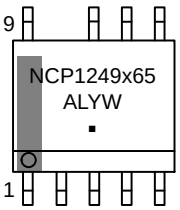
To help build rugged converters, the controller features several key protective features: a internal brown−out, a non−dissipative Over Power Protection for a constant maximum output current regardless of the input voltage and two latched over voltage protection inputs − either through a dedicated pin or via the VCC input.

The controller architecture is arranged to authorize a transient peak power excursion when the peak current hits the limit. At this point, the switching frequency is increased from 65 kHz to 130 kHz until the peak requirement disappears. The timer duration is then modulated as the converter crosses a peak power excursion mode (long) or undergoes a short circuit (short).

NCP1249 comes in both Active ON (A and B versions) and Active OFF (C and D versions).

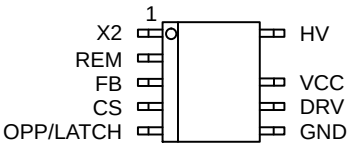
SOIC−9 NB
D SUFFIX
CASE 751BP

MARKING DIAGRAM

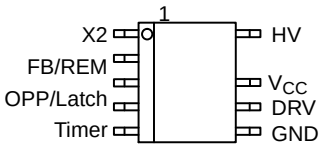


NCP1249x65 = Specific Device Code
x = A, B, C, D
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

PIN CONNECTIONS



NCP1249A/B (Top View)



NCP1249C/D (Top View)

Features

- High−voltage Current Source for Lossless Start−up Sequence
- Remote Input for Standby Operation Control
- Automatic and Lossless X2 Capacitors Discharge Function
- 65−kHz Fixed−frequency Current−mode Control Operation with 130−kHz Excursion
- Internal and Adjustable Over Power Protection (OPP) Circuit
- Internal Brown−Out Protection Circuit
- Frequency Foldback down to 26 kHz and Skip−cycle in Light Load Conditions
- Adjustable Ramp Compensation
- Internally Fixed 4−ms Soft−start
- 100% to 25% Timer Reduction from Overload to Short−circuit Fault
- Frequency Jittering in Normal and Frequency Foldback Modes
- Latched OVP Input for Improved Robustness and Latched OVP on V_{CC}
- Up to 30 V V_{CC} Maximum Rating
- +300 mA/ −500 mA Source/Sink Drive Capability
- Extremely Low No−load Standby Power
- Option for Auto−Recovery or Latched Short−Circuit Protection
- Internal Thermal Shutdown with Hysteresis
- These are Pb−Free Devices

Typical Applications

- Converters Requiring Peak−power Capability such as Printers Power Supplies, ac−dc Adapters for Game Stations

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

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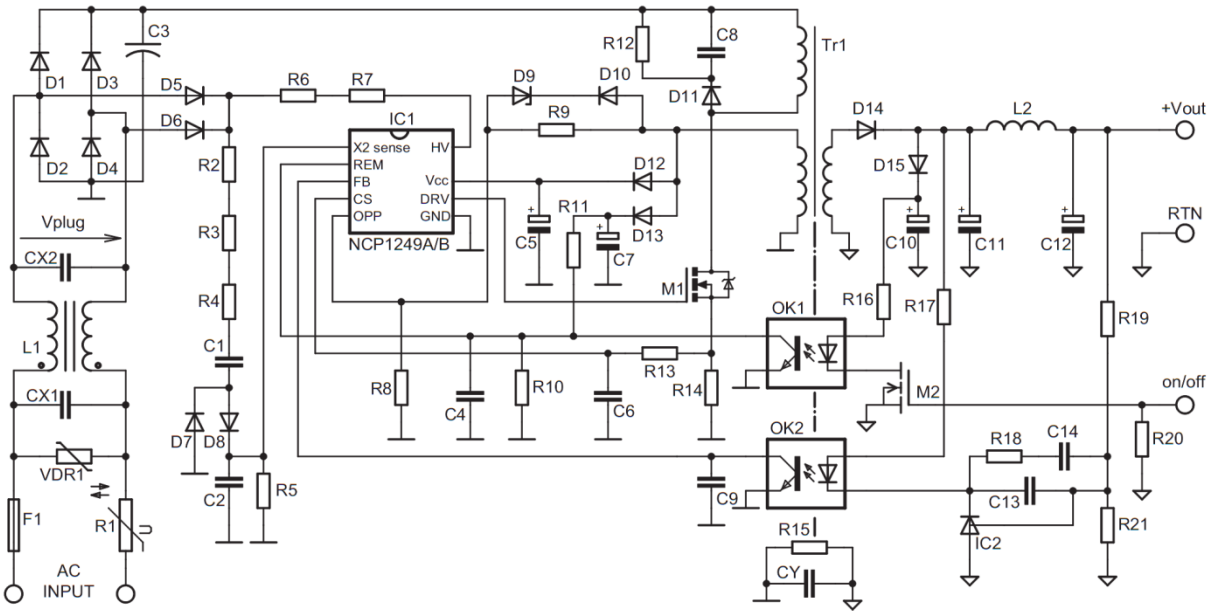

Figure 1. Typical Application Example − NCP1249 (A/B)

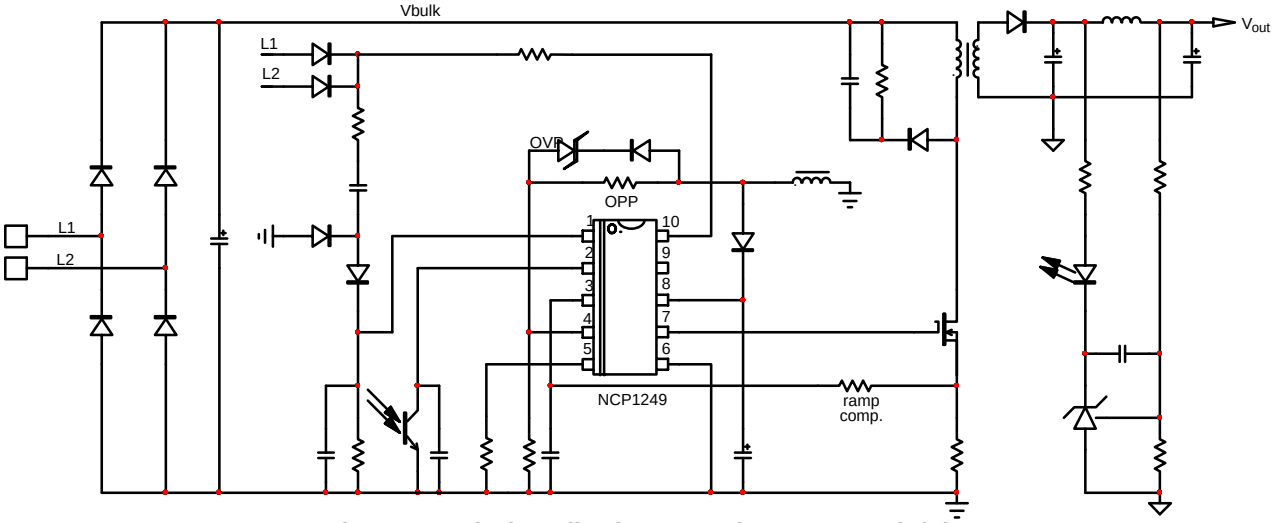

Figure 2. Typical Application Example − NCP1249 (C/D)

Table 1. PIN FUNCTIONS

A/B	C/D	Pin Name	Function	Pin Description
1	1	X2	X2−capacitors discharge	When the voltage on this pin disappears, the controller ensures the X2−capacitors discharge.
2	2	REM	Remote input	Initiates ultra low consumption mode (off−mode) when brought above 8 V (A/B) or below 0.4 V (C/D).
3	2	FB	Feedback pin	Connecting an opto−coupler to this pin allows regulation.
4	3	CS	Current sense + ramp compensation	This pin monitors the primary peak current but also offers a means to introduce slope compensation.
5	4	OPP/Latch	Adjust the Over Power Protection Latches off the part	A resistive divider from the auxiliary winding to this pin sets the OPP compensation level. When brought above 3 V, the part is fully latched off.
6	6	GND	−	The controller ground.
7	7	DRV	Driver output	The driver's output to an external MOSFET gate.
8	8	VCC	Supplies the controller	This pin is connected to an external auxiliary voltage and supplies the controller. When above a certain level, the part fully latches off.
9	9	NC	−	Increases insulation distance between high and low voltage pins.
10	10	HV	High−voltage input	This pin provides a charging current during start−up and auto−recovery faults but also a means to efficiently discharge the input X2 capacitors.
X	5	TIMER	Fault timer adjustment	A resistor to ground adjusts the timer duration in fault condition.

Table 2. MAXIMUM RATINGS TABLE

Symbol	Rating	Value	Unit
V_{cc}	Power Supply voltage, VCC pin, continuous voltage	−0.3 to 30	V
V_{HV}	High Voltage (HV) Pin (pin 10)	–0.3 to 500	V
I_{HV}	High Voltage (pin 10) Input Current	20	mA
Vpin_x	Maximum voltage on low power pins (X2, REM, FB, CS, OPP)	−0.3 to 10	V
V_{DRV}	Maximum voltage on drive pin	−0.3 to V_{cc}+0.3	V
I_{OPP}	Maximum injected current into the OPP pin	−2	mA
$R_{\theta J-A}$	Thermal Resistance Junction−to−Air	211	°C/W
$T_{J,max}$	Maximum Junction Temperature	150	°C
	Storage Temperature Range	−60 to +150	°C
	ESD Capability, HBM model (All pins except HV) per JEDEC standard JESD22, Method A114E	2	kV
	ESD Capability, Machine Model per JEDEC standard JESD22, Method A115A	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.

Table 3. OPTIONS AND ORDERING INFORMATION

Device	Overload Protection	Switching Frequency	Peak Frequency	Package	Shipping†
NCP1249AD65R2G	Latched	65 kHz	130 kHz	SOIC−9 (Pb−Free)	2500 / Tape & Reel
NCP1249BD65R2G	Autorecovery	65 kHz	130 kHz		
NCP1249CD65R2G	Latched	65 kHz	130 kHz		
NCP1249DD65R2G	Autorecovery	65 kHz	130 kHz		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging. Specifications Brochure, BRD8011/D.

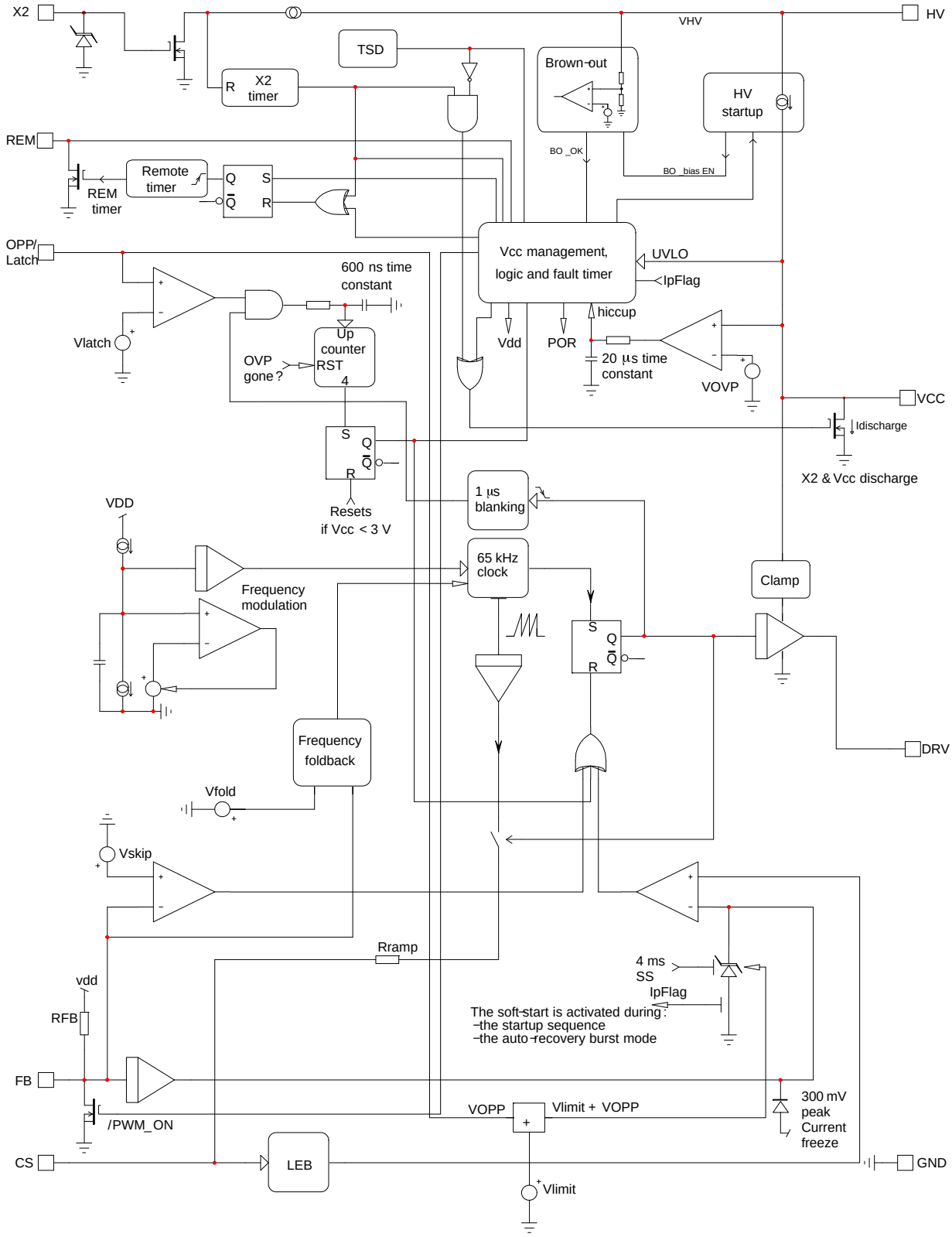

Figure 3. Internal Circuit Architecture − NCP1249 (A/B)

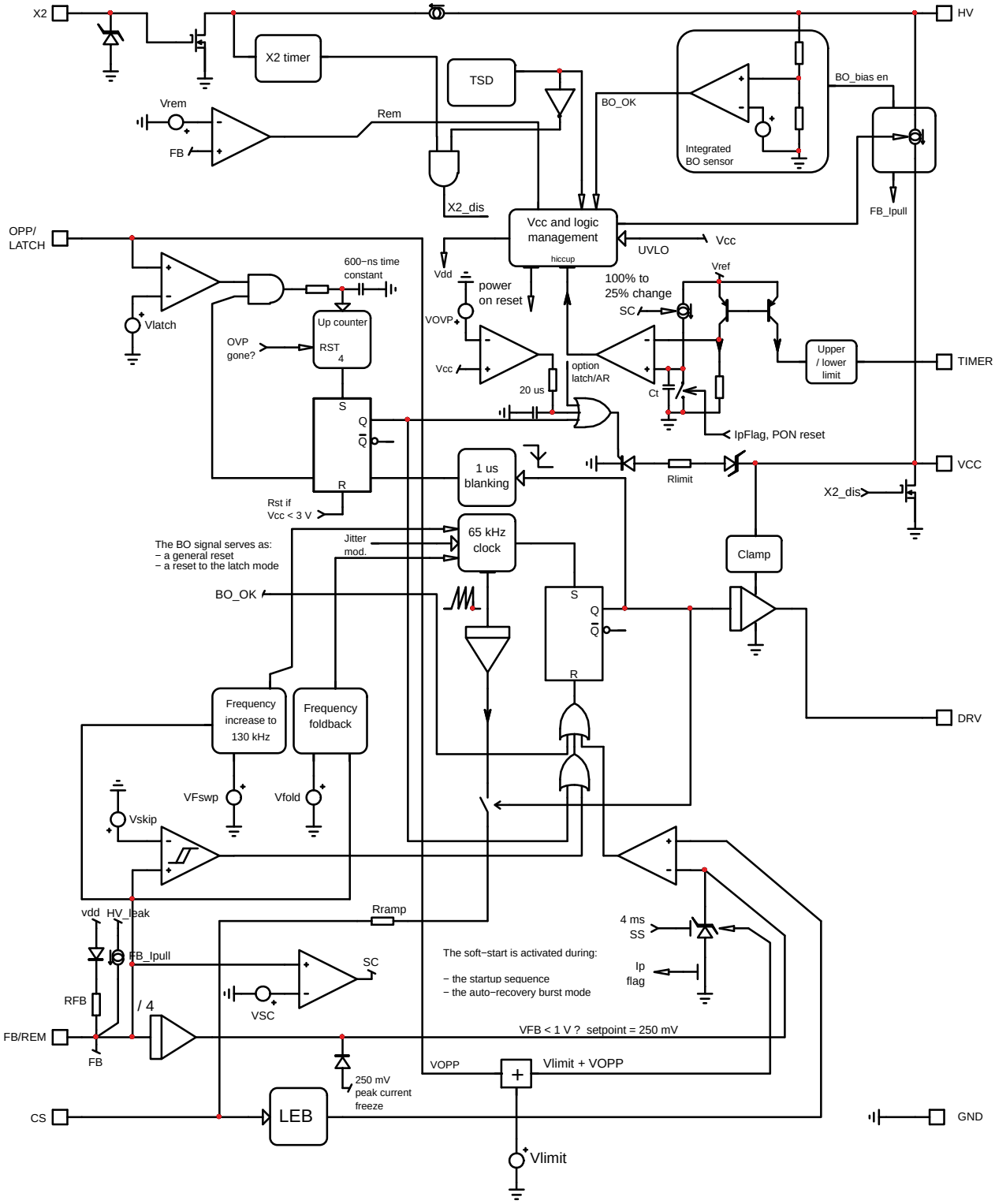

Figure 4. Internal Circuit Architecture − NCP1249 (C/D)

Table 4. ELECTRICAL CHARACTERISTICS
(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
HV STARTUP CURRENT SOURCE						
V_{HV_min}	Minimum voltage for current source operation (V_{CC} = 4V)	10	–	30	60	V
I_{start1}	Current flowing out of VCC pin (V_{CC} = 0 V)	8, 10	0.2	0.7	1	mA
I_{start2}	Current flowing out of VCC pin (V_{CC} = V_{CC_ON} – 0.5 V)	8, 10	6	10	15	mA
$V_{CC_inhibit}$	V_{CC} level for I_{start1} to I_{start2} transition	8	0.5	1	1.25	V
I_{start_off}	Off−state leakage current (V_{HV} = 500 V, V_{CC} = 15 V)	10	–	15	–	μA
$I_{HV_off-mode_1}$	HV pin leakage current when off−mode is active (V_{HV} = 141 V)	10	–	–	15	μA
$I_{HV_off-mode_2}$	HV pin leakage current when off−mode is active (V_{HV} = 325 V)	10	–	–	19	μA
$V_{HV_min_off-mode}$	Minimum voltage on HV pin during off−mode ($V_{_REM}$ = 10V, V_{CC} = 0V)	10	–	–	10	V
SUPPLY SECTION						
V_{CC_ON}	V_{CC} increasing level at which driving pulses are authorized	8	16	18	20	V
V_{CC_OFF}	V_{CC} decreasing level at which driving pulses are stopped	8	9.5	10	11	V
V_{CC_HYST}	Hysteresis V_{CC_ON}− V_{CC_OFF}	8	6	–	–	V
V_{CC_bias}	V_{CC} level during a fault	8	4.7	5.5	6.5	V
I_{CC1}	Internal IC consumption with I_{FB}=75 μA, f_{SW}=65 kHz and C_L = 0	8	–	1.6	2.6	mA
I_{CC2}	Internal IC consumption with I_{FB}=75 μA, f_{SW}=65 kHz and C_L = 1 nF	8	–	2.3	3.4	mA
I_{CC3}	Internal IC consumption with I_{FB}=75 μA, f_{SW}=130 kHz and C_L = 0	8	–	1.9	2.9	mA
I_{CC4}	Internal IC consumption with I_{FB}=75 μA, f_{SW}=130 kHz and C_L = 1 nF	8	–	3.3	4.4	mA
I_{CC_skip}	Internal IC consumption while in skip mode	8	660	960	1360	μA
I_{CC_latch}	Internal IC consumption during Latch – off mode	8	–	350	520	μA
BROWN−OUT						
$V_{_BO_on}$	Brown−Out turn−on threshold (V_{HV} going up)	10	92	101	110	V
$V_{_BO_off}$	Brown−Out turn−off threshold (V_{HV} going down)	10	84	93	102	V
BO_Timer	Timer duration for line cycle drop−out	10	40	–	100	ms
X2 DISCHARGE CIRCUITRY						
V_{th_X2}	X2 timer disable switch threshold voltage	1	1	1.5	2	V
$V_{th_X2_hyst}$	Hysteresis on the X2 pin	1	–	100	–	mV
$V_{_X2_clamp}$	X2 input clamp voltage	1	–	4	–	V
X2_Timer	X2 timer duration	1	70	–	140	ms
$I_{_X2_leak}$	X2 input leakage current ($V_{_X2}$ = 2.5 V)	1	–	–	0.3	μA
$I_{_X2_dis}$	Maximum discharge switch current (V_{CC} = 10V)	10	6	10	13	mA
DRIVE OUTPUT						
T_r	Output voltage rise−time @ C_L = 1 nF, 10−90% of output signal	7	–	40	80	ns
T_f	Output voltage fall−time @ C_L = 1 nF, 10−90% of output signal	7	–	30	70	ns
R_{OH}	Source resistance	7	–	13	–	Ω
R_{OL}	Sink resistance	7	–	6	–	Ω
I_{source}	Peak source current, V_{GS} = 0 V – note 1	7		300		mA
I_{sink}	Peak sink current, V_{GS} = 12 V – note 1	7		500		mA

2. Guaranteed by design
3. See characterization table for linearity over negative bias voltage – we recommend keeping the level on pin 5 below −300 mV.
4. A 1−MΩ resistor is connected from pin 4 to the ground for the measurement.

*C/D version

Table 4. ELECTRICAL CHARACTERISTICS
(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
DRIVE OUTPUT						
V_{DRV_low}	DRV pin level at V_{CC} close to V_{CC_OFF} with a 33−kΩ resistor to GND	7	8	−	−	V
V_{DRV_high}	DRV pin level at V_{CC}= V_{OVP} −0.2 V, DRV unloaded	7	10	12	14	V
CURRENT COMPARATOR						
I_{IB}	Input Bias Current @ 0.8 V input level on pin 4	4, 3*		0.02		μA
V_{limit}	Maximum internal current setpoint – Tj = 25 °C – pin 5 grounded	4, 3*	0.744	0.8	0.856	V
V_{limit}	Maximum internal current setpoint – Tj from −40° to 125°C – pin 5 grounded	4, 3*	0.72	0.8	0.88	V
V_{fold_cs}	Default internal voltage set point for frequency foldback trip point ≈ 47% of V_{limit}	4, 3*		475		mV
V_{freeze_cs}	Internal peak current setpoint freeze (≈31% of V_{limit})	4, 3*		250		mV
T_{DEL}	Propagation delay from current detection to gate off−state	4, 3*		100	150	ns
T_{LEB}	Leading Edge Blanking Duration	4, 3*		300		ns
T_{SS}	Internal soft−start duration activated upon startup, auto−recovery	−		4		ms
I_{OPPo}	Setpoint decrease for pin 5 biased to –250 mV – (Note 2)	4, 3*		31.3		%
I_{OOPv}	Voltage setpoint for pin 5 biased to −250 mV – (Note 2) Tj from −40° to 125 °C	4, 3*	0.5	0.55	0.62	V
I_{OPPs}	Setpoint decrease for pin 5 grounded	4, 3*		0		%
INTERNAL OSCILLATOR						
f_{OSC_nom}	Oscillation frequency, V_{FB} < $V_{FBtrans}$, pin 5 grounded	−, 4*	57	65	71	kHz
$V_{FBtrans}$	Feedback voltage above which f_{sw} increases	3, 2*		3.2		V
f_{OSC_max}	Maximum oscillation frequency for V_{FB} above V_{FBmax}	−	115	130	140	kHz
V_{FBmax}	Feedback voltage above which f_{sw} is constant	3, 2*	3.8	4	4.2	V
D_{max}	Maximum duty ratio	−	76	80	84	%
f_{jitter}	Frequency jittering in percentage of f_{OSC}	−		±5		%
f_{swing}	Swing frequency over the whole frequency range	−		240		Hz
REMOTE SECTION						
$V_{_REM_on}$ (A/B)	Remote pin voltage below which is the off−mode deactivated (V_{REM} going down) (V_{CC} = 0 V)	2	1	1.5	2	V
$V_{_REM_off}$ (A/B)	Remote pin voltage above which is the off−mode activated (V_{REM} going up)	2	7.2	8	8.8	V
$V_{_REM_off}$ (C/D)	Feedback voltage below which the part enters into off−mode	2		0.4		V
$V_{_REM_on}$ (C/D)	Feedback voltage above which is the off−mode deactivated	2	1.5	2	2.5	V
I_{FBREM} (C/D)	Feedback current that lifts the feedback pin upon off−mode exit	2		2.4	4	μA
REM_Timer	Remote timer duration	2	70	−	140	ms
$R_{_SW_REM}$	Internal remote pull down switch resistance	2	1000	−	3000	Ω
$I_{_REM_leak}$	Remote input leakage current (V_{REM} = 9 V) (Note 1)	2	−	0.02	1	μA
FEEDBACK SECTION						
$R_{up(FB)}$	Internal pull−up resistor	3, 2*		17		kΩ
R_{eq}	Equivalent ac resistor from FB to gnd	3, 2*	10	15	20	kΩ

2. Guaranteed by design
3. See characterization table for linearity over negative bias voltage – we recommend keeping the level on pin 5 below −300 mV.
4. A 1−MΩ resistor is connected from pin 4 to the ground for the measurement.

*C/D version

Table 4. ELECTRICAL CHARACTERISTICS
(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
FEEDBACK SECTION						
I_{ratio}	Pin 3 to current setpoint division ratio	3,4, (2,3)*		4		−
V_{freeze_FB}	Feedback voltage below which the peak current is frozen	3, 2*		1		V
FREQUENCY FOLDBACK						
V_{fold_FB}	Frequency foldback level on the feedback pin – ≈47% of maximum peak current	3, 2*		1.9		V
f_{trans}	Transition frequency below which skip−cycle occurs	−	22	26	30	kHz
V_{fold_end}	End of frequency foldback feedback level, $f_{sw} = f_{min}$	3, 2*		1.5		V
V_{skip}	Skip−cycle level voltage on the feedback pin	3, 2*		400		mV
Skip hysteresis	Hysteresis on the skip comparator – note 1	3, 2*		30		mV
INTERNAL SLOPE COMPENSATION						
V_{ramp}	Internal ramp level @ 25°C – note 3	4, 3*		2.5		V
R_{ramp}	Internal ramp resistance to CS pin	4, 3*		20		kΩ
PROTECTIONS						
V_{latch}	Latching level input	5, 4*	2.7	3	3.3	V
$T_{latch-blank}$	Blanking time after drive turn off	5, 4*		1		μs
$T_{latch-count}$	Number of clock cycles before latch confirmation	−		4		−
$T_{latch-del}$	OVP detection time constant	5, 4*		600		ns
V_{OVL}	Feedback voltage at which an overload is considered – OPP pin is grounded	3, 2*		3.2		V
V_{SC}	Feedback voltage above which a short−circuit is considered	3, 2*	3.9	4.1	4.3	V
$Timer_1$ (A/B)	Fault timer duration when $3.2 < V_{FB} < 4.1$ V − overload	−	100	200	300	ms
$Timer_2$ (A/B)	Fault timer duration when $V_{FB} > 4.1$ V is $Timer_1/4$ – short−circuit condition	−	25	50	75	ms
$Timer_1$ (C/D)	Fault timer duration for a 22 kΩ resistor from pin 5 to ground − overload	5*	350	500	650	ms
$Timer_2$ (C/D)	Fault timer duration when $V_{FB} > 4.1$ V is $Timer_1/4$ – short−circuit condition	5*	88	125	162	ms
$Timer_{_fault1}$ (C/D)	Timer duration when pin 5 is shorted to ground – fault condition	5*		50		ms
$Timer_{_fault2}$ (C/D)	Timer duration when pin 5 is open – fault condition	5*		1000		ms
V_{OVP}	Latched Over voltage protection on the V_{cc} rail	8	26	27.5	29	V
T_{OVP_del}	Delay before OVP on V_{cc} confirmation	8		20	30	μs
T_{A-rec_timer}	Auto−recovery timer duration	−	0.7	−	−	s
TEMPERATURE SHUTDOWN						
T_{TSD}	Temperature shutdown T_J going up	−		150		°C
$T_{TSD(HYS)}$	Temperature shutdown hysteresis	−		30		°C

2. Guaranteed by design
3. See characterization table for linearity over negative bias voltage – we recommend keeping the level on pin 5 below −300 mV.
4. A 1−MΩ resistor is connected from pin 4 to the ground for the measurement.

*C/D version

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

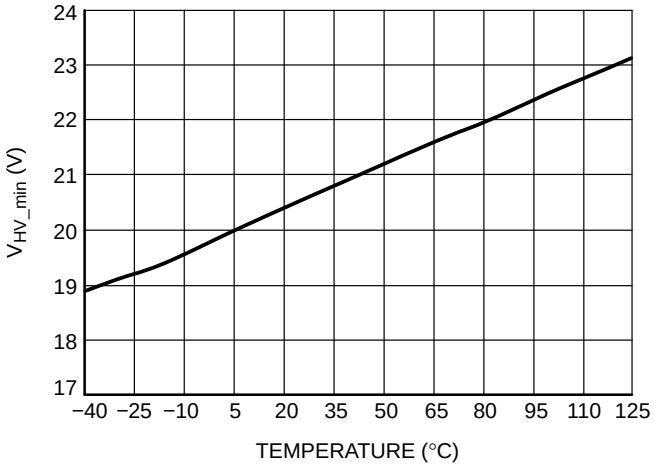

Figure 5. Minimum Current Source Operation, V_{HV_min}

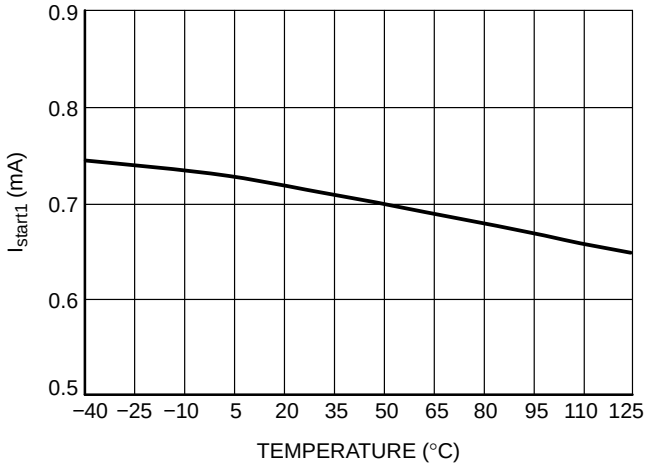

Figure 6. High Voltage Startup Current Flowing Out of V_{CC} pin, I_{start1}

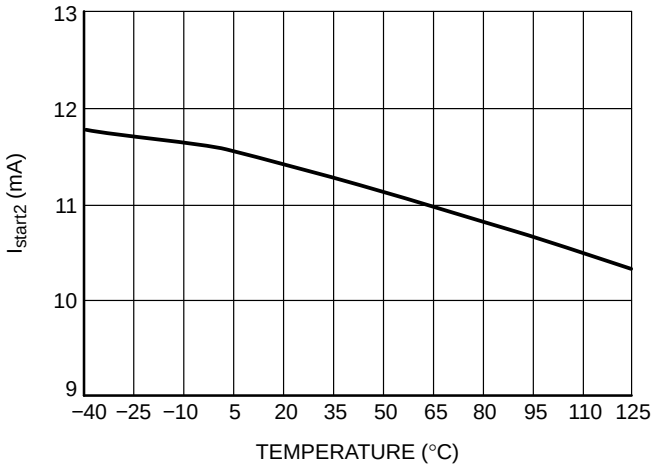

Figure 7. High Voltage Startup Current Flowing Out of VCC Pin, I_{start2}

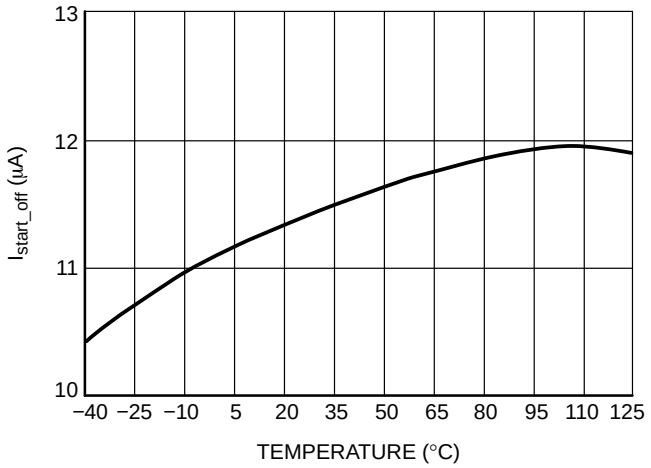

Figure 8. Off−state Leakage Current, I_{start_off}

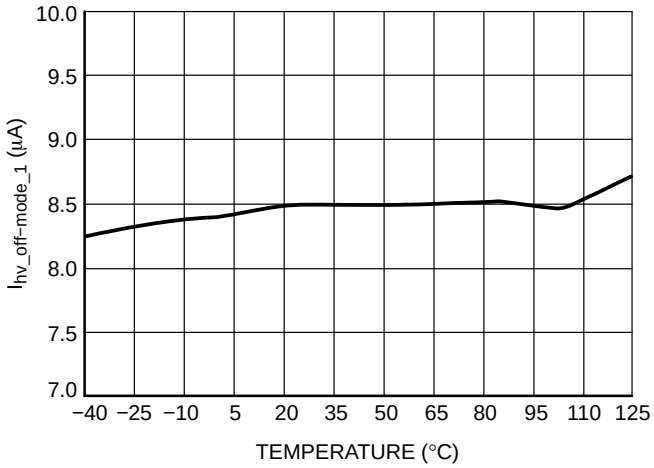

Figure 9. HV Pin Current during Off−mode, $I_{HV_off_mode_1}$

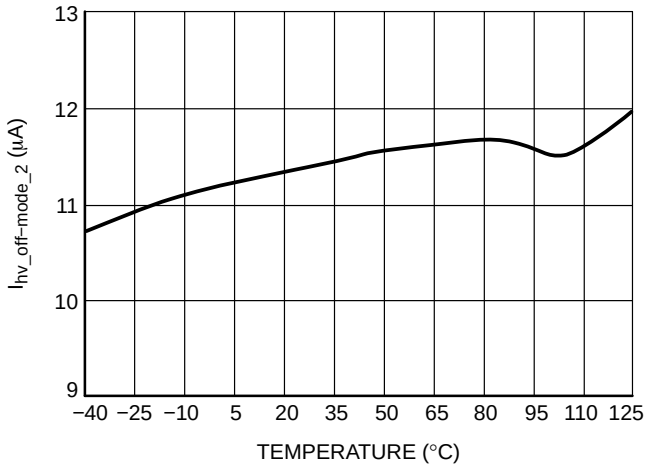

Figure 10. HV Pin Current during Off−mode, $I_{HV_off_mode_2}$

TYPICAL CHARACTERISTICS

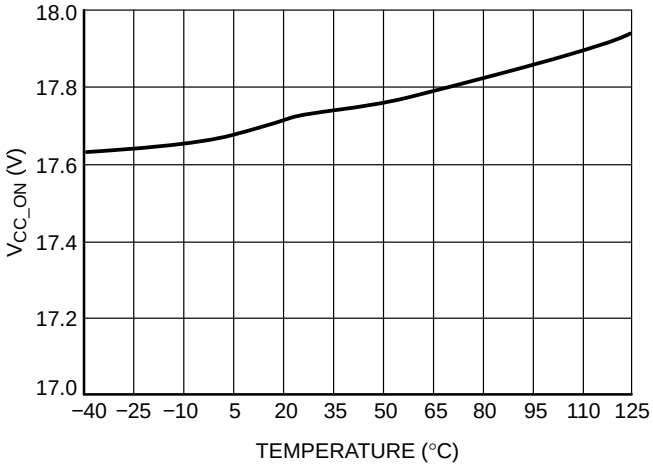

Figure 11. V_{CC} Increasing Level at which Driving Pulses are Authorized, V_{CC_ON}

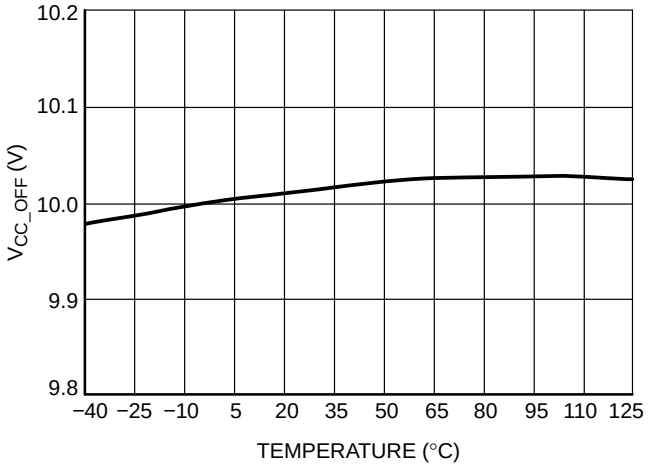

Figure 12. V_{CC} Decreasing Level at which Driving Pulses are Stopped, V_{CC_OFF}

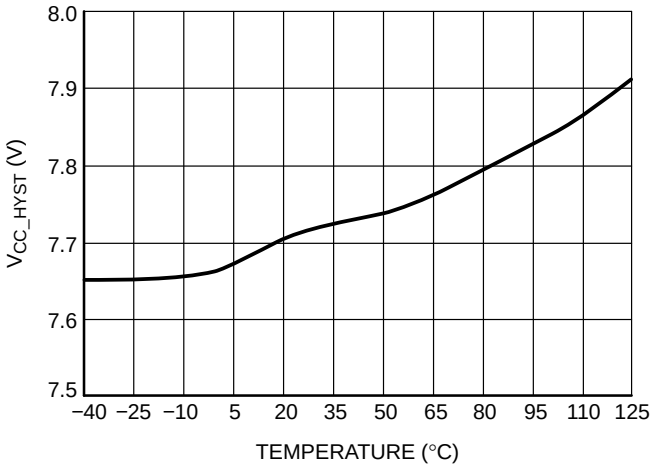

Figure 13. V_{CC} Hysteresis, V_{CC_HYST}

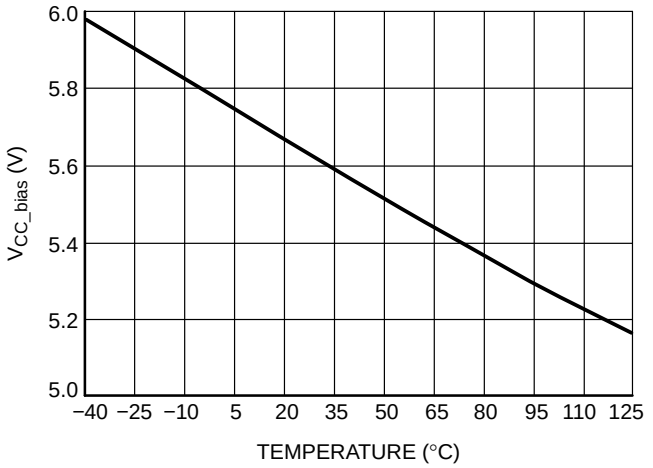

Figure 14. V_{CC} Level at Fault Modes, V_{CC_Bias}

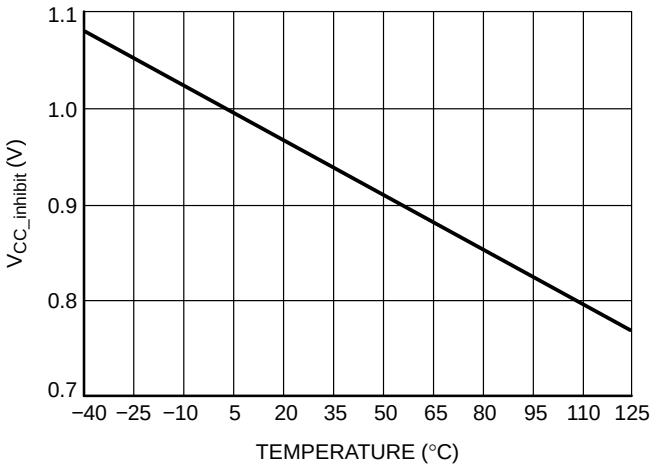

Figure 15. V_{CC} Level for I_{start1} to I_{start2} Transition, $V_{CC_inhibit}$

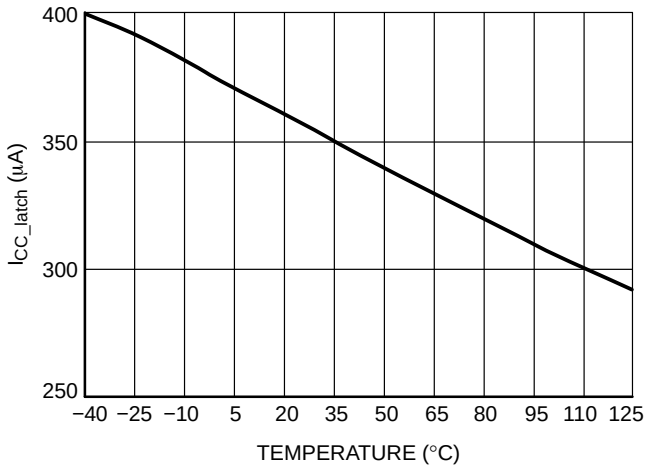

Figure 16. Internal IC Consumption during Latch−off Mode, I_{CC_latch}

TYPICAL CHARACTERISTICS

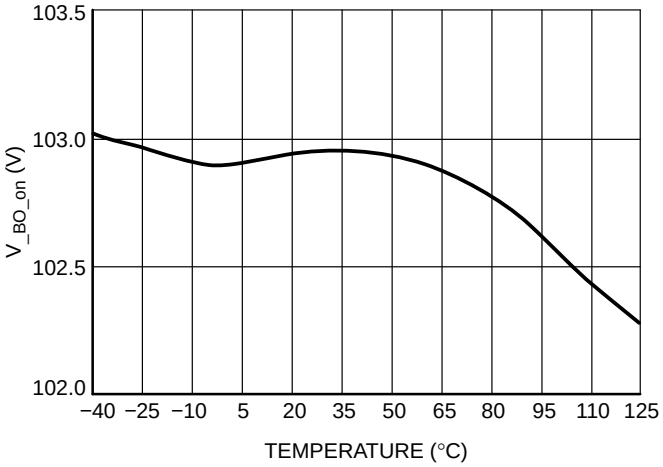

Figure 17. Brown−Out Turn−on Threshold, $V_{_BO_on}$

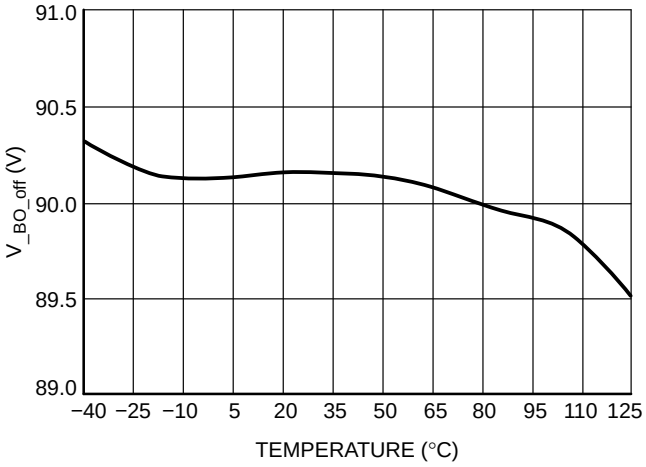

Figure 18. Brown−Out Turn−off Threshold, $V_{_BO_off}$

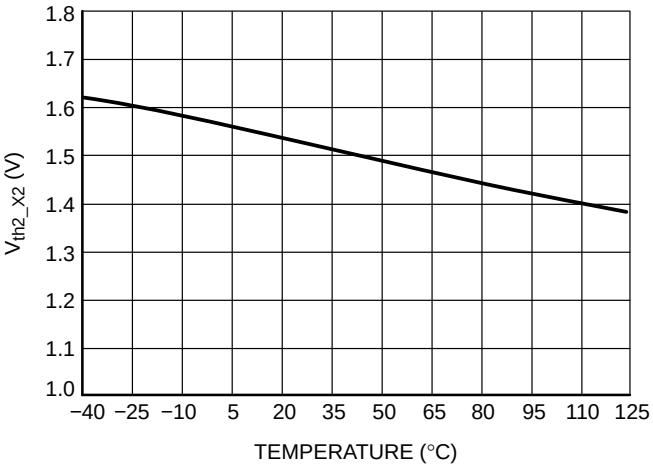

Figure 19. X2 Timer Disable Switch Threshold, V_{th_X2}

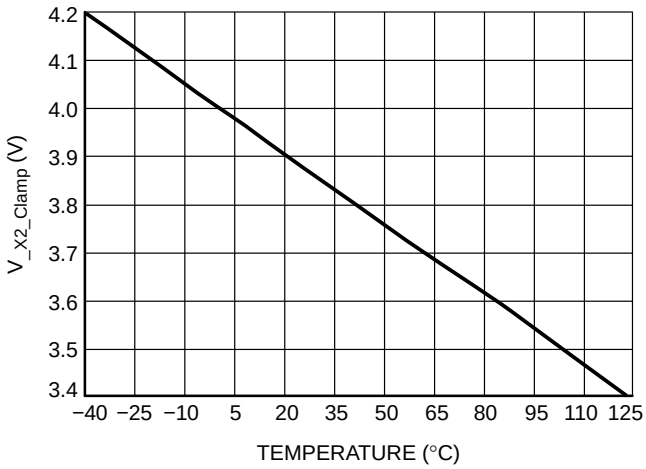

Figure 20. X2 Input Clamp Voltage, $V_{_X2_clamp}$

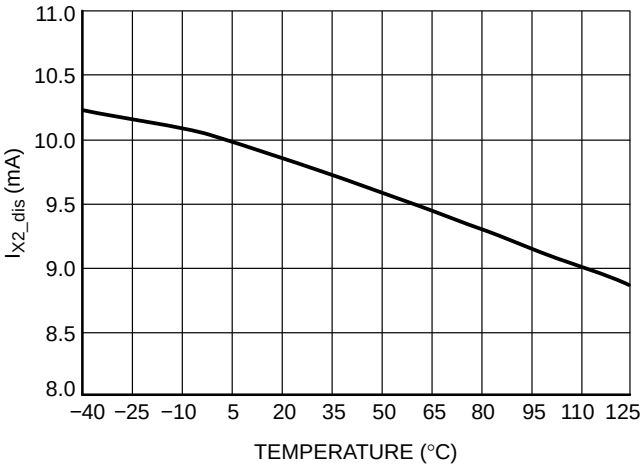

Figure 21. Maximum X2 Cap Discharge Current, $I_{_X2_dis}$

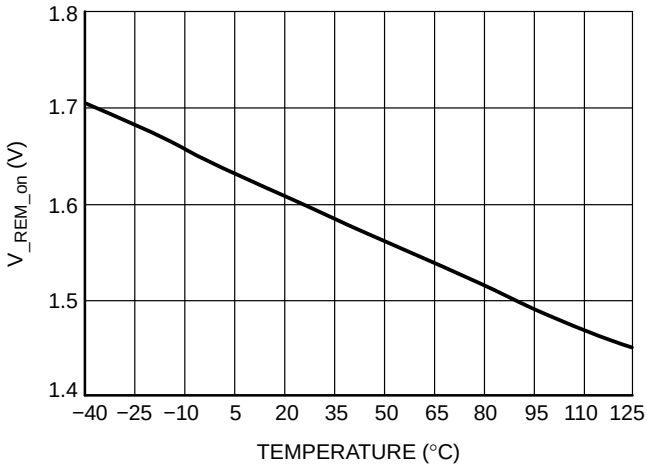

Figure 22. Off−mode Turn−off Threshold, $V_{_REM_on}$, A/B Version

TYPICAL CHARACTERISTICS

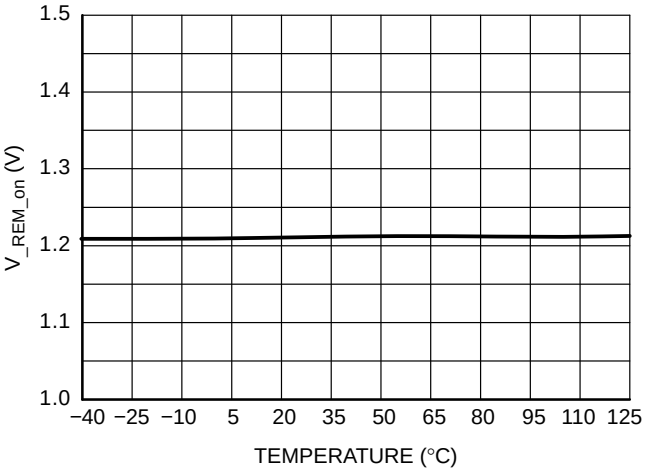

Figure 23. Off−mode Turn−off Threshold, $V_{_REM_on}$, C/D Version

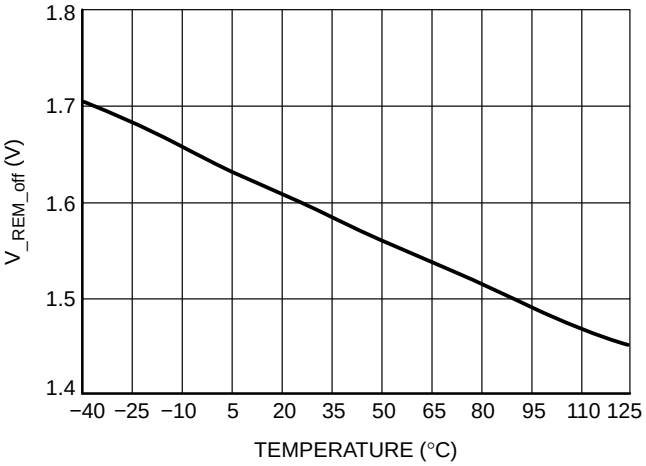

Figure 24. Off−mode Turn−on Threshold, $V_{_REM_off}$, A/B Version

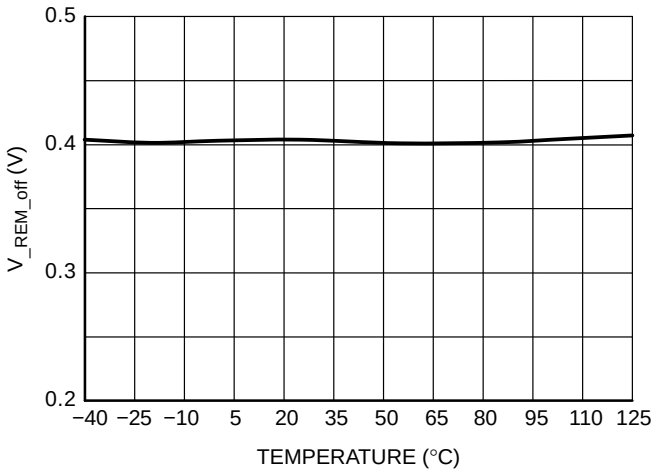

Figure 25. Off−mode Turn−on Threshold, $V_{_REM_off}$

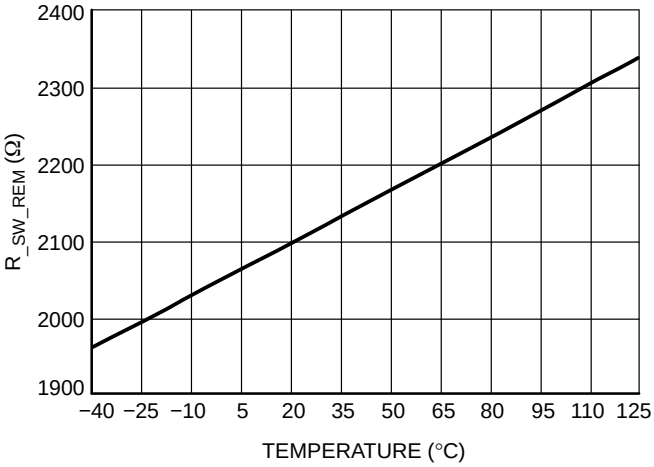

Figure 26. Internal Remote Pull Down Switch Resistance, $R_{_SW_REM}$

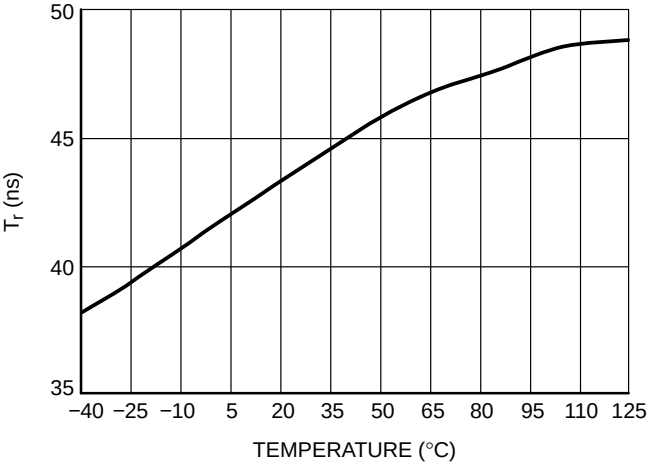

Figure 27. Output Voltage Rise−time, T_r

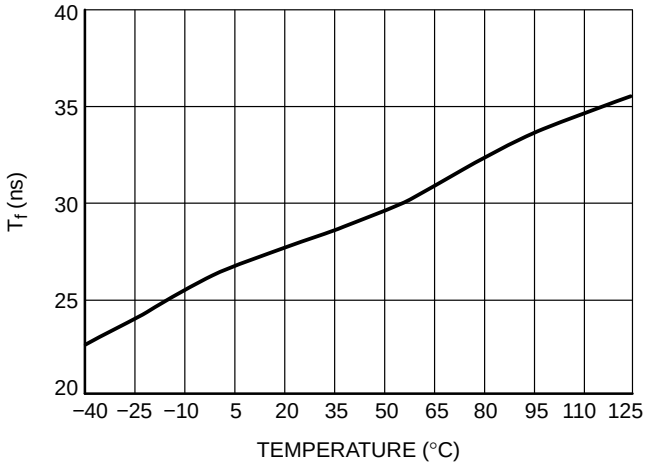

Figure 28. Output Voltage Fall−time, T_f

TYPICAL CHARACTERISTICS

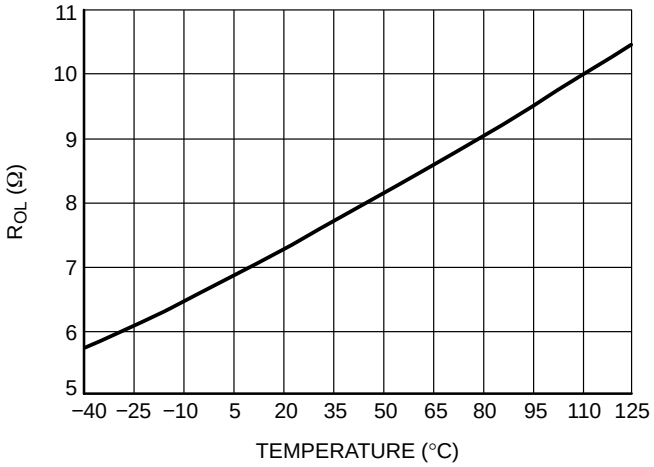

Figure 29. Source Resistance, R_{OL}

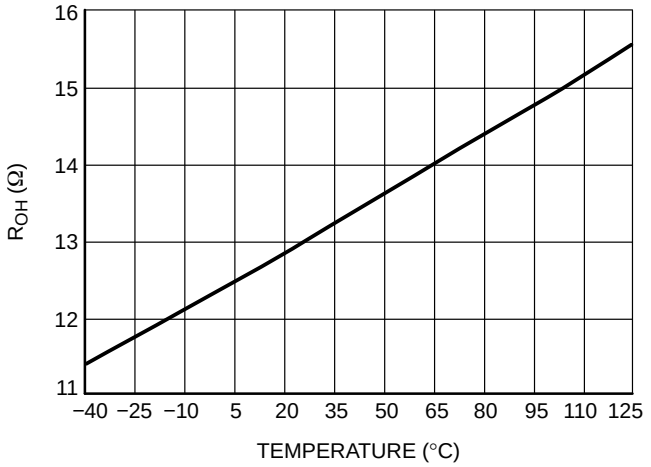

Figure 30. Sink Resistance, R_{OH}

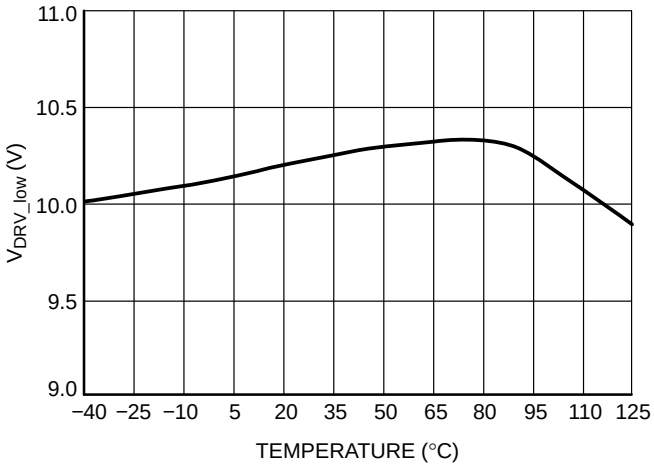

Figure 31. DRV Pin Level at V_{CC} Close to V_{CC_OFF}, V_{DRVlow}

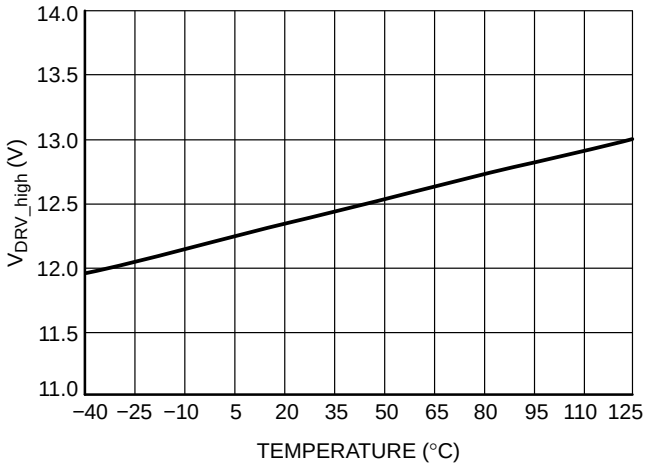

Figure 32. DRV Pin Level at V_{CC} Close to V_{OVP}, $V_{DRVhigh}$

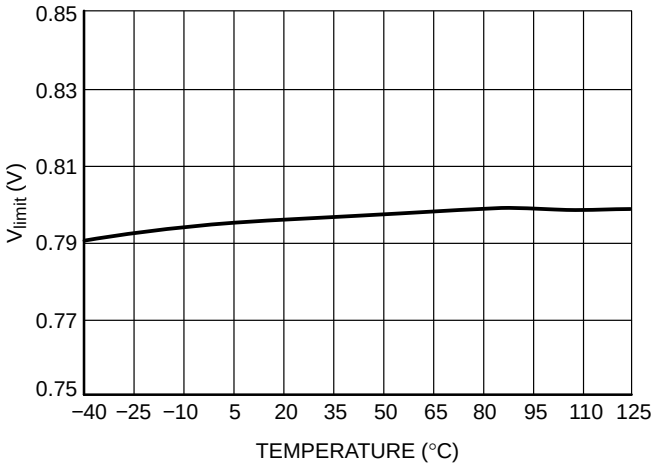

Figure 33. Maximum Internal Current Set−point, V_{limit}

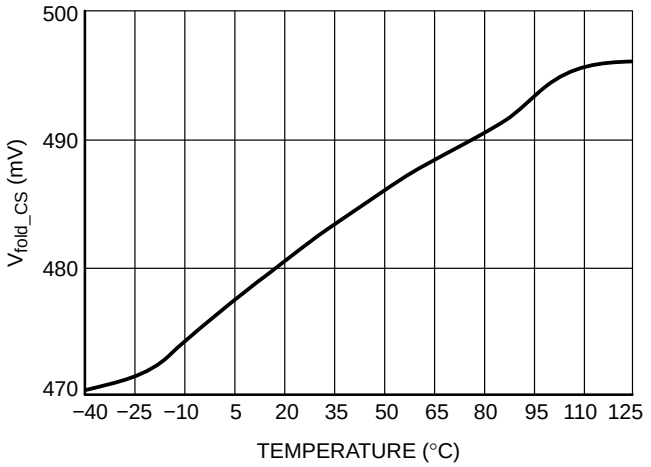

Figure 34. Default Internal Voltage Set Point for Frequency Foldback, V_{fold_CS}

TYPICAL CHARACTERISTICS

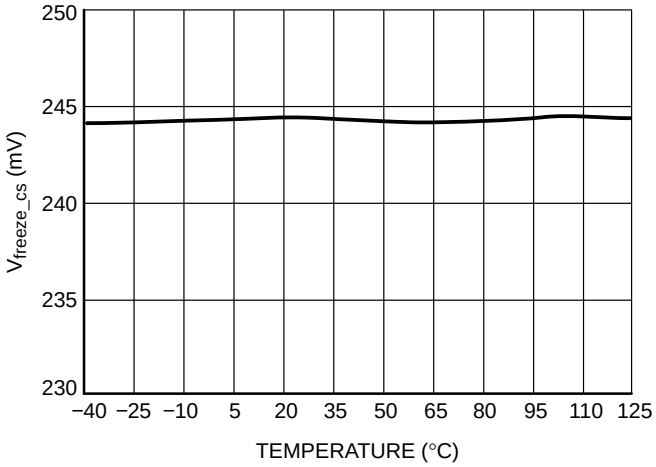

Figure 35. Internal Peak Current Set−point Freeze, V_{freeze_CS}

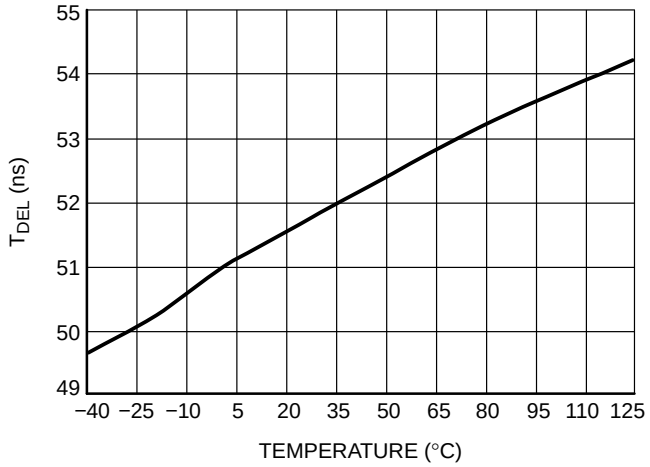

Figure 36. Propagation Delay from Current Detection to Gate Off−state, T_{DEL}

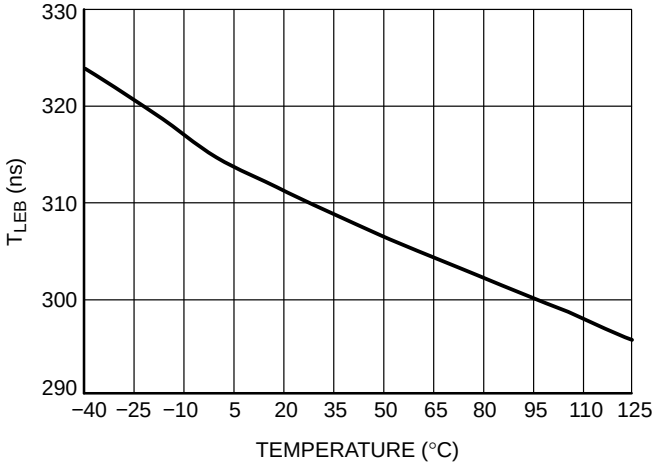

Figure 37. Leading Edge Blanking Duration, T_{LEB}

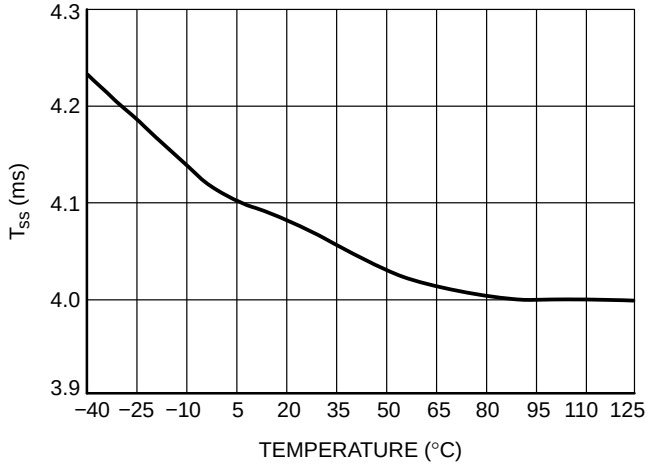

Figure 38. Internal Soft−start Duration, T_{ss}

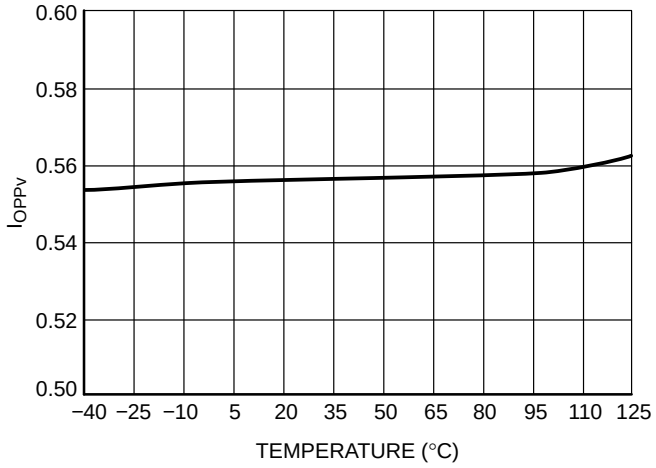

Figure 39. CS Voltage Setpoint for OPP, I_{OPPv}

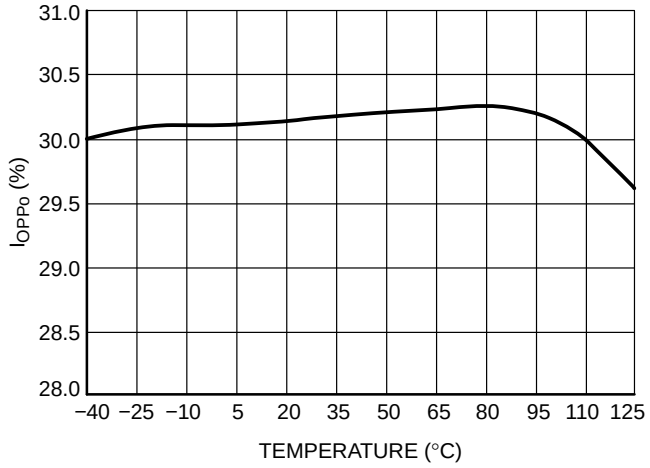

Figure 40. Set−point Decrease for OPP, I_{OPPo}

TYPICAL CHARACTERISTICS

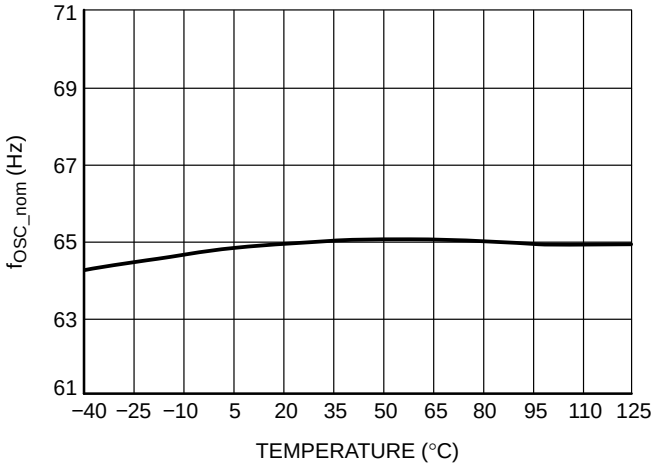

Figure 41. Oscillation Frequency, f_{OSC_nom}

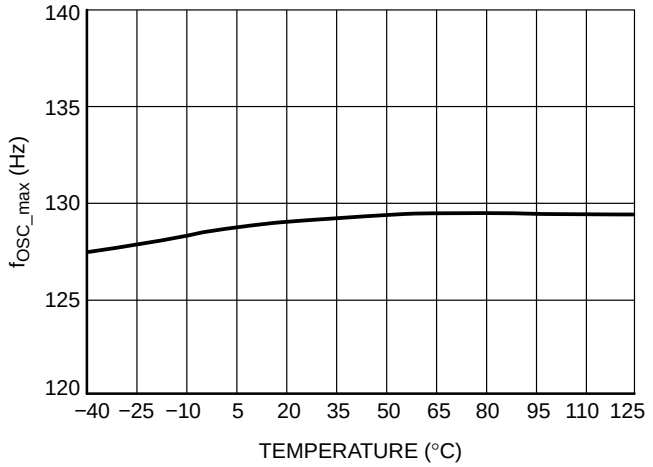

Figure 42. Maximum Oscilation Frequency, f_{OSC_max}

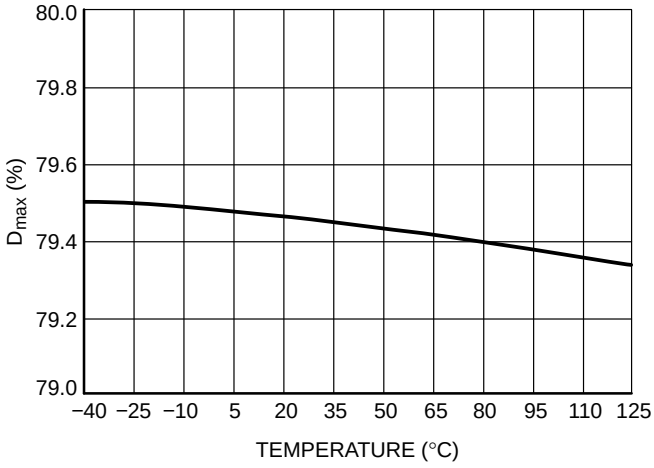

Figure 43. Maximum Duty−cycle, D_{max}

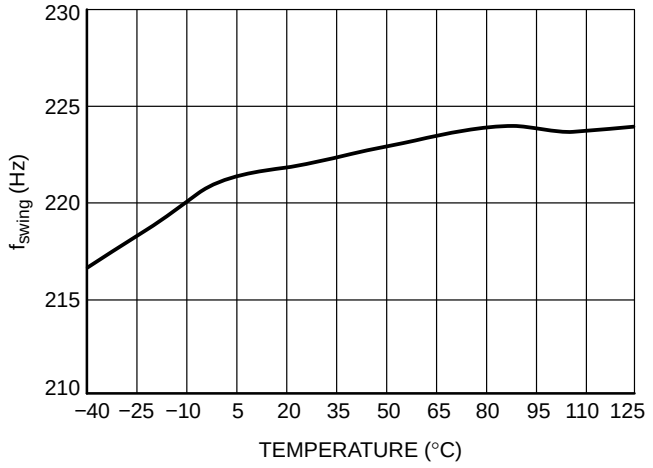

Figure 44. Swing Frequency, f_{swing}

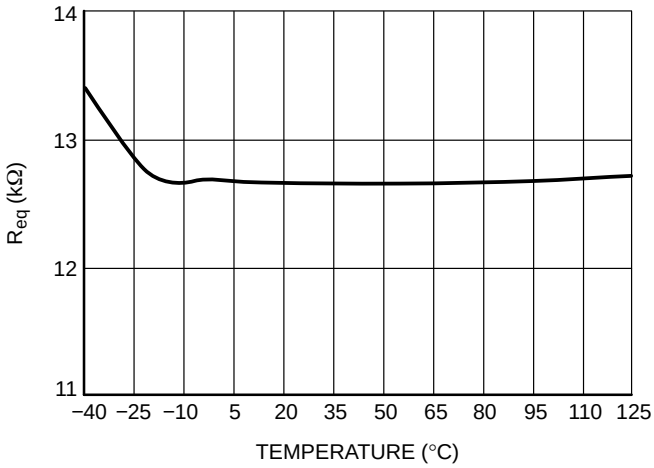

Figure 45. Equivalent ac Resistor from FB to GND, R_{eq}

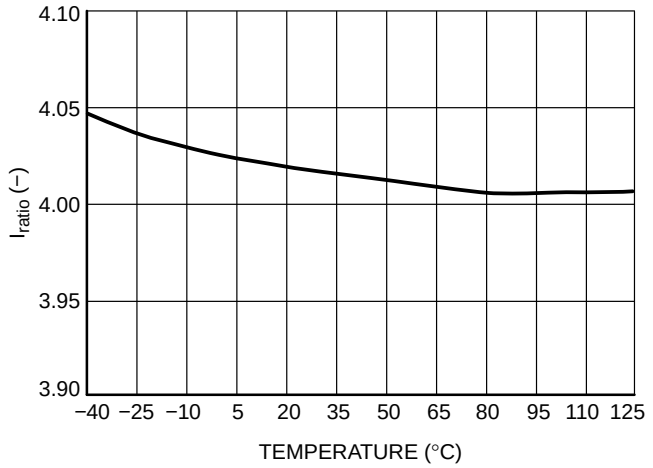

Figure 46. FB to Current Set−point Division Ratio, I_{ratio}

TYPICAL CHARACTERISTICS

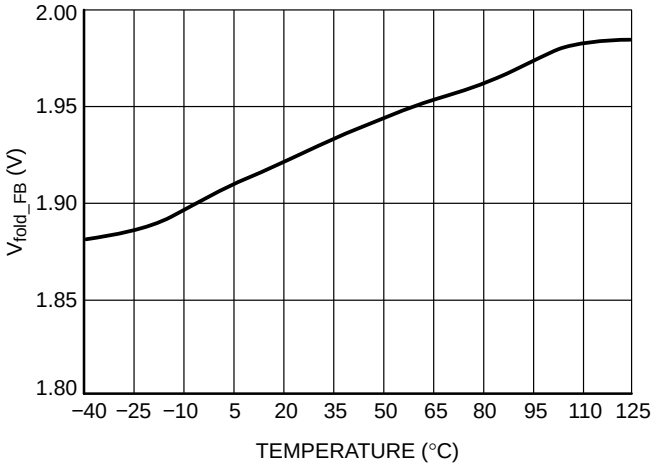

Figure 47. Frequency Foldback Level, V_{fold_FB}

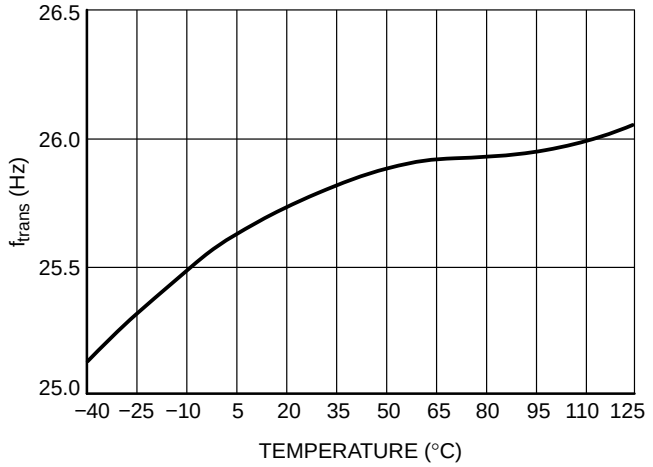

Figure 48. Transition Frequency below which Skip−cycle Occurs, f_{trans}

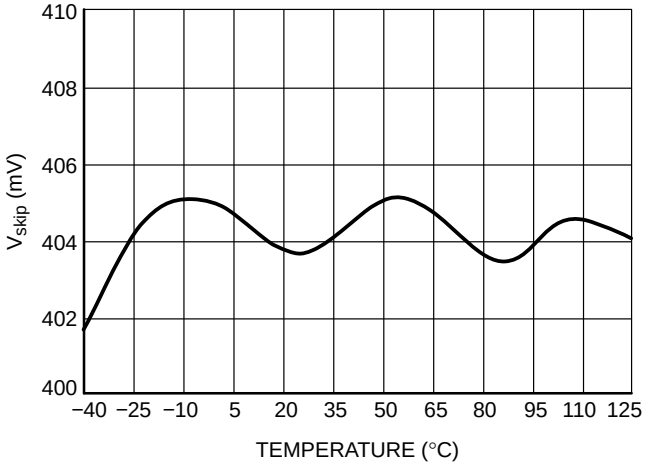

Figure 49. Skip−cycle Level Voltage on the Feedback Pin, V_{skip}

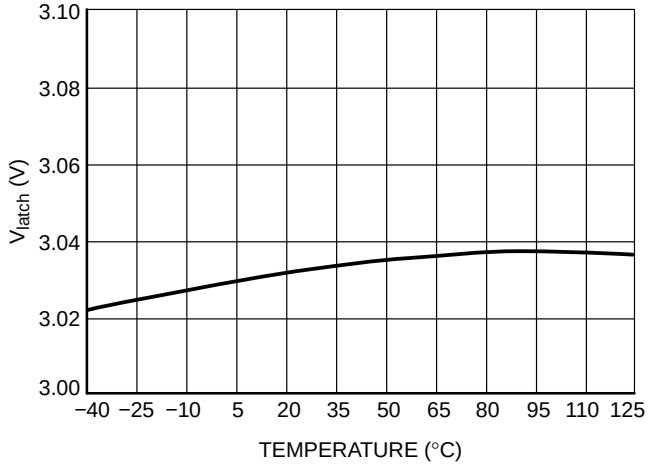

Figure 50. Latching Level Input, V_{latch}

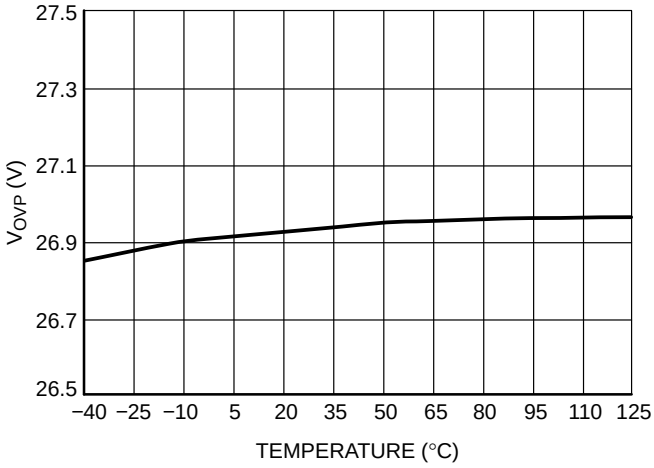

Figure 51. Over Voltage Protection on V_{CC} rail, V_{OVP}

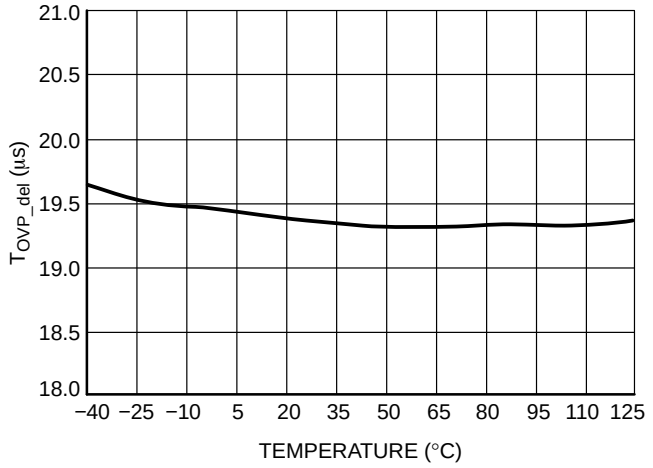

Figure 52. OVP Detection Time Constant, T_{OVP_del}

TYPICAL CHARACTERISTICS

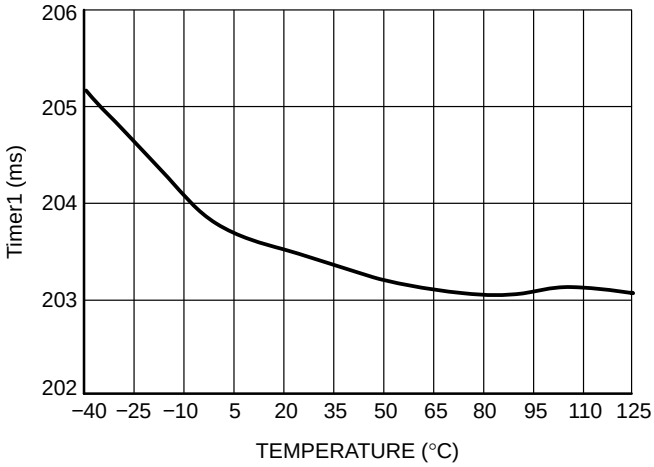

Figure 53. Fault Timer Duration − Overload, Timer1, A/B Version

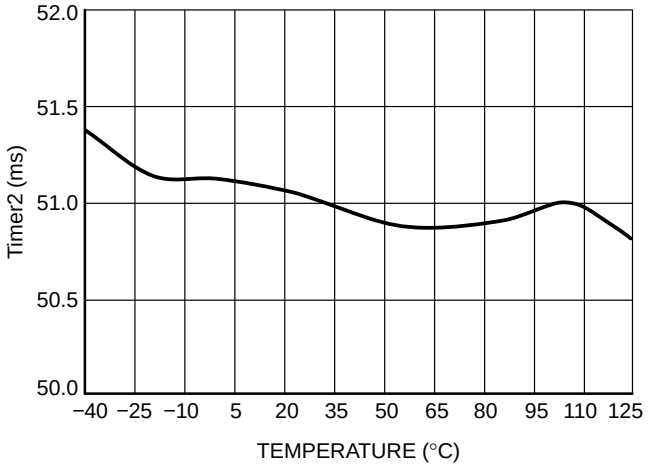

Figure 54. Fault Timer Duration − Short−circuit Condition, Timer2, A/B Version

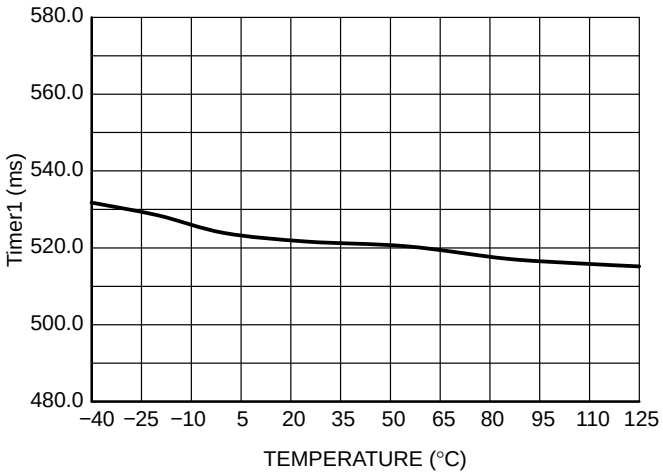

Figure 55. Fault Timer Duration − Overload, Timer1, C/D Version

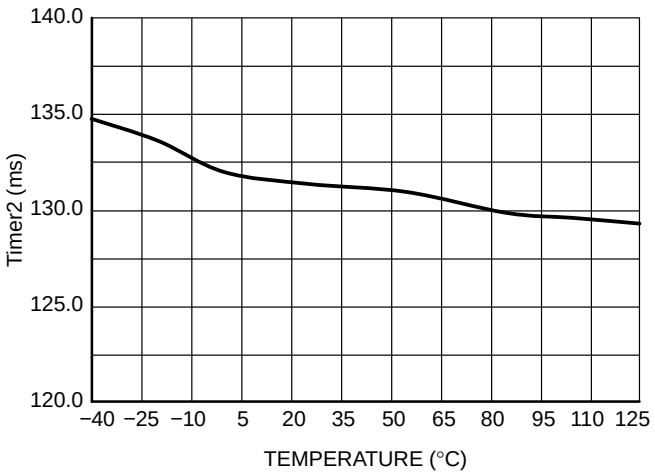

Figure 56. Fault Timer Duration − Short−circuit Condition, Timer2, C/D Version

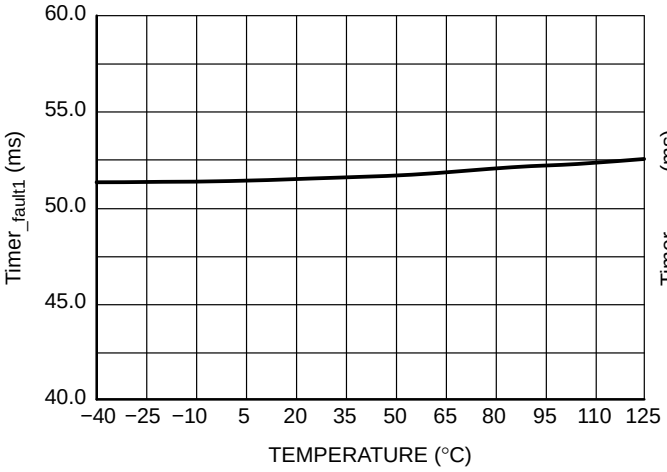

Figure 57. Fault Timer Duration when Pin 5 is Shorted to Ground − Fault Condition, Timer$_{_fault1}$, C/D Version

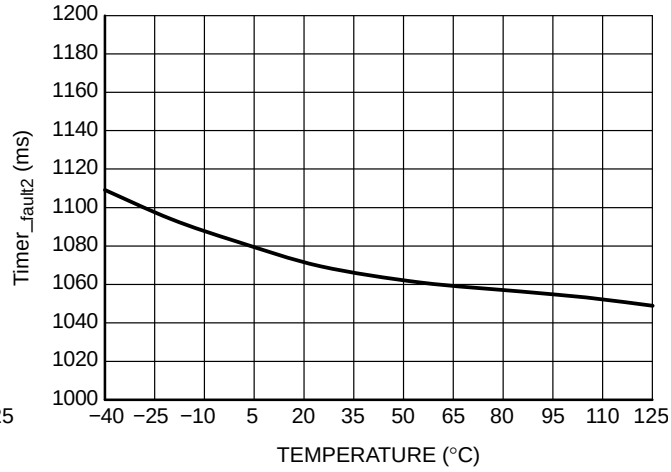

Figure 58. Fault Timer Duration when Pin 5 is Open − Fault Condition, Timer$_{_fault2}$, C/D Version

TYPICAL CHARACTERISTICS

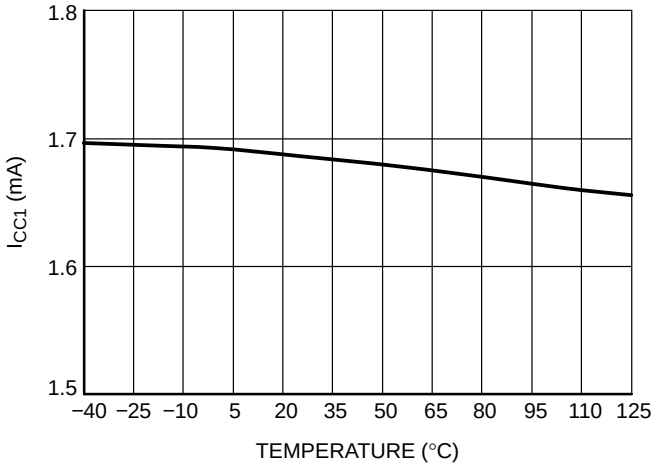

Figure 59. Internal IC Consumption, I_{CC1}

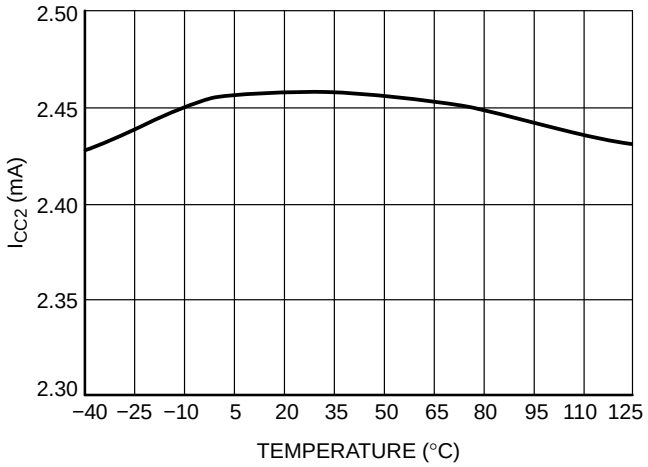

Figure 60. Internal IC Consumption, I_{CC2}

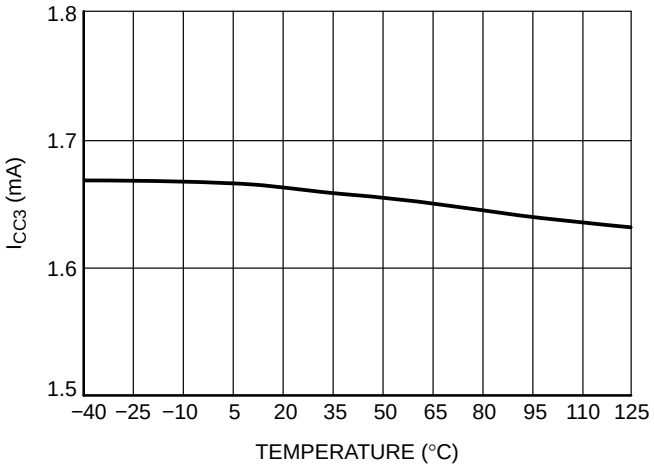

Figure 61. Internal IC Consumption, I_{CC3}

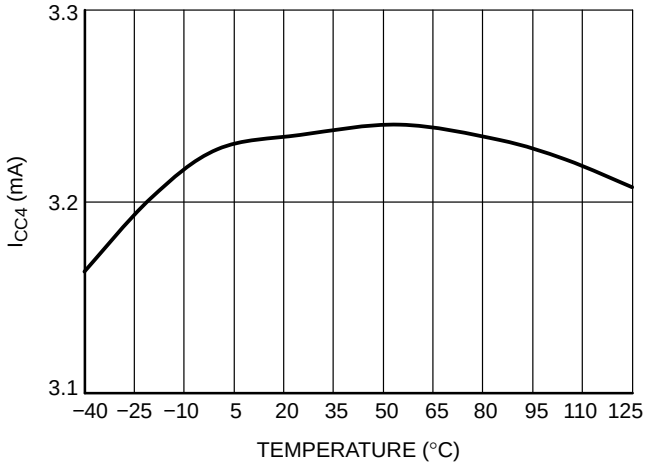

Figure 62. Internal IC Consumption, I_{CC4}

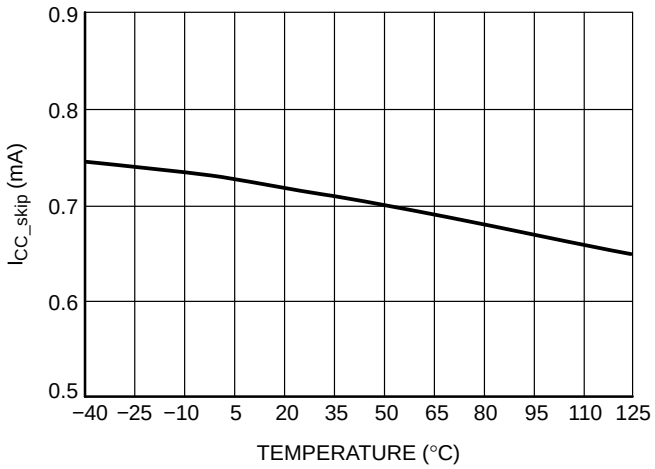

Figure 63. Internal IC Consumption during Skip Mode, I_{CC_skip}

APPLICATION INFORMATION

Introduction

The NCP1249 implements a standard current mode architecture where the switch−off event is dictated by the peak current setpoint. This component represents the ideal candidate where low part−count and cost effectiveness are the key parameters, particularly in low−cost ac−dc adapters, open−frame power supplies etc. The NCP1249 brings all the necessary components normally needed in today modern power supply designs, bringing several enhancements such as a non−dissipative OPP, a brown−out protection or peak power excursion for loads exhibiting variations over time. Accounting for the new needs of extremely low standby power requirements, the part includes an automatic X2−capacitor discharge circuitry that prevents the designer from installing power−consuming resistors across the front−end filtering capacitors. The controller is also able to enter a deep sleep mode via its dedicated remote pin.

- **High−Voltage start−up:** low standby power results cannot be obtained with the classical resistive start−up network. In this part, a high−voltage current−source provides the necessary current at start−up and turns off afterwards.
- **Internal Brown−Out protection:** a portion of the bulk voltage is internally sensed via the high−voltage pin monitoring (pin 10). When the voltage on this pin is too low, the part stops pulsing. No re−start attempt is made until the controller senses that the voltage is back within its normal range. When the brown−out comparator senses the voltage is acceptable, it sends a general reset to the controller (de−latch occurs) and authorizes to re−start.
- **X2−capacitors discharge capability:** per IEC−950 standard, the time constant of the front−end filter capacitors and their associated discharge resistors must be less than 1 s. This is to avoid electrical stress when the user unplugs the converter and inadvertently touches the power cord terminals. By providing an automatic means to discharge the X2 capacitors, the NCP1249 prevents the designer from installing the discharge resistors, helping to further save power.
- **Off−mode:** Off−mode helps to achieve low power consumption of an SMPS during no load conditions. The IC goes into Off−mode when the REM pin is brought higher (A/B, lower C/D) than the internal reference voltage $V_{_REM_off}$. The disable input is pulled low, VCC capacitor is discharged and consumption of all internal blocks is reduced once the off−mode is activated. Off mode is terminated when remote pin voltage crosses $V_{_REM_on}$ threshold or application is unplugged from the mains.
- **Current−mode operation with internal slope compensation:** implementing peak current mode control at a fixed 65−kHz frequency, the NCP1249 offers an internal ramp compensation signal that can easily by summed up to the sensed current. Sub harmonic oscillations can thus be compensated via the inclusion of a simple resistor in series with the current−sense information.
- **Frequency excursion:** when the power demand forces the peak current setpoint to reach the internal limit (0.8 V/R_{sense} typically), the frequency is authorized to increase to let the converter deliver more power. The frequency excursion stops when 130 kHz are reached.
- **Internal OPP:** by routing a portion of the negative voltage present during the on−time on the auxiliary winding to the dedicated OPP pin (pin 5), the user has a simple and non−dissipative means to alter the maximum peak current setpoint as the bulk voltage increases. If the pin is grounded, no OPP compensation occurs. If the pin receives a negative voltage down to –250 mV, then a peak current reduction down to 31.3% typical can be achieved. For an improved performance, the maximum voltage excursion on the sense resistor is limited to 0.8 V.
- **EMI jittering:** an internal low−frequency modulation signal varies the pace at which the oscillator frequency is modulated. This helps spreading out energy in conducted noise analysis. To improve the EMI signature at low power levels, the jittering will not be disabled in frequency foldback mode (light load conditions).
- **Frequency foldback capability:** a continuous flow of pulses is not compatible with no−load/light−load standby power requirements. To excel in this domain, the controller observes the feedback pin and when it reaches a level of 1.5 V, the oscillator then starts to reduce its switching frequency as the feedback level continues to decrease. When the feedback pin reaches 1 V, the peak current setpoint is internally frozen and the frequency continues to decrease. It can go down to 26 kHz (typical) reached for a feedback level of 450 mV roughly. At this point, if the power continues to drop to 400 mV, the controller enters classical skip−cycle mode.
- **Internal soft−start:** a soft−start precludes the main power switch from being stressed upon start−up. In this controller, the soft−start is internally fixed to 4 ms. Soft−start is activated when a new startup sequence occurs or during an auto−recovery hiccup.
- **Latch input:** the NCP1249 includes a latch input (pin 5) that can be used to sense an overvoltage condition on the adapter. If this pin is brought higher than the internal reference voltage V_{latch}, then the circuit permanently latches off. The VCC pin is pulled down to a fixed level, keeping the controller latched. The latch reset occurs when the user disconnects the adapter from the mains.

- **V_{CC} OVP:** a latched OVP protects the circuit against V_{cc} runaways. The fault must be present at least 20 μs to be validated. Reset occurs when the user disconnects the adapter from the mains.
- **Short−circuit protection:** short−circuit and especially over−load protections are difficult to implement when a strong leakage inductance between auxiliary and power windings affects the transformer (the aux winding level does not properly collapse in presence of an output short). Here, every time the internal 0.8−V maximum peak current limit is activated (or less when OPP is used), an error flag is asserted and a time period starts, thanks to the programmable timer. The controller can distinguish between two faulty situations:
  - There is an extra demand of power, still within the power supply capabilities. In that case, the feedback level is in the vicinity of 3.2−4 V. It corresponds to 0.8 V as the maximum peak current setpoint without OPP. The timer duration is then 100% of its normal value. If the fault disappears, e.g. the peak current setpoint no longer hits the maximum value (e.g. 0.8 V at no OPP), then the timer is reset.
  - The output is frankly shorted. The feedback level is thus pushed to its upper stop (4.5 V) and the timer is reduced to 25% of its normal value.
  - In either mode, when the fault is validated, all pulses are stopped and the controller enters an auto−recovery burst mode, with a soft−start sequence at the beginning of each cycle. Please note the presence of a divider by two which ignores one hiccup cycle over two (double hiccup type of burst).
  - As soon as the fault disappears, the SMPS resumes operation. Please note that some version offers an auto−recovery mode as we just described, some do not and latch off in case of a short circuit.

Start−up Sequence

The start−up sequence of the NCP1249 involves a high−voltage current source whose input is in pin 10. As this start−up source also performs line sensing for brown−out operation, it is recommended to wire it according to Figure 64 sketch.

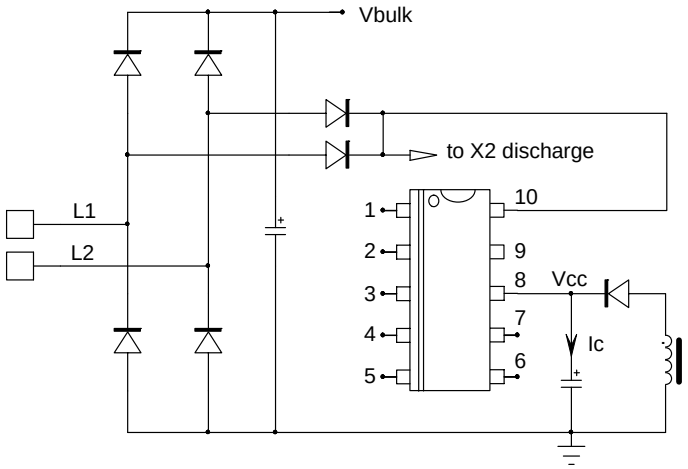

Figure 64. The startup resistor can be connected to the input mains for further power dissipation reduction

In this drawing, the high−voltage pin is not connected to the bulk, but to the full−wave rectified ac input. It is important to keep this configuration as the X2 circuitry will also use it.

The first step starts with the calculation of the needed V_{CC} capacitor which will supply the controller until the auxiliary winding takes over. Experience shows that this time t_1 can be between 5 and 20 ms. Considering that we need at least an energy reservoir for a t_1 time of 10 ms, the V_{CC} capacitor must be larger than:

$$C_{Vcc} \geq \frac{I_{CC4} \times t_1}{V_{CC_ON} - V_{CC_OFF}} \geq \frac{3\ m \times 10\ m}{18 - 10} \geq 3.75\ \mu F \quad \text{(eq. 1)}$$

In this calculation, we adopted the consumption at the highest switching frequency since this is the point at which the IC will work in cold−start case. Let us select a 4.7 μF capacitor at first and experiments in the laboratory will let us know if we were too optimistic for t_1. The V_{CC} capacitor being known, we can now evaluate the charging time to bring the V_{CC} voltage from 0 to the V_{CC_ON} of the IC, 18 V typical. This time sequence can actually be split into two events: 0 V to $V_{CC_inhibit}$ and $V_{CC_inhibit}$ to V_{CC_ON}. This is because the HV source is protected from short−circuits on the VCC pin. In case this happens, the source detects that the V_{CC} voltage is less than $V_{CC_inhibit}$ and only delivers I_{start1} which is below 1 mA: the die power consumption is maintained to the lowest value. In normal operation, when the voltage has normally reached $V_{CC_inhibit}$, the source toggles to the full current and charges the V_{CC} capacitor at a larger current, I_{start2}. The first time duration involves I_{start1} and $V_{CC_inhibit}$.

$$t_{start1} = \frac{V_{CC_inhibit} \times C_{Vcc}}{I_{start1}} = \frac{1 \times 4.7\ \mu}{700\ \mu} \approx 6.7\ ms \quad \text{(eq. 2)}$$

The second duration involves V_{CC_ON} and I_{start2}:

$$t_{start2} = \frac{\left(V_{CC_ON} - V_{CC_inhibit}\right)C_{Vcc}}{I_{start2}} = \frac{(18 - 1) \times 4.7\ \mu}{10\ m} \approx 8\ ms \quad \text{(eq. 3)}$$

The total start−up time is thus around 14−15 ms.

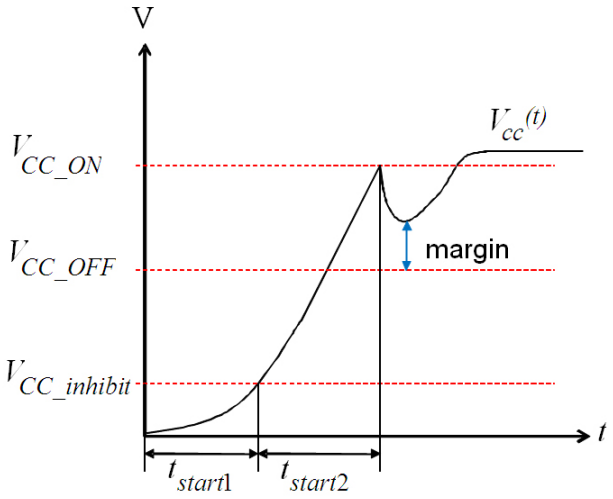

Figure 65. The V_{CC} at start−up is made of two segments given the short−circuit protection implemented on the HV source

In case the V_{CC} capacitor must be increased to cope with no−load standby requirements, there is plenty of margin to keep the total start−up sequence duration below 1 s. Assume the V_{CC} capacitor is 100 μF, then the total start−up time would be below 400 ms.

Brown−out Circuitry

The NCP1249 features, on its HV pin, a true AC line monitoring circuitry – refer to Figure 66. This system includes a minimum start−up threshold and auto−recovery brown−out protection; both of them independent of the input voltage ripple. The thresholds are fixed, but they are designed to fit most of the standard AC−DC converter applications. When the HV pin voltage drops below $V_{_BO_off}$ threshold for more than 50 ms, the brown−out condition is detected and confirmed. Thus the controller stops operation – refer to Figure 67. The V_{CC} capacitor is discharged to $Vcc_{_bias}$ level. The HV current source maintains V_{CC} at $Vcc_{_bias}$ level until the input voltage is back above $V_{_BO_on}$. The controller then fully discharges V_{CC} capacitor first to restart internal logic. Standard startup attempt is then placed by the controller.

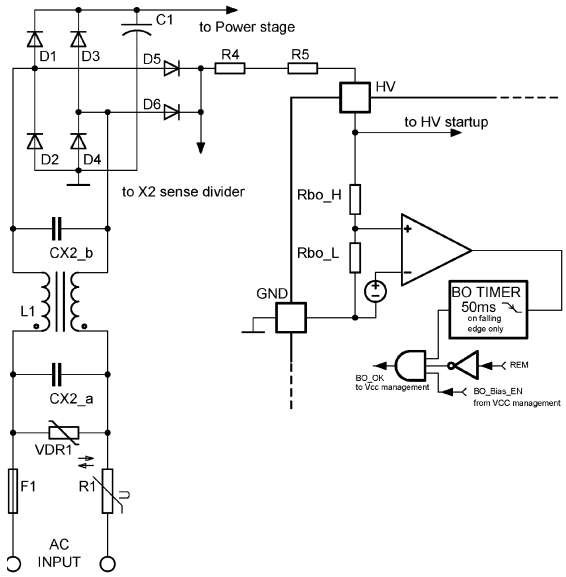

Figure 66. Simplified Block Diagram of Brown−out Detection Circuitry

The Internal HV BO sensing network is formed by high impedance resistor divider with minimum resistance of 20 MΩ. This solution reducing power losses during off−mode and thus helps to pass maximum standby power consumption limit. The internal BO network solution provides excellent noise and PCB leakage currents immunity that is hard to achieve when using external resistor divider built from SMT chip resistors.

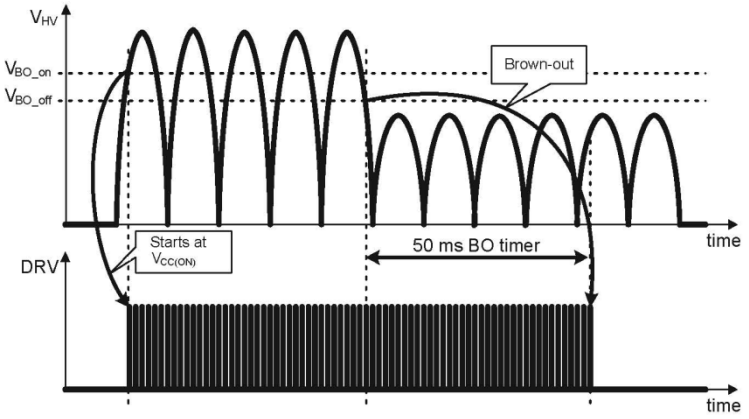

Figure 67. Brown−out Event Detection

X2 and V_{CC} Discharge Circuitry

The NCP1249 X2 discharge circuitry uses dedicated pin (X2) together with external charge pump sensing network to detect whether is application plugged into the mains or not. Advantage of this solution is that the internal IC consumption can be reduced to extremely low level by keeping all internal blocks unbiased except simple and low consuming X2 timer disable circuitry. The internal X2 timer with typical duration of 100 ms is used to overcome unwanted activation of the X2 discharge switch in case of AC line dropout. The internal X2 discharge switch is activated once the X2 timer elapses. The HV startup current source is enabled in the same time thus the discharge path for X2 capacitor exists – refer to Figure 68.

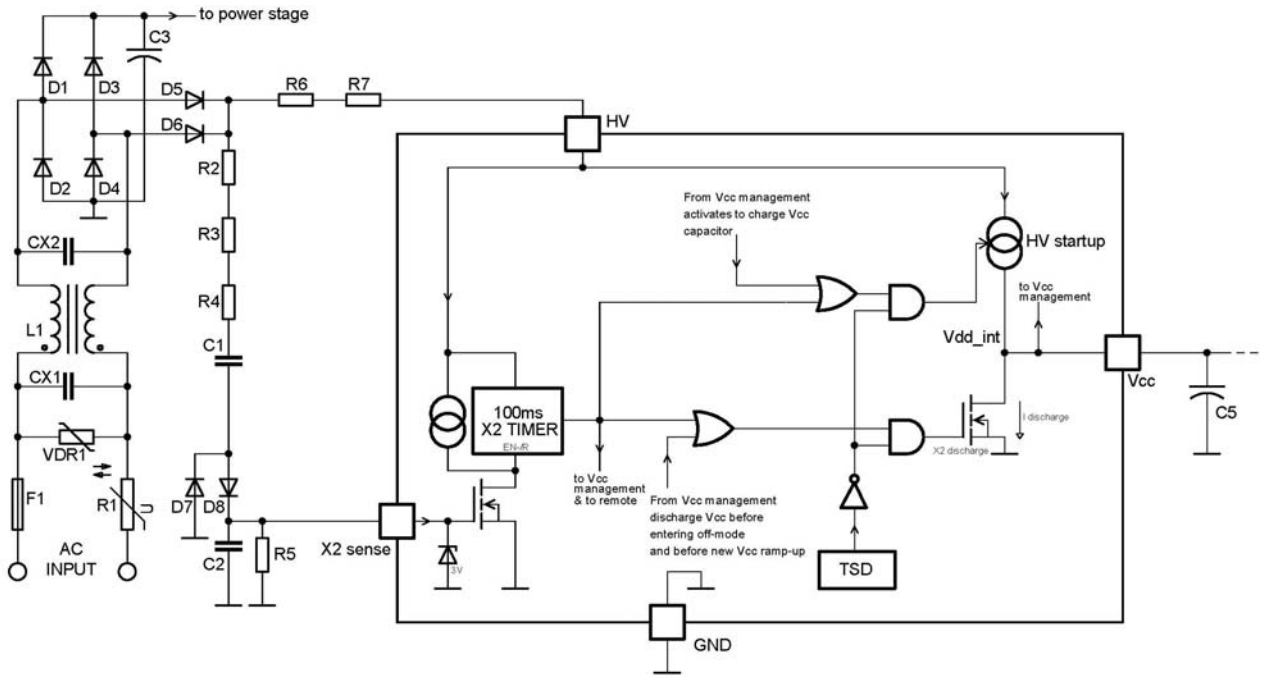

Figure 68. Simplified Block Diagram of X2 and Vcc Capacitor Discharge Circuitry

The time duration of X2 capacitors discharging could be calculated by:

$$t = \frac{U_{C_{X1,2}}}{I_{_X2_dis}} \cdot C_{X1,2} \qquad \text{(eq. 4)}$$

The X2 capacitor discharging process can be interrupted by increasing voltage on X2 pin back above V_{th_X2}.

The over temperature protection block is active during discharging process to protect controller chip against unwanted overheat that could occur in case the X2 pin is opened and the high voltage is present on the HV pin (like during open – short pins testing for instance).

The X2 discharge switch is also activated to discharge V_{CC} capacitor when entering into fault mode (latch mode, auto−recovery mode or the HV pin voltage drops below $V_{_BO_off}$ threshold for more than 50 ms), off−mode and also before controller V_{CC} restart.

Remote Input with Remote Timer − A/B Version

The NCP1249A/B features dedicated input (REM pin) that allows user to activate ultra low consumption mode during which the IC consumption is reduced to only very low HV pin leakage current (refer to $I_{HV_off-mode_1}$ and $I_{HV_off-mode_2}$ parameters). The off−mode is activated when remote pin voltage exceeds $V_{_REM_off}$ threshold (8 V typically). Normal operating mode (i.e. on−mode) is then initiated again when remote input voltage drops back below $V_{_REM_on}$ threshold (1.5 V typically) – refer to Figure 69 for better understanding.

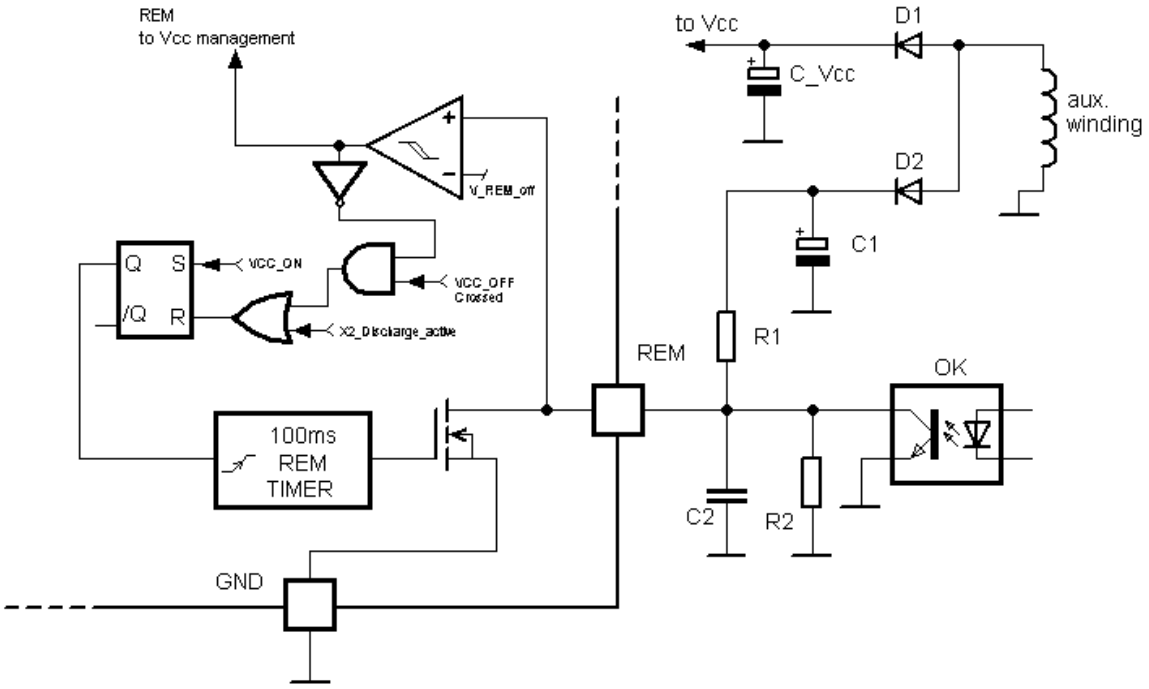

Figure 69. Simplified Block Diagram of Remote Control Input

The off−mode is activated when the remote input is pulled up by auxiliary remote supply (refer to Figure 69.). The normal operation mode is then activated when dedicated opto−coupler pulls the remote input down. There could occur situation, in the application, that the auxiliary remote supply stays charged while the secondary bias has been lost. The application then cannot restart until the auxiliary remote supply capacitor fully discharges. Thus the remote input hosts internal pull down switch and remote timer with duration *REM_timer*. The controller pulls down remote pin using this circuitry in order to allow correct application restart in case the auxiliary bias capacitor (C1) stays charged while the secondary side is fully discharged already. The remote timer is activated each time the application starts after these events:

- Start after application was plugged into the mains (X2 discharger signal resets remote timer latch in this case)
- Start after application has been un−latched by re−plugging to the mains (X2 discharger signal resets remote timer latch in this case)
- Restart from fault conditions in auto−recovery versions
- Restart after V_{CC} has been lost while remote pin was at low state
- Restart after BO event
- Restart after OVP/OTP event

The remote timer helps to assure correct application start or re−start from fault conditions by forcing controller operation for 100 ms typically. However, the secondary controller drives remote pin via opto−coupler during normal operating conditions in order to switch between on−mode and off−mode states. The on−mode is activated for very short time during no−load conditions − just to re−fill primary and secondary capacitors to keep application biased. The remote timer thus cannot be used in this case because it would increase no−load power consumption by forcing application on−mode operation for longer time than it is naturally needed. The remote timer with internal pull down switch is thus not activated in this case (i.e. when application restarts from off−mode operation).

Feedback/Remote Input − C/D Version

The off mode is activated when the remote pin is low and V_{CC_OFF} threshold is crossed i.e. when the skip mode takes so long time that V_{CC} is lost. V_{CC} capacitor is then discharged by internal consumption. Maximum skip mode duration before the NCP1249 enters off-mode is thus given by value of V_{CC} capacitor, total consumption during skip mode and voltage level on V_{CC} capacitor in the time when flyback controller enters skip mode.

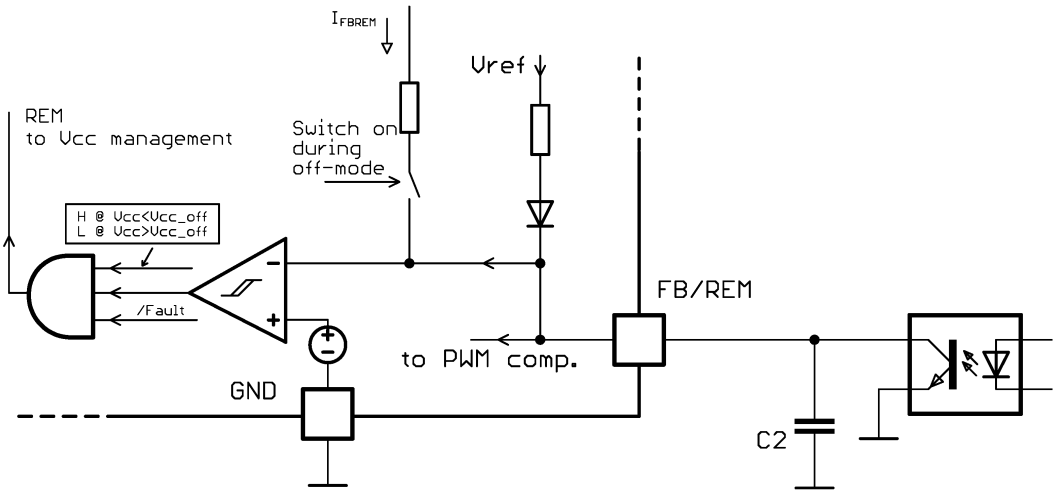

Figure 70. Simplified Block Diagram of FB/REM Control Input

To force the controller entering the off mode, the voltage on the feedback pin has to go below the skip cycle level, 400 mV typically. At this moment, all pulses are blocked and the auxiliary V_{CC} declines down to 0 V at a pace fixed by the V_{CC} capacitor and the controller consumption. When it passes below the V_{CC_OFF} threshold, because the FB pin is still maintained low, the controller does not reactivate the high-voltage start-up source and the circuit remains locked, consuming the least power. The circuit remains off as long as the feedback pin pulled to ground.

When the feedback pin is released, an internal current source (I_{FBREM}), pulls the feedback voltage up, above the inhibition comparator. At this moment, the high-voltage source is good to go and it refuels the V_{CC} capacitor until a new start-up sequence occurs. If the feedback pin is driven by a dedicated off-mode controller, shortly after the new start-up sequence, the feedback pin will go down again, initiating another off cycle. The resulting output voltage exhibits a large low-frequency ripple, naturally decreasing the overall consumption budget of the converter. Typical V_{CC} and feedback signals while in this mode are drawn in Figure 71.

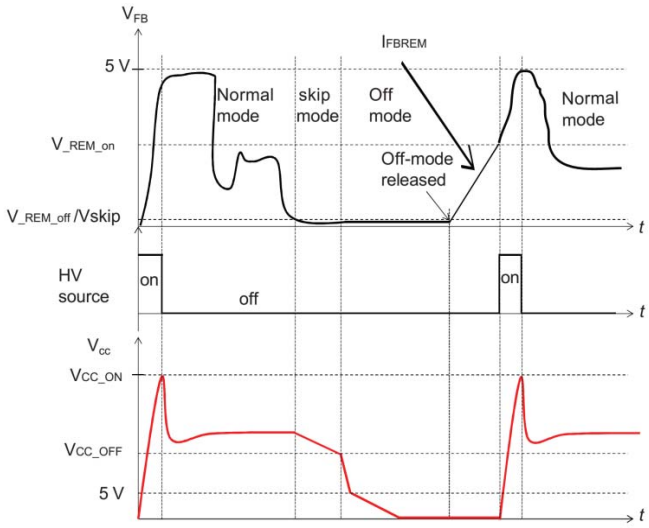

Figure 71. Combined FB/REM Pin Behavior

Operating Status Diagram

The NCP1249A/B V_{CC} management behavior is clearly described in status diagram on Figure 72.

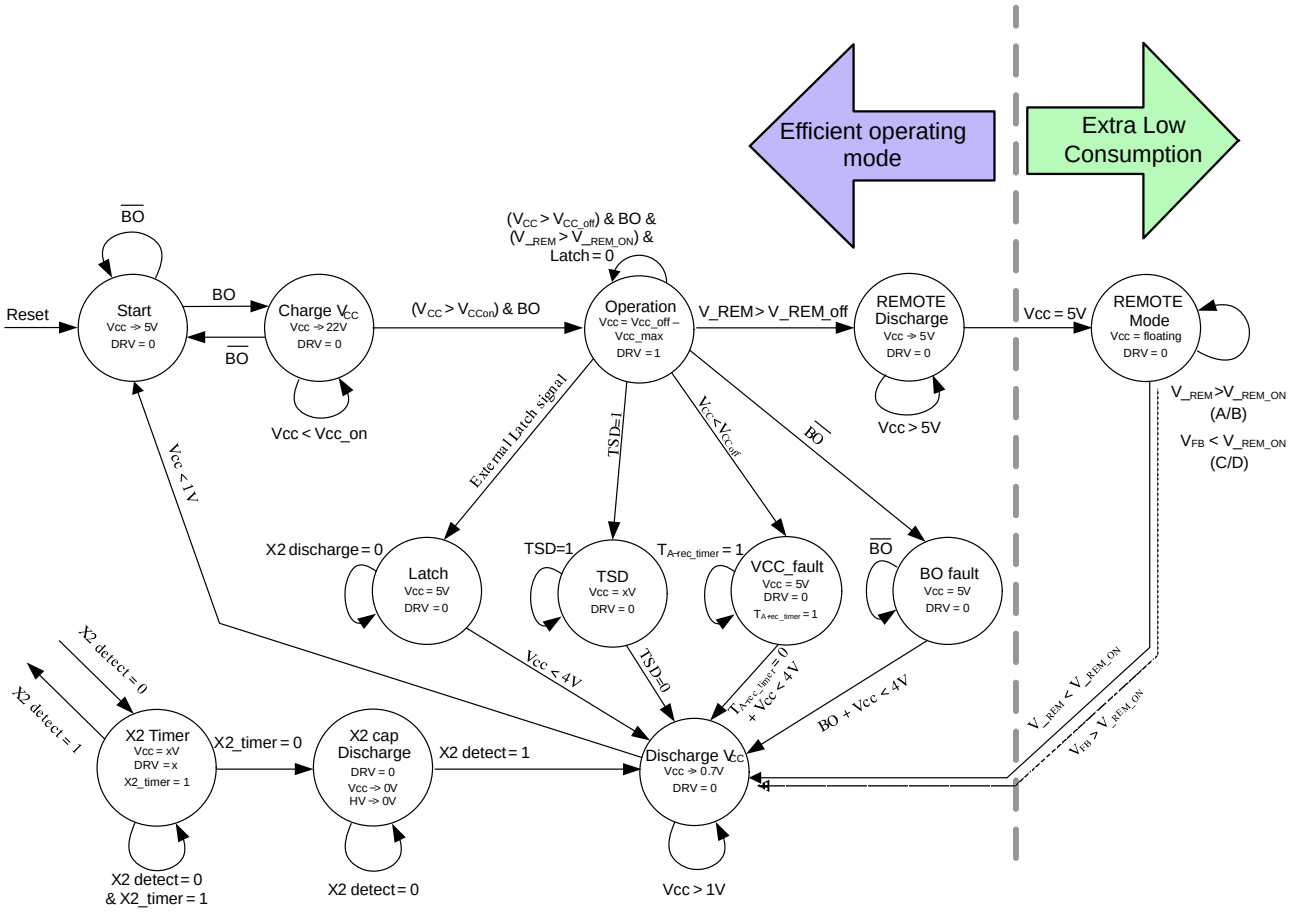

Figure 72. V_{CC} Management Status Diagram

Internal Over Power Protection

There are several known ways to implement Over Power Protection (OPP), all suffering from particular problems. These problems range from the added consumption burden on the converter or the skip−cycle disturbance brought by the current−sense offset. A way to reduce the power capability at high line is to capitalize on the negative voltage swing present on the auxiliary diode anode. During the turn−on time, this point dips to $-NV_{in}$, *N* being the turns ratio between the primary winding and the auxiliary winding. The negative plateau observed on Figure 73 will have amplitude depending on the input voltage. The idea implemented in this chip is to sum a portion of this negative swing with the 0.8 V internal reference level. For instance, if the voltage swings down to −150 mV during the on time, then the internal peak current set point will be fixed to 0.8 − 0.150 = 650 mV. The adopted principle appears in Figure 74 and shows how the final peak current set point is constructed.

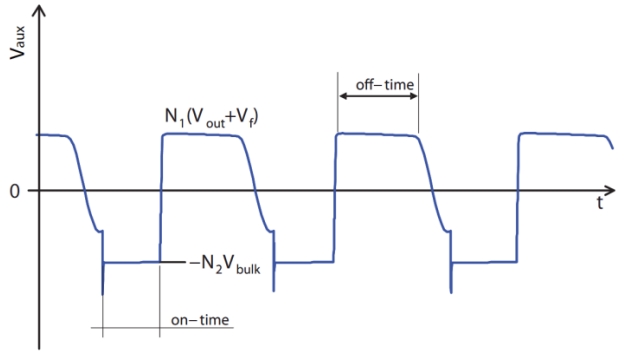

Figure 73. The signal obtained on the auxiliary winding swings negative during the on−time

Let's assume we need to reduce the peak current from 2.5 A at low line, to 2 A at high line. This corresponds to a 20% reduction or a set point voltage of 640 mV. To reach this level, then the negative voltage developed on the OPP pin must reach:

$$V_{OPP} = 640\ m - 800\ m = -160\ mV \quad \text{(eq. 5)}$$

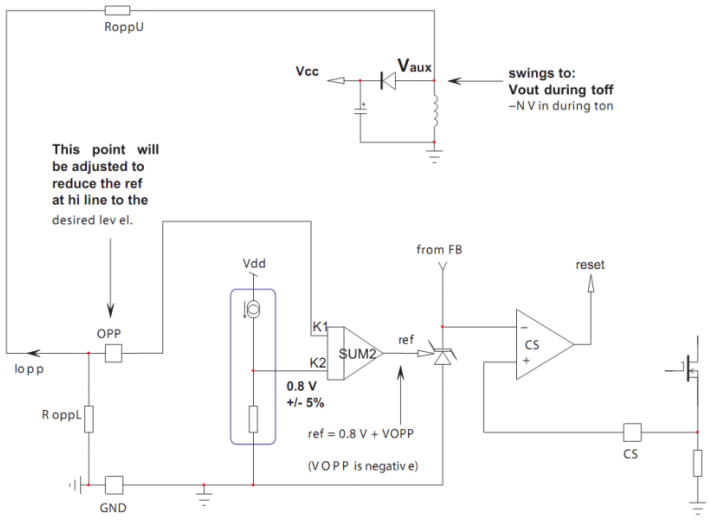

Figure 74. The OPP circuitry affects the maximum peak current set point by summing a negative voltage to the internal voltage reference

Let us assume that we have the following converter characteristics:

V_{out} = 19 V

V_{in} = 85 to 265 V rms

$N_1 = N_p:N_s$ = 1:0.25

$N_2 = N_p:N_{aux}$ = 1:0.18

Given the turns ratio between the primary and the auxiliary windings, the on−time voltage at high line (265 Vac) on the auxiliary winding swings down to:

$$V_{aux} = -N_2 V_{in,max} = -0.18 \times 375 = -67.5\ V \quad \text{(eq. 6)}$$

To obtain a level as imposed by (Eq. 5), we need to install a divider featuring the following ratio:

$$\text{Div} = \frac{0.16}{67.5} \approx 2.4\ m \quad \text{(eq. 7)}$$

If we arbitrarily fix the pull−down resistor R_{OPPL} to 1 kΩ, then the upper resistor can be obtained by:

$$R_{OPPU} = \frac{67.5 - 0.16}{0.16/1\ k} \approx 421\ k\Omega \quad \text{(eq. 8)}$$

If we now plot the peak current set point obtained by implementing the recommended resistor values, we obtain the following curve (Figure 75):

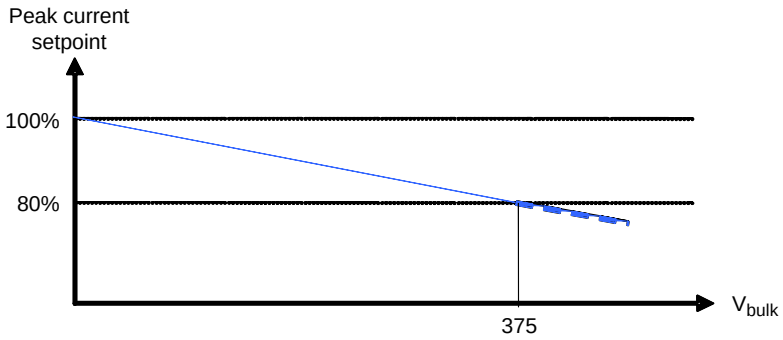

Figure 75. The peak current regularly reduces down to 20% at 375 V dc

The OPP pin is surrounded by Zener diodes stacked to protect the pin against ESD pulses. These diodes accept some peak current in the avalanche mode and are designed to sustain a certain amount of energy. On the other side, negative injection into these diodes (or forward bias) can cause substrate injection which can lead to an erratic circuit behavior. To avoid this problem, the pin is internal clamped slightly below –300 mV which means that if more current is injected before reaching the ESD forward drop, then the maximum peak reduction is kept to 40%. If the voltage finally forward biases the internal zener diode, then care must be taken to avoid injecting a current beyond –2 mA. Given the value of R_{OPPU}, there is no risk in the present example. Finally, please note that another comparator internally fixes the maximum peak current set point to 0.8 V even if the OPP pin is adversely biased above 0 V.

For optimum performance over temperature, we recommend keeping the low−side OPP resistor below 3 kΩ.

Frequency Foldback

The reduction of no−load standby power associated with the need for improving the efficiency, requires a change in the traditional fixed−frequency type of operation. This controller implements a switching frequency foldback when the feedback voltage passes below a certain level, V_{fold_FB}, set around 1.9 V. At this point, the oscillator turns into a Voltage−Controlled Oscillator and reduces its switching frequency. The peak current setpoint is following the feedback pin until its level reaches 1 V. Below this value, the peak current freezes to V_{freeze_FB} (250 mV or ≈31% of the maximum 0.8 V setpoint) and the only way to further reduce the transmitted power is to diminish the operating frequency down to 26 kHz. This value is reached at a voltage feedback level of 450 mV typically. Below this point, if the output power continues to decrease, the part enters skip cycle for the best noise−free performance in no−load conditions. Figure 76 depicts the adopted scheme for the part.

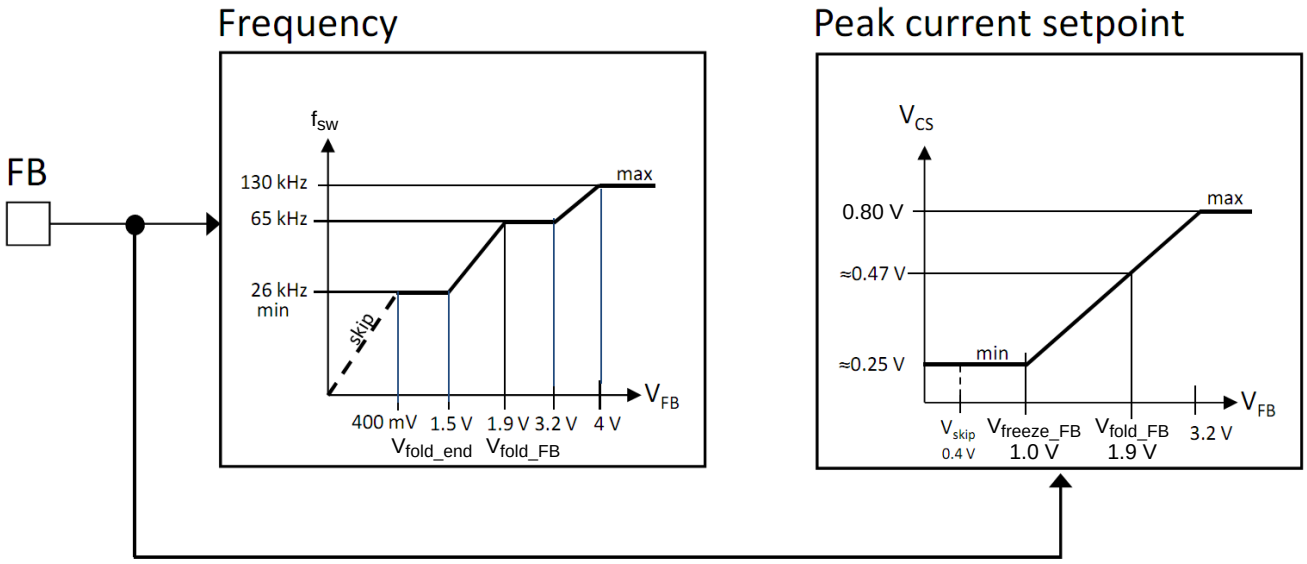

Figure 76. By observing the voltage on the feedback pin, the controller reduces its switching frequency for an improved performance at light load

Auto−recovery Short−circuit Protection

In case of output short−circuit or if the power supply experiences a severe overloading situation, an internal error flag is raised and starts a countdown timer. If the flag is asserted longer than fault timer duration, the driving pulses are stopped and the V_{CC} capacitor is discharged down to 10 V (V_{CC_OFF} threshold) by controller Icc consumption. At this point, the controller activates 2 s auto−recovery timer that starts to count down the time to new restart attempt. The total restart time from fault confirmation is thus given by sum of two times: VCC capacitor discharge time from given Vcc level (present at fault confirmation event) to V_{CC_OFF} level and 2 s internal auto−recovery timer duration. The V_{CC} capacitor is discharged to $Vcc_{_bias}$ level when auto−recovery timer starts counting. The V_{CC} is maintained at $Vcc_{_bias}$ level during this operation to keep timer and other internal circuitry running.

The V_{CC} capacitor is fully discharged by X2 discharge switch before controller tries for restart from fault condition. The restart from fault condition is caused when auto−recovery timer elapses or V_{CC} is forced below 4 V externally. The HV startup current source is activated to charge the Vcc capacitor in fast manner to V_{CC_ON} level and thus to restart converter operation in case the input line voltage is above $V_{_BO_on}$ threshold. The controller is then checking for the absence of the fault. If the fault is still there, the supply enters another cycle of so−called hiccup. If the fault has disappeared, the power supply resumes operations. Please note that the soft−start is activated during each of the re−start sequence.

Slope Compensation

The NCP1249 includes an internal ramp compensation signal. This is the buffered oscillator clock delivered during the on time only. Its amplitude is around 2.5 V at the maximum authorized duty−ratio. Ramp compensation is a known means used to cure sub harmonic oscillations in CCM−operated current−mode converters. These oscillations take place at half the switching frequency and occur only during Continuous Conduction Mode (CCM) with a duty−ratio greater than 50%. To lower the current loop gain, one usually mixes between 50 and 100% of the inductor downslope with the current−sense signal. Figure 77 depicts how internally the ramp is generated. Please note that the ramp signal will be disconnected from the CS pin, during the off−time.

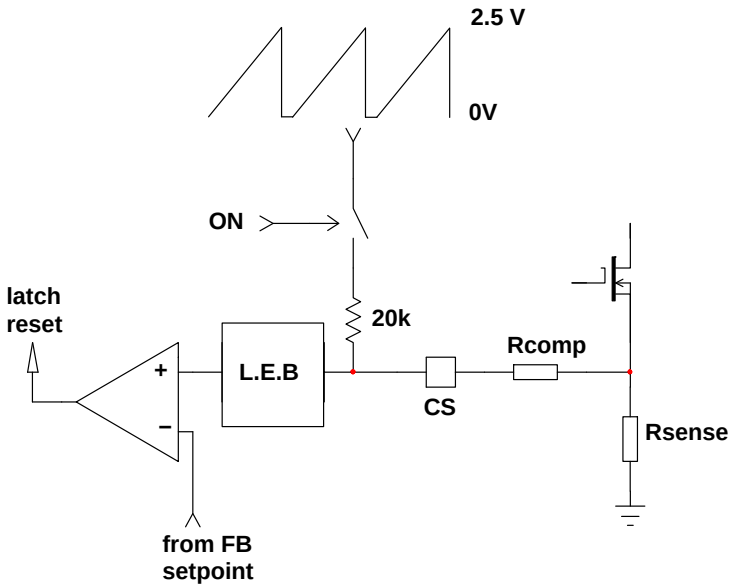

Figure 77. Inserting a resistor in series with the current sense information brings slope compensation and stabilizes the converter in CCM operation

In the NCP1249 controller, the oscillator ramp exhibits a 2.5 V swing reached at a 80% duty−ratio. If the clock operates at a 65−kHz frequency, then the available oscillator slope corresponds to:

$$S_{ramp} = \frac{V_{ramp}}{D_{max} \times T_{sw}} = \frac{2.5}{0.8 \times 15\,\mu} = 208\text{kV/s or } 208\text{mV/}\mu\text{s} \quad \text{(eq. 9)}$$

In our flyback design, let's assume that our primary inductance L_p is 770 μH, and the SMPS delivers 19 V with a N_p:N_s turns ratio of 1:0.25. The off−time primary current slope S_p is thus given by:

$$S_p = \frac{\left(V_{out} + V_f\right)\frac{N_p}{N_s}}{L_p} = \frac{(19 + 0.8) \times 4}{770\,\mu} = 103\text{ kA/s} \quad \text{(eq. 10)}$$

Given a sense resistor of 330 mΩ, the above current ramp turns into a voltage ramp of the following amplitude:

$$S_{sense} = S_p R_{sense} = 103\text{ k} \times 0.33 = 34\text{ kV/s or } 34\text{ mV/}\mu\text{s} \quad \text{(eq. 11)}$$

If we select 50% of the downslope as the required amount of ramp compensation, then we shall inject a ramp whose slope is 17 mV/μs. Our internal compensation being of 208 mV/μs, the divider ratio (*divratio*) between R_{comp} and the internal 20 kΩ resistor is:

$$\text{divratio} = \frac{17\text{ m}}{208\text{ m}} = 0.082 \quad \text{(eq. 12)}$$

The series compensation resistor value is thus:

$$R_{comp} = R_{ramp}\,\text{divratio} = 20\text{ k} \times 0.082 \approx 1.64\text{ k}\Omega \quad \text{(eq. 13)}$$

A resistor of the above value will then be inserted from the sense resistor to the current sense pin. We recommend adding a small 100 pF capacitor, from the current sense pin to the controller ground for improved noise immunity. Please make sure both components are located very close to the controller.

Latching Off the Controller

The OPP pin not only allows a reduction of the peak current set point in relationship to the line voltage, it also offers a means to permanently latch−off the part. When the part is latched−off, the VCC pin is internally pulled down to V_{CC_bias} and the part stays in this state until the user un−plugs the converter from the mains outlet or V_{CC} is forced below 4 V externally. The latch detection is made by observing the OPP pin by a comparator featuring a 3 V reference voltage. However, for noise reasons and in particular to avoid the leakage inductance contribution at turn off, a 1 μs blanking delay is introduced before the output of the OVP comparator is checked. Then, the OVP comparator output is validated only if its high−state duration lasts a minimum of 600 ns. Below this value, the event is ignored. Then, a counter ensures that only four successive OVP events have occurred before actually latching the part. There are several possible implementations, depending on the needed precision and the parameters you want to control.

The first and easiest solution is the additional resistive divider on top of the OPP one. This solution is simple and inexpensive but requires the insertion of a diode to prevent disturbing the OPP divider during the on−time.

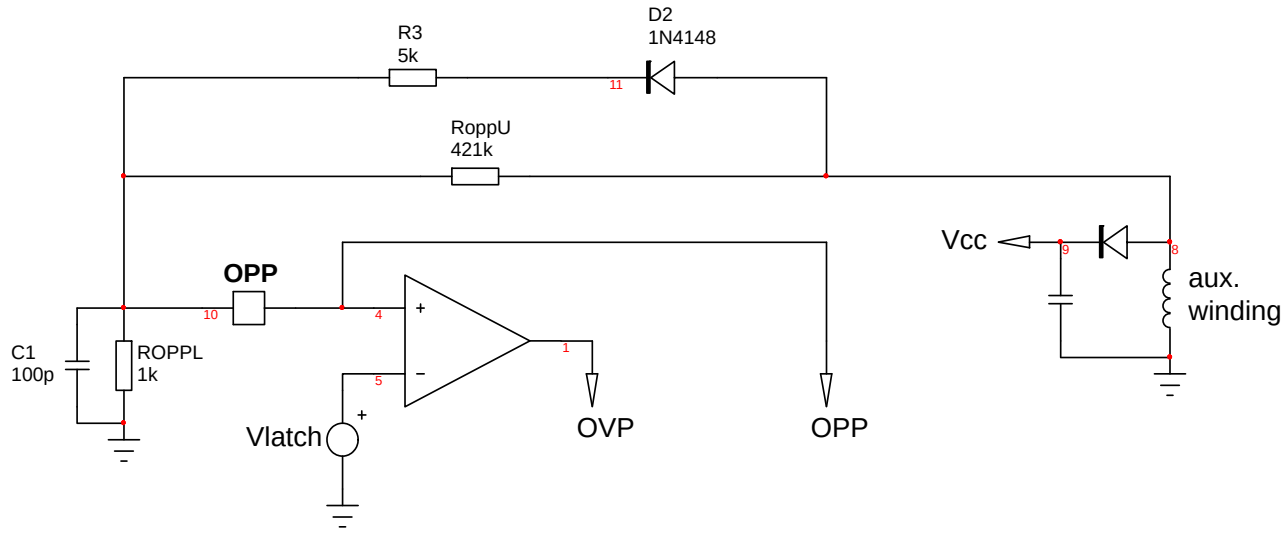

Figure 78. Simple resistive divider brings the OPP pin above 3 V in case of a V_{cc} voltage runaway above 18 V

First, calculate the OPP network with the above equations. Then, suppose we want to latch off our controller when V_{out} exceeds 25 V. On the auxiliary winding, the plateau reflects the output voltage by the turns ratio between the power and the auxiliary windings. In case of voltage runaway for our 19 V adapter, the plateau will go up to:

$$V_{aux,OVP} = 25 \times \frac{0.18}{0.25} = 18\ V \qquad \text{(eq. 14)}$$

Since our OVP comparator trips at a 3 V level, across the 1 kΩ selected OPP pull−down resistor, it implies a 3 mA current. From 3 V to go up to 18 V, we need an additional 15 V. Under 3 mA and neglecting the series diode forward drop, it requires a series resistor of:

$$R_{OVP} = \frac{V_{latch} - V_{VOP}}{V_{OVP}/R_{OPPL}} = \frac{18 - 3}{3/1\ k} = \frac{15}{3\ m} = 5\ k\Omega \qquad \text{(eq. 15)}$$

In nominal conditions, the plateau establishes to around 14 V. Given the divide−by ratio 6, the OPP pin will swing to 14/6 = 2.3 V during normal conditions, leaving 700 mV for the noise immunity. A 100 pF capacitor can be added to improve it and avoids erratic trips in presence of external surges. Do not increase this capacitor too much otherwise the OPP signal will be affected by the integrating time constant.

A second solution for the OVP detection alone, is to use a Zener diode wired as recommended by Figure 79.

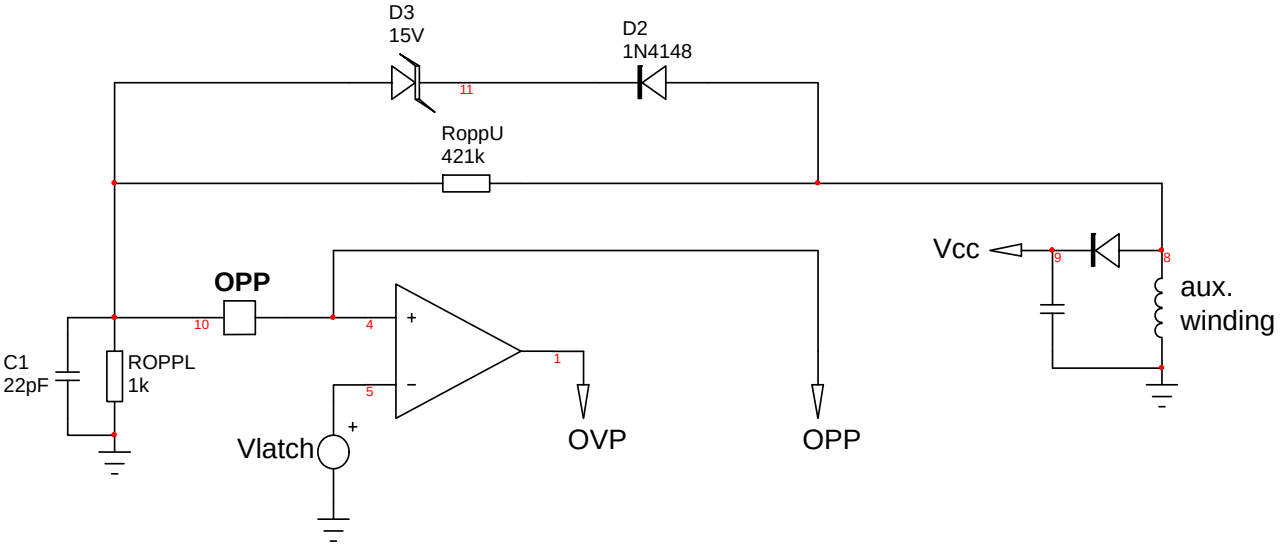

Figure 79. Zener Diode in Series with a Diode Helps to Improve the Noise Immunity of the System

In this case, to still trip at a 18 V level, we have selected a 15 V Zener diode. In nominal conditions, the voltage on the OPP pin is almost 0 V during the off time as the Zener is fully blocked. This technique clearly improves the noise immunity of the system compared to that obtained from a resistive string as in Figure 78. Please note the reduction of the capacitor on the OPP pin to 10−22 pF. This is because of the potential spike going through the Zener parasitic capacitor and the possible auxiliary level shortly exceeding its breakdown voltage during the leakage inductance reset period (hence the internal 1 μs blanking delay at turn off). This spike despite its very short time is energetic enough to charge the added capacitor C_1 and given the time constant, could make it discharge slower, potentially disturbing the blanking circuit. When implementing the Zener option, it is important to carefully observe the OPP pin voltage (short probe connections!) and check that enough margin exists to that respect.

Internal and External Over Temperature Protection

The NCP1249 includes a temperature shutdown protection. When the temperature rises above the high threshold during stable operation − i.e. start−up sequence is ended and V_{CC} is between V_{CC_ON} and V_{CC_OFF} levels, the controller immediately stops driver pulses. After the temperature falls back below the lower threshold, the V_{CC} capacitor is fully discharged by X2 discharge switch to restart the controller.

The TSD protection can be activated at some other cases (charging V_{CC} capacitor − start−up sequence and discharging X2 or V_{CC} capacitors). The TSD protection only interrupts current operating sequence – i.e. the operation sequence continue after the temperature falls back below the lower threshold. The controller is not reset by TSD activation in these cases.

In a lot of designs, the adapter must be protected against thermal runaways, e.g. when the temperature inside the adapter box increases beyond a certain value. Figure 80 shows how to implement a simple OTP using an external NTC and a series diode. The principle remains the same: make sure the OPP network is not bothered by the additional NTC hence the presence of this diode. When the NTC resistor will diminish as the temperature increases, the voltage on the OPP pin during the off time will slowly increase and, once it crosses 3 V for 4 consecutive clock cycles, the controller will permanently latch off.

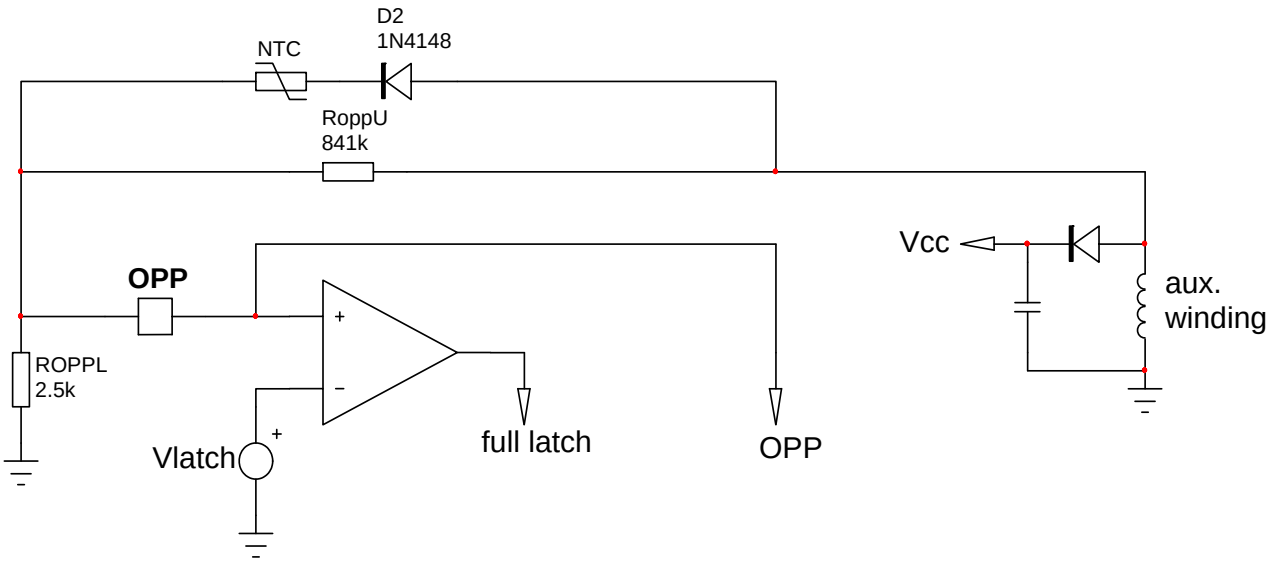

Figure 80. The internal circuitry hooked to pin 1 can be used to implement over temperature protection (OTP)

Back to our 19 V adapter, we have found that the plateau voltage on the auxiliary diode was 13 V in nominal conditions. We have selected an NTC which offers a 470 kΩ resistor at 25°C and drops to 8.8 kΩ at 110°C. If our auxiliary winding plateau is 14 V and we consider a 0.6 V forward drop for the diode, then the voltage across the NTC in fault mode must be:

$$V_{NTC} = 14 - 3 - 0.6 = 10.4\ V \qquad \text{(eq. 16)}$$

Based on the 8.8 kΩ NTC resistor at 110°C, the current inside the device must be:

$$I_{NTC} = \frac{10.4}{8.8\ k} \approx 1.2\ mA \qquad \text{(eq. 17)}$$

As such, the bottom resistor R_{OPPL}, can easily be calculated:

$$R_{OPPL} = \frac{3}{1.2\ m} = 2.5\ k\Omega \qquad \text{(eq. 18)}$$

Now that the pull−down OPP resistor is known, we can calculate the upper resistor value R_{OPPU} to adjust the power limit at the chosen output power level. Suppose we need a 200 mV decrease from the 0.8 V set point and the on−time swing on the auxiliary anode is −67.5 V, then we need to drop over R_{OPPU} a voltage of:

$$V_{R_{OPPU}} = 67.5 - 0.2 = 67.3\ V \qquad \text{(eq. 19)}$$

The current circulating in the pull down resistor R_{OPPL} in this condition will be:

$$I_{R_{OPPL}} = \frac{200\ m}{2.5\ k} = 80\ \mu A \qquad \text{(eq. 20)}$$

The R_{OPPU} value is therefore easily derived:

$$R_{OPPU} = \frac{67.3}{80\ \mu} = 841\ k\Omega \qquad \text{(eq. 21)}$$

Combining OVP and OTP

The OTP and Zener−based OVP can be combined together as illustrated by Figure 81.

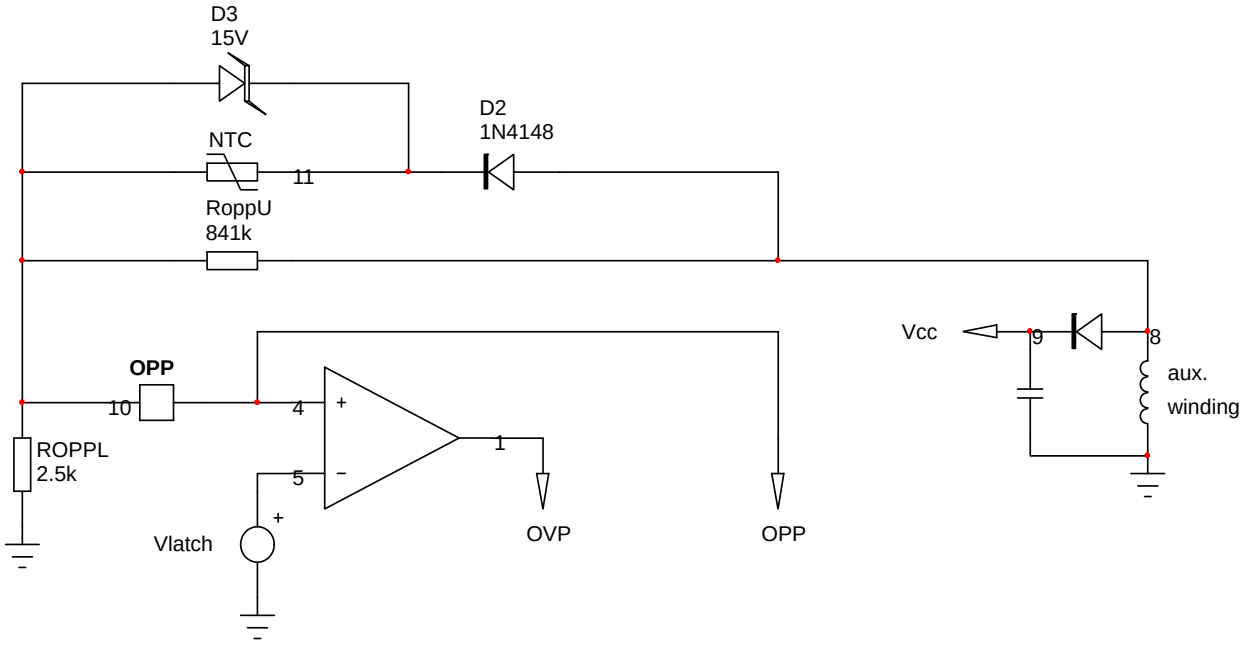

Figure 81. With the NTC back in place, the circuit nicely combines OVP, OTP and OPP on the same pin

In nominal V_{CC}/output conditions, when the Zener is not activated, the NTC can drive the OPP pin and trigger the adapter in case of a fault. On the contrary, in nominal temperature conditions, if the loop is broken, the voltage runaway will be detected and acknowledged by the controller.

In case the OPP pin is not used for either OPP or OVP, it can simply be grounded.

Filtering the Spikes

The auxiliary winding is the seat of spikes that can couple to the OPP pin via the parasitic capacitances exhibited by the Zener diode and the series diode. To prevent an adverse triggering of the Over Voltage Protection circuitry, it is possible to install a small *RC* filter before the detection network. Typical values are those given in Figure 82 and must be selected to provide the adequate filtering function without degrading the stand−by power by an excessive current circulation.

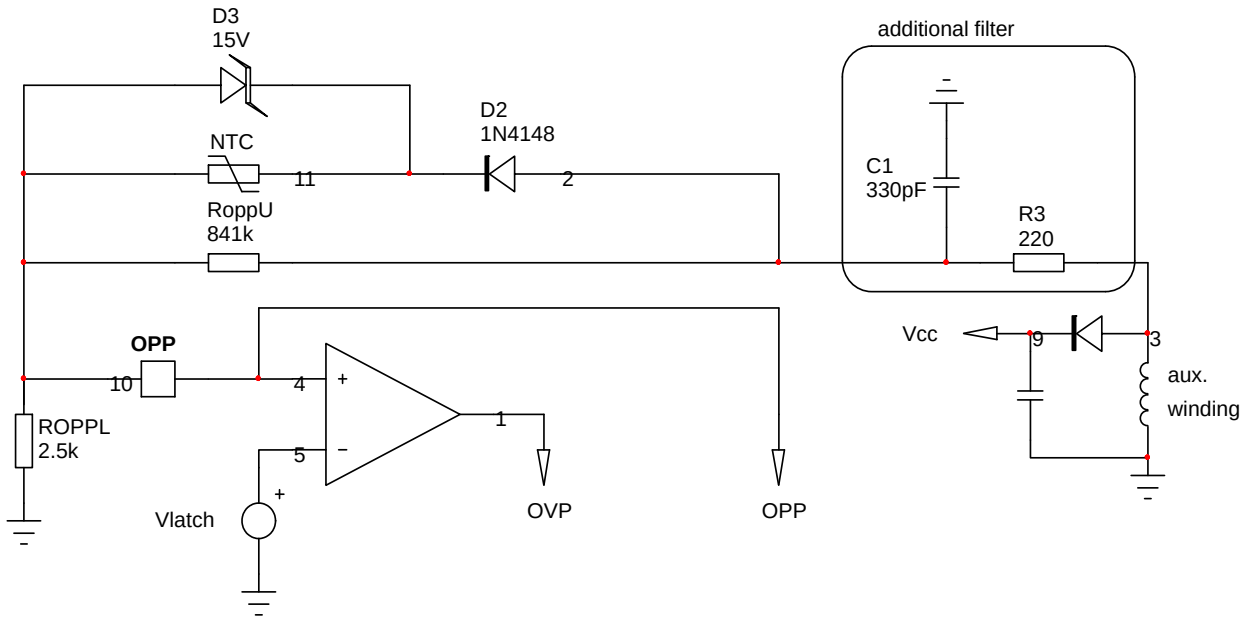

Figure 82. A small *RC* filter avoids the fast rising spikes from reaching the protection pin of the NCP1249 in presence of energetic perturbations superimposed on the input line

Latching Off with the VCC pin

The NCP1249 hosts a dedicated comparator on the VCC pin. When the voltage on this pin exceeds 27.5 V typically for more than 20 μs, a signal is sent to the internal latch and the controller immediately stops the driving pulses while remaining in a lockout state. The part can be reset when the user disconnects the adapter from the mains. This technique offers a simple and cheaper means to protect the converter against optocoupler failures without using the OPP pin and a Zener diode.

Peak Power Excursions

There are applications where the load profile heavily changes from a nominal to a peak value. For instance, it is possible that a 30 W ac−dc adapter accepts power excursions up to 60 W in certain conditions. Inkjet printers typically fall in that category of peak power adapters. However, to avoid growing the transformer size, an existing technique consists in freezing the peak current to a maximum value ($0.8/R_{sense}$ in our case) but authorizes frequency increase to a certain point. This point is internally fixed at 130 kHz.

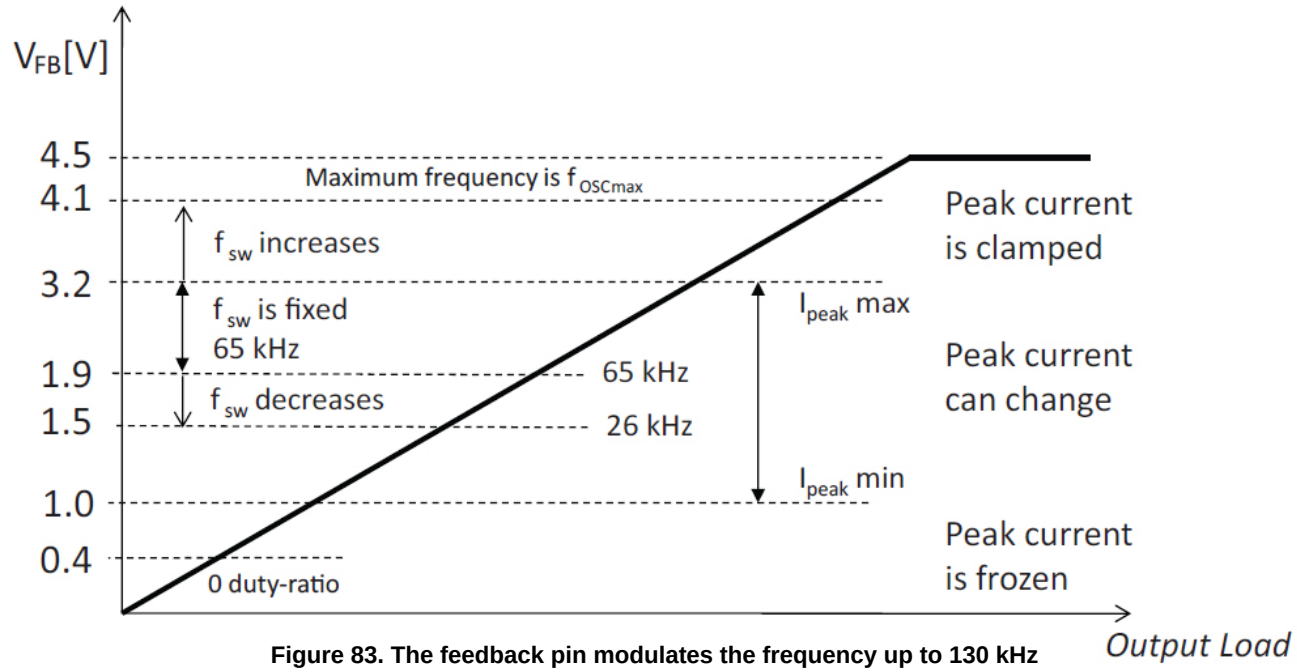

Figure 83. The feedback pin modulates the frequency up to 130 kHz (short−circuit, maximum power) or down to 26 kHz in frequency foldback

Figure 83 shows the voltage evolution from almost 0 V to the open−loop level, around 4.5 V. At low power levels or in no−load operation, the feedback voltage stays in the vicinity of 400 mV and ensures skip−cycle operation. In this mode, the peak current is frozen to 31% of its maximum value and the operating frequency is 26 kHz. This freeze lasts as long as V_{FB} stays below 1 V. Beyond 1 V, the peak current is authorized to follow V_{FB} through a ratio of 4. When the power demand goes further up, the feedback pin crosses a level of 1.5 V where the switching frequency linearly increases from 26 kHz up to 65 kHz, a value reached when the feedback voltage exceeds 1.9 V. Beyond 1.9 V, the frequency no longer changes. As V_{FB} still increases, the controller is in a fixed−frequency variable peak current mode control type of operation until the feedback voltage hits 3.2 V. At this point, the maximum current is limited to 0.8 V/R_{sense}. If V_{FB} further increases, it means the converter undergoes an overload and requires more power from the source. As the peak current excursion is stopped, the only way to deliver more power is to increase the switching frequency. From 3.2 V up to 4.1 V, the frequency linearly increases from 65 kHz to 130 kHz. Beyond 4.1 V, the frequency is fixed to 130 kHz. The maximum power delivered by the converter depends whether it operates in Discontinuous Conduction Mode (DCM) or in Continuous Conduction Mode (CCM):

$$P_{max,DCM} = \frac{1}{2} L_p f_{OSC_max} I_{peak,max}^2 \eta \quad \text{(eq. 22)}$$

$$P_{max,CCM} = \frac{1}{2} L_p f_{OSC_max} \left(I_{peak,max}^2 - I_{valley}^2 \right) \eta \quad \text{(eq. 23)}$$

Where $I_{peak,max}$ is the maximum peak current authorized by the controller and I_{valley} the valley current reached just before a new switching cycle begins. This current is expressed by the following formula:

$$I_{valley} = I_{peak} - \frac{V_{out} + V_f}{NL_p} t_{off} \quad \text{(eq. 24)}$$

In DCM, the valley current is equal to 0.

Two Levels of Protection

Once the feedback voltage asks for the maximum peak current, the controller knows that an overload condition has started. An internal timer is operated as soon as the maximum peak is reached. If the feedback voltage continues its rise, it means that the converter output voltage is going down further, close to a short−circuit situation. When the feedback voltage reaches the open−loop level (above 4.1 V typically), the original timer duration is divided by 4. Of course, if the feedback does not stay that long in the region of concern, the timer is reset when returning to a normal level. Figure 84 shows the timer values versus the feedback voltage.

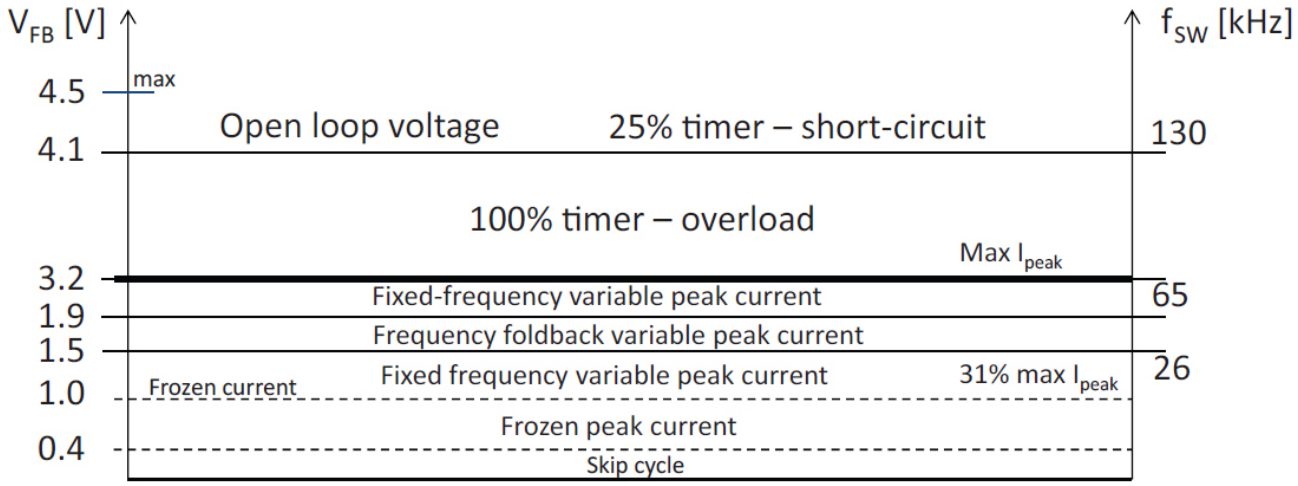

Figure 84. Depending on the feedback level, the timer will take two different values: it will authorize a transient overload, but will reduce a short−circuit duration

Please note that the overload situation (OVL) is detected when the maximum peak current limit is hit. It can be 3.2 V as indicated in the graph in case of no Over Power Protection (OPP). If you have programmed an OPP level of −200 mV for instance, the OVL threshold becomes (0.8 − 0.2) x 4 = 2.4 V. When the maximum peak current situation is lifted, the converter returns to a normal situation, the timer is reset. The short circuit situation is detected by sensing a feedback voltage beyond 4.1 V. For the sake of the explanation, we have gathered two different events in Figure 85 (V_{Ct} is voltage on internal capacitor which defines fault timer duration).

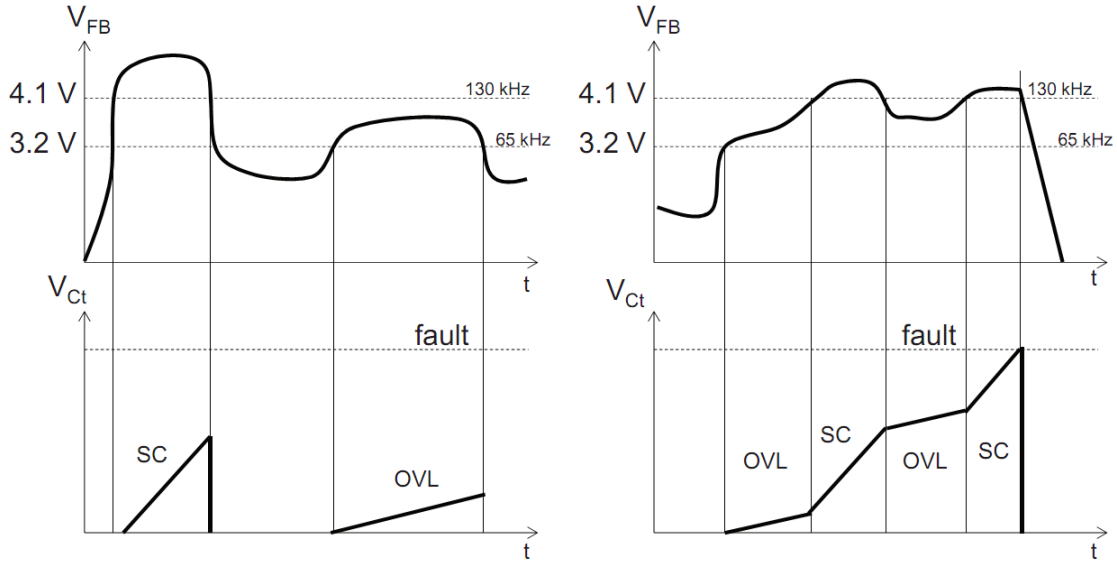

Figure 85.

When the feedback voltage exits a fault region before time completion, the timer is reset. On the contrary, if the timer elapses, the part enters an auto−recovery hiccup or latches off depending on the operated version.

In the first case, the feedback is pushed to the maximum upon start−up. The timer starts with a charging slope of the short−circuit condition (SC). As soon as regulation occurs, the timer gets reset. An overload occurs shortly after (OVL). The internal timer immediately starts to count when the 3.2 V level is crossed (V_{FB} with no OPP). As the overload lasts less than the fault timer elapses, the feedback returns to its regulation level and resets the timer.

In the second case, the overload occurs after regulation but the feedback voltage quickly jumps into the short−circuit area. At this point, the countdown is accelerated as the charging slope changed to a steeper one. The load goes back to an OVL mode and the counter slows down. Finally, back to short circuit again and the timer trips the fault circuitry after completion: all pulses are immediately stopped.

The OVL timer is adjusted by wiring a resistor (R_{Timer}) from pin 5 to ground. The below chart shows what value to adopt to fit your timer duration needs. Typically, a 22 kΩ pull-down resistor will set the OVL duration to 500 ms. In case of the pin short-circuit to ground (safety test), the duration will be reduced to 500/4 or 125 ms.

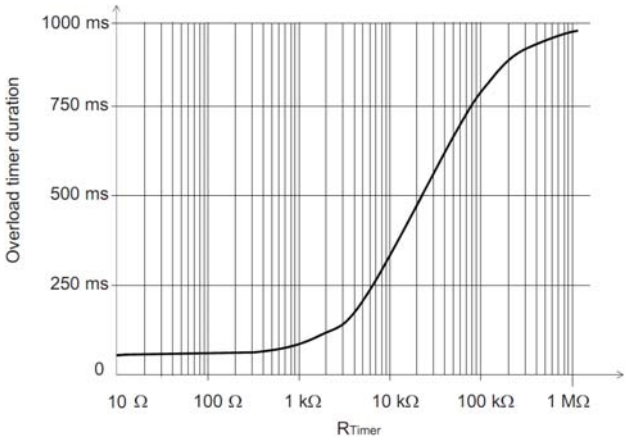

Figure 86. This Curve Shows How to Program the OVL Timer Duration

Please note that pin 5 includes a circuitry that manages the timer current in case of pin opening or shortening to ground. In both cases, the timer is set to known value as listed in the parameters sheet. The given duration is that of the OVL timer.

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CASE 751BP
ISSUE A

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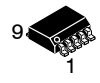
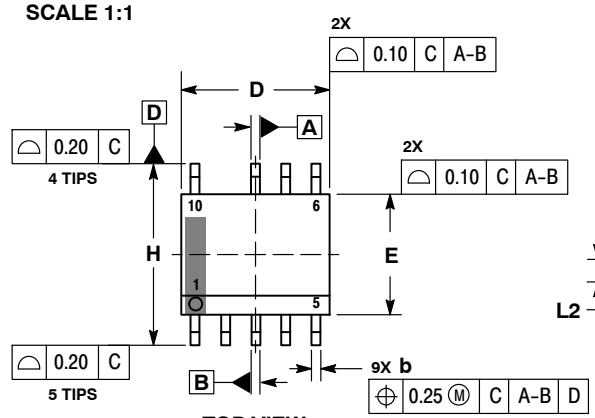
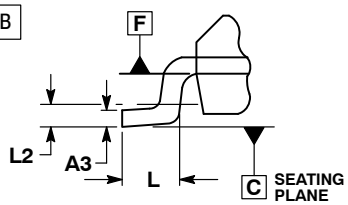


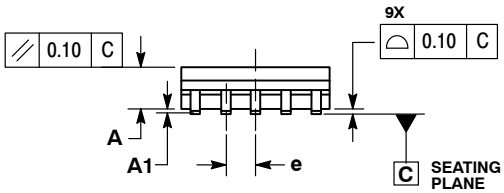
SCALE 1:1



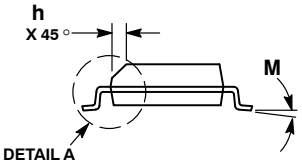
TOP VIEW



DETAIL A



SIDE VIEW

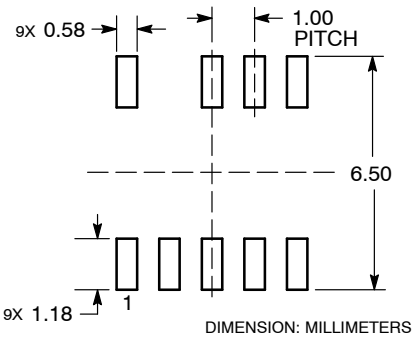


END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF 'b' AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	1.25	1.75
A1	0.10	0.25
A3	0.17	0.25
b	0.31	0.51
D	4.80	5.00
E	3.80	4.00
e	1.00 BSC	
H	5.80	6.20
h	0.37 REF	
L	0.40	1.27
L2	0.25 BSC	
M	0°	8°

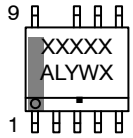
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G", may or not be present.

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