NCP1203

PWM Controller, Fixed Frequency, Flyback, Current Mode

Housed in SOIC–8 or PDIP–8 package, the NCP1203 represents a major leap toward ultra-compact Switchmode Power Supplies and represents an excellent candidate to replace the UC384X devices. Due to its proprietary SMARTMOS™ Very High Voltage Technology, the circuit allows the implementation of complete off-line AC–DC adapters, battery charger and a high-power SMPS with few external components.

With an internal structure operating at a fixed 40 kHz, 60 kHz or 100 kHz switching frequency, the controller features a high-voltage startup FET which ensures a clean and loss-less startup sequence. Its current-mode control naturally provides good audio-susceptibility and inherent pulse-by-pulse control.

When the current setpoint falls below a given value, e.g. the output power demand diminishes, the IC automatically enters the so-called skip cycle mode and provides improved efficiency at light loads while offering excellent performance in standby conditions. Because this occurs at a user adjustable low peak current, no acoustic noise takes place.

The NCP1203 also includes an efficient protective circuitry which, in presence of an output over load condition, disables the output pulses while the device enters a safe burst mode, trying to restart. Once the default has gone, the device auto-recoveres. Finally, a temperature shutdown with hysteresis helps building safe and robust power supplies.

Features
• High-Voltage Startup Current Source
• Auto-Recovery Internal Output Short-Circuit Protection
• Extremely Low No-Load Standby Power
• Current-Mode with Adjustable Skip-Cycle Capability
• Internal Leading Edge Blanking
• 250 mA Peak Current Capability
• Internally Fixed Frequency at 40 kHz, 60 kHz and 100 kHz
• Direct Optocoupler Connection
• Undervoltage Lockout at 7.8 V Typical
• SPICE Models Available for TRANSient and AC Analysis
• Pin to Pin Compatible with NCP1200
• These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications
• AC–DC Adapters for Notebooks, etc.
• Offline Battery Chargers
• Auxiliary Power Supplies (USB, Appliances, TVs, etc.)
**PIN FUNCTION DESCRIPTION**

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Name</th>
<th>Function</th>
<th>Pin Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Adj</td>
<td>Adjust the skipping peak current</td>
<td>This pin lets you adjust the level at which the cycle skipping process takes place. Shorting this pin to ground, permanently disables the skip cycle feature.</td>
</tr>
<tr>
<td>2</td>
<td>FB</td>
<td>Sets the peak current setpoint</td>
<td>By connecting an optocoupler to this pin, the peak current setpoint is adjusted accordingly to the output power demand. Skip cycle occurs when FB falls below Vpin1.</td>
</tr>
<tr>
<td>3</td>
<td>CS</td>
<td>Current sense input</td>
<td>This pin senses the primary current and routes it to the internal comparator via an L.E.B.</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>The IC ground</td>
<td>–</td>
</tr>
<tr>
<td>5</td>
<td>Drv</td>
<td>Driving pulses</td>
<td>The driver’s output to an external MOSFET.</td>
</tr>
<tr>
<td>6</td>
<td>VCC</td>
<td>Supplies the IC</td>
<td>This pin is connected to an external bulk capacitor of typically 22 µF.</td>
</tr>
<tr>
<td>7</td>
<td>NC</td>
<td>–</td>
<td>This unconnected pin ensures adequate creepage distance.</td>
</tr>
<tr>
<td>8</td>
<td>HV</td>
<td>Ensure a clean and lossless startup sequence</td>
<td>Connected to the high-voltage rail, this pin injects a constant current into the VCC capacitor during the startup sequence.</td>
</tr>
</tbody>
</table>

*Please refer to the application information section
Figure 2. Internal Circuit Architecture

MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Voltage</td>
<td>V_CC, Drv</td>
<td>16</td>
<td>V</td>
</tr>
<tr>
<td>Power Supply Voltage on all other pins except Pin 5 (Drv), Pin 6 (V_CC) and Pin 8 (HV)</td>
<td>-</td>
<td>-0.3 to 10</td>
<td>V</td>
</tr>
<tr>
<td>Maximum Current into all pins except Pin 6 (V_CC) and Pin 8 (HV) when 10 V ESD diodes are activated</td>
<td>-</td>
<td>5.0</td>
<td>mA</td>
</tr>
<tr>
<td>Thermal Resistance, Junction—to—Air, PDIP—8 Version</td>
<td>R_JA</td>
<td>100</td>
<td>°C/W</td>
</tr>
<tr>
<td>Thermal Resistance, Junction—to—Air, SOIC Version</td>
<td>R_JA</td>
<td>178</td>
<td>°C/W</td>
</tr>
<tr>
<td>Thermal Resistance, Junction—to—Case</td>
<td>R_JC</td>
<td>57</td>
<td>°C/W</td>
</tr>
<tr>
<td>Maximum Junction Temperature</td>
<td>T_JMAX</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Temperature Shutdown</td>
<td>T_J</td>
<td>-170</td>
<td>°C</td>
</tr>
<tr>
<td>Hysteresis in Shutdown</td>
<td>-</td>
<td>30</td>
<td>°C</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>T_J</td>
<td>-40 to +125</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>T_stg</td>
<td>-60 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>ESD Capability, Human Body Model, All pins except Pin 6 (V_CC) and Pin 8 (HV)</td>
<td>-</td>
<td>2.0</td>
<td>kV</td>
</tr>
<tr>
<td>ESD Capability, Machine Model</td>
<td>-</td>
<td>200</td>
<td>V</td>
</tr>
<tr>
<td>Maximum Voltage on Pin 8 (HV) with Pin 6 (V_CC) Decoupled to Ground with 10 μF</td>
<td>-</td>
<td>500</td>
<td>V</td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection rated using the following tests:
   Human Body Model (HBM) 2000 V per JEDEC Standard JESD22, Method A114E.
   Machine Model (MM) 200 V per JEDEC Standard JESD22, Method A115A.
### ELECTRICAL CHARACTERISTICS

(For typical values $T_J = 25^\circ C$, for min/max values $T_J = 0^\circ C$ to $+125^\circ C$, Max $T_J = 150^\circ C$, $V_{CC} = 11\, V$ unless otherwise noted.)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Pin</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Turn−on Threshold Level, $V_{CC}$ Going Up</strong></td>
<td>$V_{CC(on)}$</td>
<td>6</td>
<td>12.2</td>
<td>12.8</td>
<td>14</td>
<td>V</td>
</tr>
<tr>
<td><strong>Minimum Operating Voltage after Turn−on</strong></td>
<td>$V_{CC(min)}$</td>
<td>6</td>
<td>7.2</td>
<td>7.8</td>
<td>8.4</td>
<td>V</td>
</tr>
<tr>
<td><strong>$V_{CC}$ Decreasing Level at which the Latchoff Phase Ends</strong></td>
<td>$V_{CC latch}$</td>
<td>6</td>
<td>–</td>
<td>4.9</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td><strong>Internal IC Consumption, No Output Load on Pin 5</strong></td>
<td>$I_{CC1}$</td>
<td>6</td>
<td>–</td>
<td>1.2</td>
<td>1.4</td>
<td>μA</td>
</tr>
<tr>
<td><strong>Internal IC Consumption, 1.0 nF Output Load on Pin 5, $F_{SW} = 40$ kHz</strong></td>
<td>$I_{CC2}$</td>
<td>6</td>
<td>–</td>
<td>1.4</td>
<td>1.6</td>
<td>mA</td>
</tr>
<tr>
<td><strong>Internal IC Consumption, 1.0 nF Output Load on Pin 5, $F_{SW} = 60$ kHz</strong></td>
<td>$I_{CC2}$</td>
<td>6</td>
<td>–</td>
<td>2.0</td>
<td>2.2</td>
<td>mA</td>
</tr>
<tr>
<td><strong>Internal IC Consumption, Latch−off Phase, $V_{CC} = 6.0$ V</strong></td>
<td>$I_{CC3}$</td>
<td>6</td>
<td>–</td>
<td>250</td>
<td>–</td>
<td>μA</td>
</tr>
<tr>
<td><strong>Internal Startup Current Source (Pin 8 biased at 50 V)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>High−Voltage Current Source, $V_{CC} = 10$ V</strong></td>
<td>$I_{C1}$</td>
<td>8</td>
<td>3.5</td>
<td>6.0</td>
<td>9.0</td>
<td>mA</td>
</tr>
<tr>
<td><strong>High−Voltage Current Source, $V_{CC} = 0$</strong></td>
<td>$I_{C2}$</td>
<td>8</td>
<td>–</td>
<td>11</td>
<td>–</td>
<td>mA</td>
</tr>
<tr>
<td><strong>Drive Output</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Output Voltage Rise−Time @ CL = 1.0 nF, 10−90% of Output Signal</strong></td>
<td>$T_r$</td>
<td>5</td>
<td>–</td>
<td>67</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td><strong>Output Voltage Fall−Time @ CL = 1.0 nF, 10−90% of Output Signal</strong></td>
<td>$T_f$</td>
<td>5</td>
<td>–</td>
<td>28</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td><strong>Source Resistance</strong></td>
<td>$R_{OH}$</td>
<td>5</td>
<td>27</td>
<td>40</td>
<td>61</td>
<td>Ω</td>
</tr>
<tr>
<td><strong>Sink Resistance</strong></td>
<td>$R_{OL}$</td>
<td>5</td>
<td>5.0</td>
<td>10</td>
<td>20</td>
<td>Ω</td>
</tr>
<tr>
<td><strong>Current Comparator (Pin 5 loaded unless otherwise noted)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Input Bias Current @ 1.0 V Input Level on Pin 3</strong></td>
<td>$I_{IB}$</td>
<td>3</td>
<td>–</td>
<td>0.02</td>
<td>–</td>
<td>μA</td>
</tr>
<tr>
<td><strong>Maximum Internal Current Setpoint (Note 3)</strong></td>
<td>$I_{Limit}$</td>
<td>3</td>
<td>–</td>
<td>0.85</td>
<td>0.92</td>
<td>1.0</td>
</tr>
<tr>
<td><strong>Default Internal Current Setpoint for Skip Cycle Operation</strong></td>
<td>$I_{Skip}$</td>
<td>3</td>
<td>–</td>
<td>360</td>
<td>–</td>
<td>mV</td>
</tr>
<tr>
<td><strong>Propagation Delay from Current Detection to Gate OFF State</strong></td>
<td>$T_{DEL}$</td>
<td>3</td>
<td>–</td>
<td>90</td>
<td>160</td>
<td>ns</td>
</tr>
<tr>
<td><strong>Leading Edge Blanking Duration (Note 3)</strong></td>
<td>$T_{LEB}$</td>
<td>3</td>
<td>–</td>
<td>230</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td><strong>Internal Oscillator ($V_{CC} = 11$ V, Pin 5 loaded by 1 nF)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Oscillation Frequency, 40 kHz Version</strong></td>
<td>$f_{OSC}$</td>
<td>–</td>
<td>37</td>
<td>42</td>
<td>47</td>
<td>kHz</td>
</tr>
<tr>
<td><strong>Oscillation Frequency, 60 kHz Version</strong></td>
<td>$f_{OSC}$</td>
<td>–</td>
<td>57</td>
<td>65</td>
<td>73</td>
<td>kHz</td>
</tr>
<tr>
<td><strong>Oscillation Frequency, 100 kHz Version</strong></td>
<td>$f_{OSC}$</td>
<td>–</td>
<td>90</td>
<td>103</td>
<td>115</td>
<td>kHz</td>
</tr>
<tr>
<td><strong>Maximum Duty−Cycle</strong></td>
<td>$D_{max}$</td>
<td>–</td>
<td>74</td>
<td>80</td>
<td>87</td>
<td>%</td>
</tr>
<tr>
<td><strong>Feedback Section ($V_{CC} = 11$ V, Pin 5 unloaded)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Internal Pullup Resistor</strong></td>
<td>$R_{up}$</td>
<td>2</td>
<td>–</td>
<td>20</td>
<td>–</td>
<td>kΩ</td>
</tr>
<tr>
<td><strong>Pin 3 to Current Setpoint Division Ratio</strong></td>
<td>$I_{ratio}$</td>
<td>–</td>
<td>–</td>
<td>3.3</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td><strong>Skip Cycle Generation</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Default Skip Mode Level</strong></td>
<td>$V_{skip}$</td>
<td>1</td>
<td>1.0</td>
<td>1.2</td>
<td>1.4</td>
<td>V</td>
</tr>
<tr>
<td><strong>Pin 1 Internal Output Impedance</strong></td>
<td>$Z_{out}$</td>
<td>1</td>
<td>–</td>
<td>22</td>
<td>–</td>
<td>kΩ</td>
</tr>
</tbody>
</table>

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Max value at $T_J = 0^\circ C$.
2. Maximum value @ $T_J = 25^\circ C$, please see characterization curves.
3. Pin 5 loaded by 1 nF.
Figure 3. $V_{CC(on)}$ Threshold versus Temperature

Figure 4. $V_{CC(min)}$ Level versus Temperature

Figure 5. $I_C$ Current Consumption (No Load) versus Temperature

Figure 6. $I_{CC}$ Consumption (Loaded by 1 nF) versus Temperature

Figure 7. HV Current Source at $V_{CC} = 10$ V versus Temperature

Figure 8. $I_C$ Consumption at $V_{CC} = 6$ V versus Temperature
Figure 9. Drive Source Resistance versus Temperature

Figure 10. Drive Sink Resistance versus Temperature

Figure 11. Maximum Current Setpoint versus Temperature

Figure 12. Frequency versus Temperature
Introduction

The NCP1203 implements a standard current mode architecture where the switch–off time is dictated by the peak current setpoint. This component represents the ideal candidate where low part–count is the key parameter, particularly in low–cost AC–DC adapters, auxiliary supplies etc. Due to its high–performance SMARTMOS High–Voltage technology, the NCP1203 incorporates all the necessary components normally needed in UC384X based supplies: timing components, feedback devices, low–pass filter and startup device. This later point emphasizes the fact that ON Semiconductor’s NCP1203 does not need an external startup resistance but supplies the startup current directly from the high–voltage rail. On the other hand, more and more applications are requiring low no–load standby power, e.g. for AC–DC adapters, VCRs etc. UC384X series have a lot of difficulty to reduce the switching losses at low power levels. NCP1203 elegantly solves this problem by skipping unwanted switching cycles at a user–adjustable power level. By ensuring that skip cycles take place at low peak current, the device ensures quiet, noise free operation. Finally, an auto–recovery output short–circuit protection (OCP) prevents from any lethal thermal runaway in overload conditions.

Startup Sequence

When the power supply is first powered from the mains outlet, the internal current source (typically 6.0 mA) is biased and charges up the VCC capacitor. When the voltage on this VCC capacitor reaches the VCC(on) level (typically 12.8 V), the current source turns off and no longer wastes any power. At this time, the VCC capacitor only supplies the controller and the auxiliary supply is supposed to take over before VCC collapses below VCC(min). Figure 13 shows the internal arrangement of this structure:

![Figure 13. The Current Source Brings VCC Above 12.8 V and then Turns Off](image)

Once the power supply has started, the VCC shall be constrained below 16 V, which is the maximum rating on pin 6. Figure 14 portrays a typical startup sequence with a VCC regulated at 12.5 V:

![Figure 14. A Typical Startup Sequence for the NCP1203](image)
Current–Mode Operation
As the UC384X series, the NCP1203 features a well-known current mode control architecture which provides superior input audio–susceptibility compared to traditional voltage–mode controllers. Primary current pulse–by–pulse checking together with a fast over current comparator offers greater security in the event of a difficult fault condition, e.g. a saturating transformer.

Adjustable Skip Cycle Level
By offering the ability to tailor the level at which the skip cycle takes place, the designer can make sure that the skip operation only occurs at low peak current. This point guarantees a noise–free operation with cheap transformers. Skip cycle offers a proven mean to reduce the standby power in no or light loads situations.

Wide Switching–Frequency Offer
Four different options are available: 40 kHz – 65 kHz – 100 kHz. Depending on the application, the designer can pick up the right device to help reducing magnetics or improve the EMI signature before reaching the 150 kHz starting point.

Overcurrent Protection (OCP)
When the auxiliary winding collapses below UVLOlow, the controller stops switching and reduces its consumption. It stays in this mode until Vcc reaches 4.9 V typical, where the startup source is reactivated and a new startup sequence is attempted. The power supply is thus operated in burst mode and avoids any lethal thermal runaway. When the default goes way, the power supply automatically resumes operation.

Wide Duty–Cycle Operation
Wide mains operation requires a large duty–cycle excursion. The NCP1203 can go up to 80% typically.

Low Standby Power
If SMPS naturally exhibit a good efficiency at nominal load, they begin to be less efficient when the output power demand diminishes. By skipping un–needed switching cycles, the NCP1203 drastically reduces the power wasted during light load conditions. In no–load conditions, the NCP1203 allows the total standby power to easily reach next International Energy Agency (IEA) recommendations.

No Acoustic Noise while Operating
Instead of skipping cycles at high peak currents, the NCP1203 waits until the peak current demand falls below a user–adjustable 1/3rd of the maximum limit. As a result, cycle skipping can take place without having a singing transformer … You can thus select cheap magnetic components free of noise problems.

External MOSFET Connection
By leaving the external MOSFET external to the IC, you can select avalanche proof devices which, in certain cases (e.g. low output powers), let you work without an active clamping network. Also, by controlling the MOSFET gate signal flow, you have an option to slow down the device commutation, therefore reducing the amount of ElectroMagnetic Interference (EMI).

SPICE Model
A dedicated model to run transient cycle–by–cycle simulations is available but also an averaged version to help you closing the loop. Ready–to–use templates can be downloaded in OrCAD’s Pspice and INTUSOFT’s from ON Semiconductor web site, NCP1203 related section.

Overload Operation
In applications where the output current is purposely not controlled (e.g. wall adapters delivering raw DC level), it is interesting to implement a true short–circuit protection. A short–circuit actually forces the output voltage to be at a low level, preventing a bias current to circulate in the optocoupler LED. As a result, the auxiliary voltage also decreases because it also operates in Flyback and thus duplicates the output voltage, providing the leakage inductance between windings is kept low. To account for this situation and properly protect the power supply, NCP1203 hosts a dedicated overload detection circuitry. Once activated, this circuitry imposes to deliver pulses in a burst manner with a low duty–cycle. The system auto–recovers when the fault condition disappears.

During the startup phase, the peak current is pushed to the maximum until the output voltage reaches its target and the feedback loop takes over. The auxiliary voltage takes place after a few switching cycles and self–supplies the IC. In presence of a short circuit on the output, the auxiliary voltage will go down until it crosses the undervoltage lockout level of typically 7.8 V. When this happens, NCP1203 immediately stops the switching pulses and unbiases all unnecessary logical blocks. The overall consumption drops, while keeping the gate grounded, and the Vcc slowly falls down. As soon as Vcc reaches typically 4.8 V, the startup source turns–on again and a new startup sequence occurs, bringing Vcc toward 12.8 V as an attempt to restart. If the default has gone, then the power supply normally restarts. If not, a new protective burst is initiated, shielding the SMPS from any runaway. Figure 15, on the following page, portrays the typical operating signals in short circuit.
Calculating the $V_{CC}$ Capacitor
The $V_{CC}$ capacitor can be calculated knowing the IC consumption as soon as $V_{CC}$ reaches 12.8 V. Suppose that a NCP1203P60 is used and drives a MOSFET with a 30 nC total gate charge ($Q_g$). The total average current is thus made of $I_{CC1}$ (700 μA) plus the driver current, $F_{sw} \times Q_g$ or 1.8 mA. The total current is therefore 2.5 mA. The $\Delta V$ available to fully startup the circuit (e.g. never reach the 7.8 V UVLO during power on) is 12.8–7.8 = 5 V. We have a capacitor who then needs to supply the NCP1203 with 2.5 mA during a given time until the auxiliary supply takes over. Suppose that this time was measured at around 15 ms. $C_{V_{CC}}$ is calculated using the equation $C = \frac{\Delta t \cdot i}{\Delta V}$ or $C \geq 7.5 \mu F$. Select a 22 μF/16 V and this will fit.

Skipping Cycle Mode
The NCP1203 automatically skips switching cycles when the output power demand drops below a given level. This is accomplished by monitoring the FB pin. In normal operation, pin 2 imposes a peak current accordingly to the load value. If the load demand decreases, the internal loop asks for less peak current. When this setpoint reaches a determined level (Vpin 1), the IC prevents the current from decreasing further down and starts to blank the output pulses: the IC enters the so-called skip cycle mode, also named controlled burst operation. The power transfer now depends upon the width of the pulse bunches (Figure 17). Suppose we have the following component values:

- $L_p$, primary inductance = 350 μH
- $F_{sw}$, switching frequency = 61 kHz
- $I_p \text{skip} = 600$ mA (or 333 mV/Rsense)

The theoretical power transfer is therefore:

$$\frac{1}{2} \cdot L_p \cdot I_p^2 \cdot F_{sw} = 3.8 \text{ W}$$

If this IC enters skip cycle mode with a bunch length of 10 ms over a recurrent period of 100 ms, then the total power transfer is: $3.8 \cdot 0.1 = 380$ mW.

To better understand how this skip cycle mode takes place, a look at the operation mode versus the FB level immediately gives the necessary insight:

When FB is above the skip cycle threshold (1.0 V by default), the peak current cannot exceed 1.0 V/Rsense. When the IC enters the skip cycle mode, the peak current cannot go below Vpin1/3.3/Rsense. The user still has the flexibility to alter this 1.0 V by either shunting pin 1 to ground through a resistor or raising it through a resistor up to the desired level. Grounding pin 1 permanently invalidates the skip cycle operation. However, given the extremely low standby power the controller can reach, the PWM in no-load conditions can quickly enter the minimum $t_{on}$ and still transfer too much power. An instability can take place. We recommend in that case to leave a little bit of skip level to always allow 0% duty cycle.
Figure 17. Output Pulses at Various Power Levels (X = 5.0 \mu s/div) \( P_1 < P_2 < P_3 \)

Figure 18. The Skip Cycle Takes Place at Low Peak Currents which Guaranties Noise–Free Operation

We recommend a pin 1 operation between 400 mV and 1.3 V that will fix the skip peak current level between 120 mV/Rsense and 390 mV/Rsense.

**Non–Latching Shutdown**

In some cases, it might be desirable to shut off the part temporarily and authorize its restart once the default has disappeared. This option can easily be accomplished through a single NPN bipolar transistor wired between FB and ground. By pulling FB below the Adj pin 1 level, the output pulses are disabled as long as FB is pulled below pin 1. As soon as FB is relaxed, the IC resumes its operation. Figure 19 depicts the application example.
Figure 19. Another Way of Shutting Down the IC without a Definitive Latch–Off State

Full Latching Shutdown

Other applications require a full latching shutdown, e.g. when an abnormal situation is detected (overtemperature or overvoltage). This feature can easily be implemented through two external transistors wired as a discrete SCR.

When the VCC level exceeds the zener breakdown voltage, the NPN biases the PNP and fires the equivalent SCR, permanently bringing down the FB pin. The switching pulses are disabled until the user unplugs the power supply.

Figure 20. Two Bipolars Ensure a Total Latch–Off of the SMPS in Presence of an OVP

Rhold ensures that the SCR stays on when fired. The bias current flowing through Rhold should be small enough to let the VCC ramp up (12.8 V) and down (4.9 V) when the SCR is fired. The NPN base can also receive a signal from a temperature sensor. Typical bipolars can be MMBT2222 and MMBT2907 for the discrete latch. The MMBT3946 features two bipolars NPN+PNP in the same package and could also be used.

Protecting the Controller Against Negative Spikes

As with any controller built upon a CMOS technology, it is the designer’s duty to avoid the presence of negative spikes on sensitive pins. Negative signals have the bad habit to forward bias the controller substrate and induce erratic behaviors. Sometimes, the injection can be so strong that internal parasitic SCRs are triggered, engendering irremediable damages to the IC if a low impedance path is offered between VCC and GND. If the current sense pin is often the seat of such spurious signals, the high–voltage pin can also be the source of problems in certain circumstances. During the turn–off sequence, e.g. when the user un–plugs the power supply, the controller is still fed by its VCC capacitor and keeps activating the MOSFET ON and OFF with a peak current limited by Rsense. Unfortunately, if the quality coefficient Q of the resonating network formed by Lp and Cbulk is low (e.g. the MOSFET Rdson + Rsense are small), conditions are met to make the circuit resonate and thus negatively bias the controller. Since we are talking about ms pulses, the amount of injected charge (Ω = I x t) immediately latches the controller which brutally discharges its VCC capacitor. If this VCC capacitor is of sufficient value, its stored energy damages the controller. Figure 21 depicts a typical negative shot occurring on the HV pin where the brutal VCC discharge testifies for latchup.
Simple and inexpensive cures exist to prevent from internal parasitic SCR activation. One of them consists in inserting a resistor in series with the high-voltage pin to keep the negative current to the lowest when the bulk becomes negative (Figure 22). Please note that the negative spike is clamped to \(-2 \times V_f\) due to the diode bridge. Also, the power dissipation of this resistor is extremely small since it only heats up during the startup sequence.

Another option (Figure 23) consists in wiring a diode from \(V_{CC}\) to the bulk capacitor to force \(V_{CC}\) to reach \(UVLO_{low}\) sooner and thus stops the switching activity before the bulk capacitor gets deeply discharged. For security reasons, two diodes can be connected in series.
## ORDERING INFORMATION

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<th>Device</th>
<th>Package</th>
<th>Shipping†</th>
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<tr>
<td>NCP1203D40R2G</td>
<td>SOIC−8 (Pb−Free)</td>
<td>2500 Units / Tape &amp; Reel</td>
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<td>2500 Units / Tape &amp; Reel</td>
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</tbody>
</table>

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

PDIP-8
CASE 626-05
ISSUE P

DATE 22 APR 2015

NOTES:
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACK-
AGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH
OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE
NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM
PLANES H WITH THE LEADS CONSTRAINED PERPENDICULAR
TO DATUM C.
6. DIMENSION b IS MEASURED AT THE LEAD TIPS WITH THE
LEADS UNCONSTRAINED.
7. DATUM PLANES H IS COINCIDENT WITH THE BOTTOM OF THE
LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE
Corners);

<table>
<thead>
<tr>
<th>INCHES</th>
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<tbody>
<tr>
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<td>b2</td>
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<td>M</td>
<td>3.81</td>
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<tr>
<td>b2</td>
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</table>

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC – IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. VCC

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rights of others.
SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

### SOLDERING FOOTPRINT*

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**STYLES ON PAGE 2**
### STYLE 1:
- **PIN 1. Emitter**
- 2. Collector
- 3. Collector
- 4. Emitter
- 5. Emitter
- 6. Base
- 7. Base
- 8. Emitter

### STYLE 2:
- **PIN 1. Collector, Die, #1**
- 2. Collector, #1
- 3. Collector, #2
- 4. Collector, #2
- 5. Base, #2
- 6. Emitter, #2
- 7. Base, #1
- 8. Emitter, #1

### STYLE 3:
- **PIN 1. Drain, Die #1**
- 2. Drain, #1
- 3. Drain, #2
- 4. Drain, #2
- 5. Gate, #2
- 6. Source, #2
- 7. Gate, #1
- 8. Source, #1

### STYLE 4:
- **PIN 1. Anode**
- 2. Base, #1
- 3. Base, #2
- 4. Collector, #2
- 5. Collector, #2
- 6. Emitter, #2
- 7. Anode
- 8. Common Cathode

### STYLE 8:
- **PIN 1. Collector, Die #1**
- 2. Collector, #1
- 3. Collector, #2
- 4. Collector, #2
- 5. Collector, #2
- 6. Collector, #2
- 7. Collector, #2
- 8. Collector, #1

**DESCRIPTION:**

- **98ASB42564B**
- **CASE 751–07**
- **ISSUE AK**

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