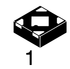
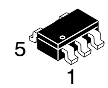
LDO Regulator - High PSRR

300 mA

NCP115



XDFN4
CASE 711AJ



TSOP−5
CASE 483

The NCP115 is 300 mA LDO that provides the engineer with a very stable, accurate voltage with low noise suitable for space constrained, noise sensitive applications. In order to optimize performance for battery operated portable applications, the NCP115 employs the dynamic quiescent current adjustment for very low I_Q consumption at no−load.

Features

- Operating Input Voltage Range: 1.7 V to 5.5 V
- Available in Fixed Voltage Options: 0.8 V to 3.6 V
  Contact Factory for Other Voltage Options
- Very Low Quiescent Current of Typ. 50 μA
- Soft Start Feature with Two V_{OUT} Slew Rate Speed
- Standby Current Consumption: Typ. 0.1 μA
- Low Dropout: 250 mV Typical at 300 mA @ 2.8 V
- ±1% Accuracy at Room Temperature
- High Power Supply Ripple Rejection: 70 dB at 1 kHz
- Thermal Shutdown and Current Limit Protections
- Available in XDFN4 and TSOP−5 Packages
- Stable with a 1 μF Ceramic Output Capacitor
- These are Pb−Free Devices

Typical Applicaitons

- PDAs, Mobile phones, GPS, Smartphones
- Wireless Handsets, Wireless LAN, Bluetooth®, Zigbee®
- Portable Medical Equipment
- Other Battery Powered Applications

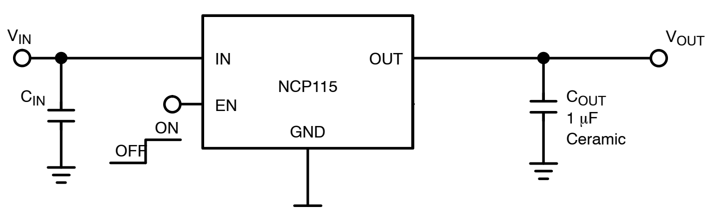
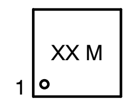
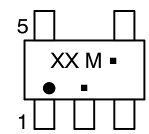


Figure 1. Typical Application Schematic

MARKING DIAGRAMS



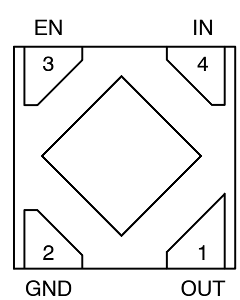
XX = Specific Device Code
M = Date Code



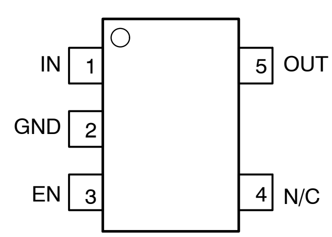
XX = Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)
*Date Code orientation and/or position may vary depending upon manufacturing location.

PIN CONNECTIONS



(Bottom View)



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 15 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 15.

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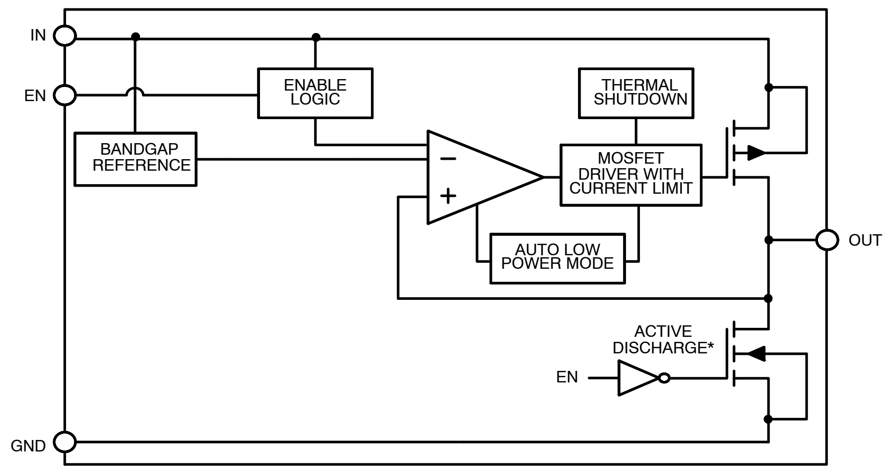


*Active output discharge function is present only in NCP115A and NCP115C devices.
yyy denotes the particular V_{OUT} option.

Figure 2. Simplified Schematic Block Diagram

PIN FUNCTION DESCRIPTION

Pin No. (XDFN4)	Pin No. (TSOP5)	Pin Name	Description
1	5	OUT	Regulated output voltage pin. A small ceramic capacitor with minimum value of 1 μF is needed from this pin to ground to assure stability.
2	2	GND	Power supply ground.
3	3	EN	Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode.
4	1	IN	Input pin. A small capacitor is needed from this pin to ground to assure stability.
–	4	N/C	Not connected. This pin can be tied to ground to improve thermal dissipation.
–	–	EPAD	Exposed pad should be connected directly to the GND pin. Soldered to a large ground copper plane allows for effective heat removal.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 V to 6 V	V
Output Voltage	V_{OUT}	−0.3 V to V_{IN} + 0.3 V or 6 V	V
Enable Input	V_{EN}	−0.3 V to 6 V	V
Output Short Circuit Duration	t_{SC}	∞	s
Maximum Junction Temperature	$T_{J(MAX)}$	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per EIA/JESD22−A114,
   ESD Machine Model tested per EIA/JESD22−A115,
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

THERMAL CHARACTERISTICS (Note 3)

Rating	Symbol	Value	Unit
Thermal Characteristics, XDFN4 1x1 mm Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	208	°C/W
Thermal Characteristics, TSOP−5 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	162	°C/W

3. Single component mounted on 1 oz, FR 4 PCB with 645 mm^2 Cu area.

ELECTRICAL CHARACTERISTICS −40°C ≤ T_J ≤ 85°C; V_{IN} = $V_{OUT(NOM)}$ + 1 V for V_{OUT} options greater than 1.5 V. Otherwise V_{IN} = 2.5 V, whichever is greater; I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1 μF, unless otherwise noted. V_{EN} = 0.9 V. Typical values are at T_J = +25°C. Min./Max. are for T_J = −40°C and T_J = +85°C respectively (Note 4).

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage			V_{IN}	1.7		5.5	V
Output Voltage Accuracy	−40°C ≤ T_J ≤ 85°C	V_{OUT} ≤ 2.0 V	V_{OUT}	−40		+40	mV
		V_{OUT} > 2.0 V		−2		+2	%
Line Regulation	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 5.5 V (V_{IN} ≥ 1.7 V)		Reg_{LINE}		0.01	0.1	%/V
Load Regulation − XDFN4 package	I_{OUT} = 1 mA to 300 mA		Reg_{LOAD}		12	30	mV
Load Regulation − TSOP−5 package					28	45	
Dropout Voltage − XDFN4 package (Note 5)	I_{OUT} = 300 mA	V_{OUT} = 1.8 V	V_{DO}		425	560	mV
		V_{OUT} = 2.8 V			250	320	
		V_{OUT} = 3.3 V			215	260	
Dropout Voltage − TSOP−5 package (Note 5)	I_{OUT} = 300 mA	V_{OUT} = 1.8 V	V_{DO}		445	580	mV
		V_{OUT} = 2.8 V			270	340	
		V_{OUT} = 3.3 V			235	280	
Output Current Limit	V_{OUT} = 90% $V_{OUT(nom)}$		I_{CL}	300	600		mA
Quiescent Current	I_{OUT} = 0 mA		I_Q		50	95	μA
Shutdown Current	V_{EN} ≤ 0.4 V, V_{IN} = 5.5 V		I_{DIS}		0.01	1	μA
EN Pin Threshold Voltage High Threshold Low Threshold	V_{EN} Voltage increasing V_{EN} Voltage decreasing		V_{EN_HI} V_{EN_LO}	0.9		0.4	V
V_{OUT} Slew Rate (Note 6)	V_{OUT} = 3.3 V, I_{OUT} = 10 mA	Normal (version A and B)	V_{OUT_SR}		190		mV/μs
		Slow (version C and D)			20		
EN Pin Input Current	V_{EN} = 5.5 V		I_{EN}		0.3	1.0	μA
Power Supply Rejection Ratio	V_{IN} = 3.8 V, V_{OUT} = 3.5 V I_{OUT} = 10 mA	f = 1 kHz	PSRR		70		dB
Output Noise Voltage	f = 10 Hz to 100 kHz		V_N		70		μV_{rms}
Thermal Shutdown Temperature	Temperature increasing from T_J = +25°C		T_{SD}		160		°C
Thermal Shutdown Hysteresis	Temperature falling from T_{SD}		T_{SDH}		20		°C
Active Output Discharge Resistance	V_{EN} < 0.4 V, Version A and C only		R_{DIS}		100		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T_J = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
5. Characterized when V_{OUT} falls 100 mV below the regulated voltage at V_{IN} = $V_{OUT(NOM)}$ + 1 V.
6. Please refer OPN to determine slew rate. NCP115A, NCP115B − Normal speed. NCP115C, NCP115D − slower speed

TYPICAL CHARACTERISTICS

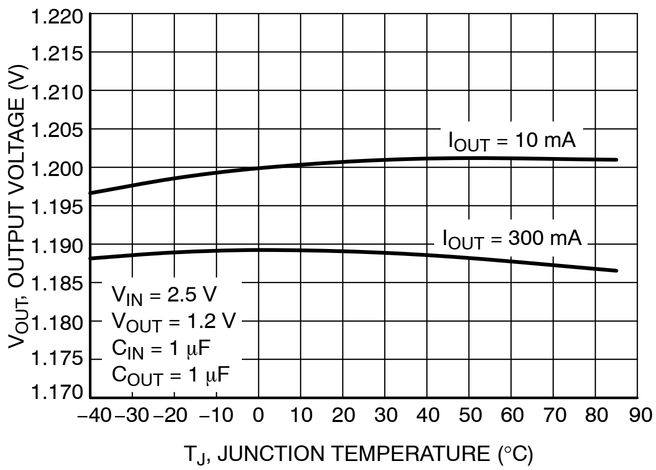


Figure 3. Output Voltage vs. Temperature – V_{OUT} = 1.2 V – XDFN4

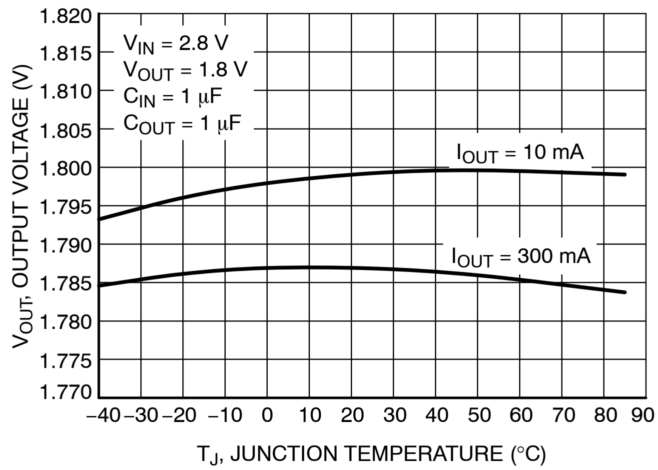


Figure 4. Output Voltage vs. Temperature – V_{OUT} = 1.8 V – XDFN4

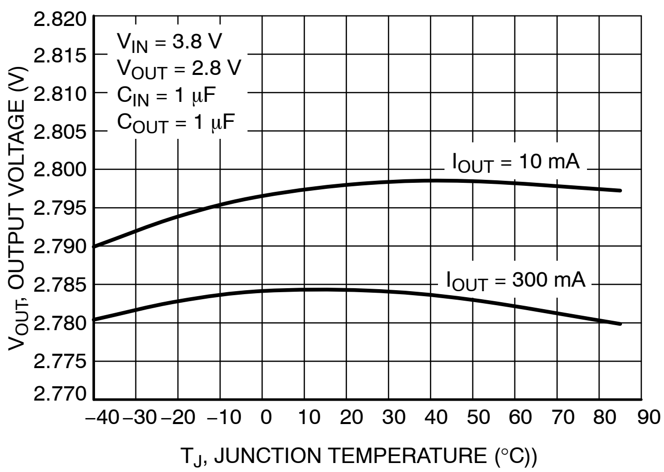


Figure 5. Output Voltage vs. Temperature – V_{OUT} = 2.8 V – XDFN4

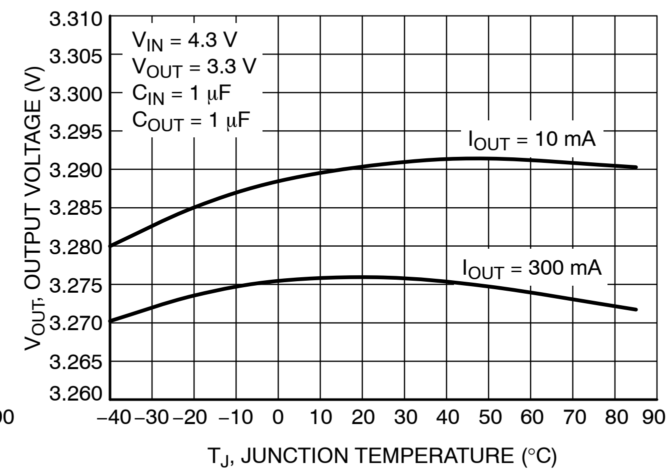


Figure 6. Output Voltage vs. Temperature – V_{OUT} = 3.3 V – XDFN4

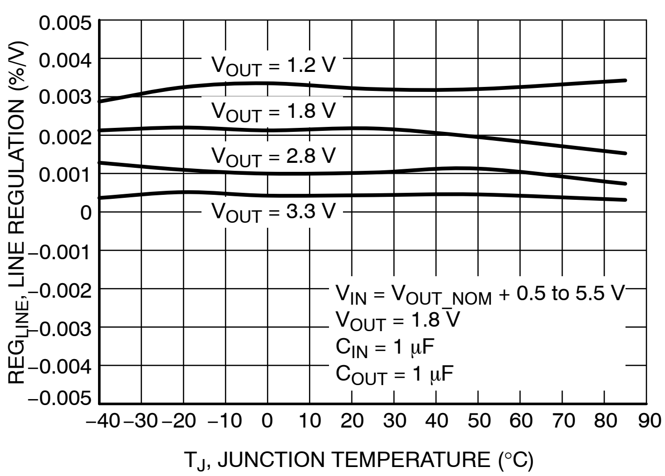


Figure 7. Line Regulation vs. Temperature

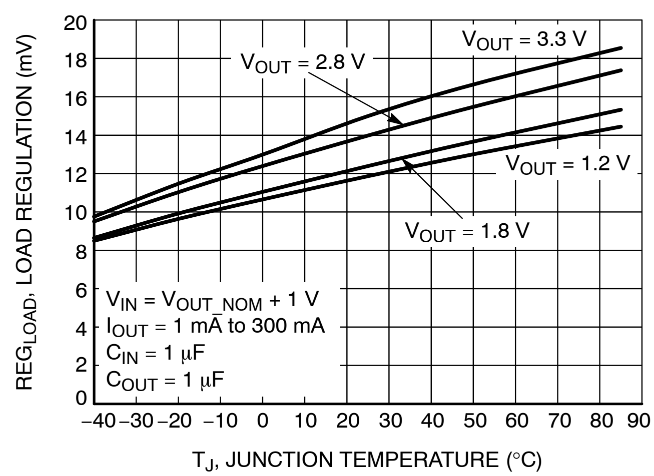


Figure 8. Load Regulation vs. Temperature – XDFN4

TYPICAL CHARACTERISTICS (continued)

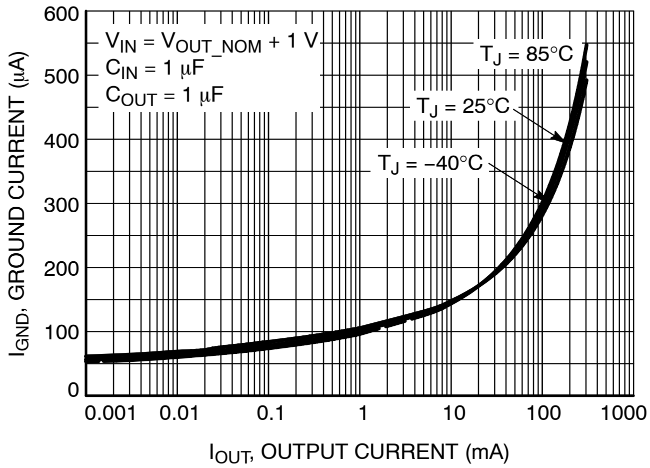


Figure 9. Ground Current vs. Load Current

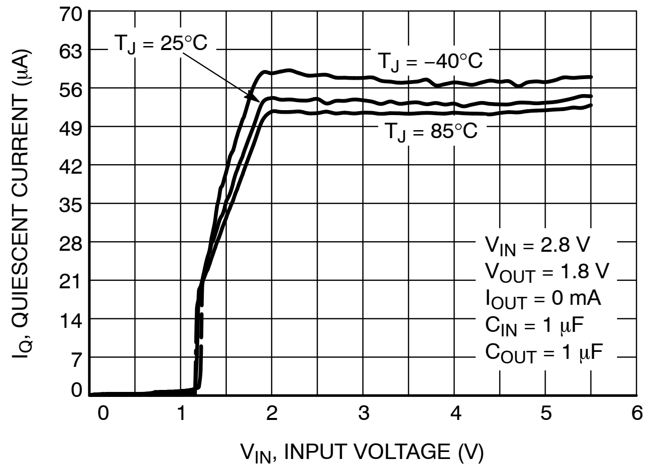


Figure 10. Quiescent Current vs. Input Voltage $V_{OUT} = 1.8$ V

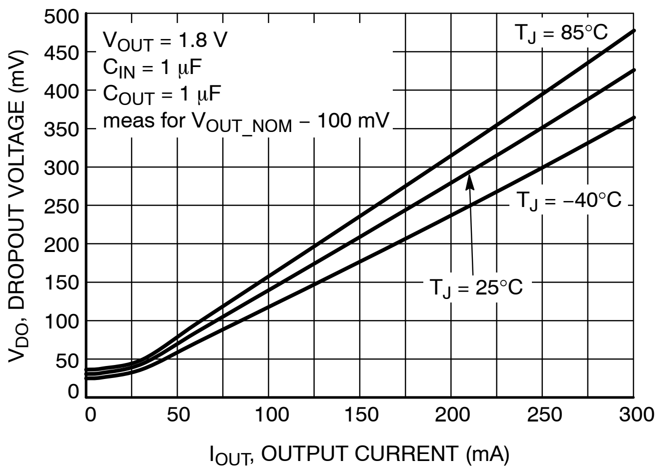


Figure 11. Dropout Voltage vs. Load Current – $V_{OUT} = 1.8$ V

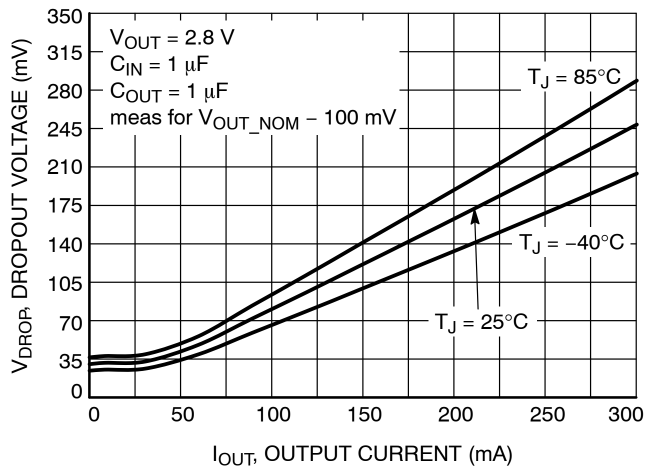


Figure 12. Dropout Voltage vs. Load Current – $V_{OUT} = 2.8$ V

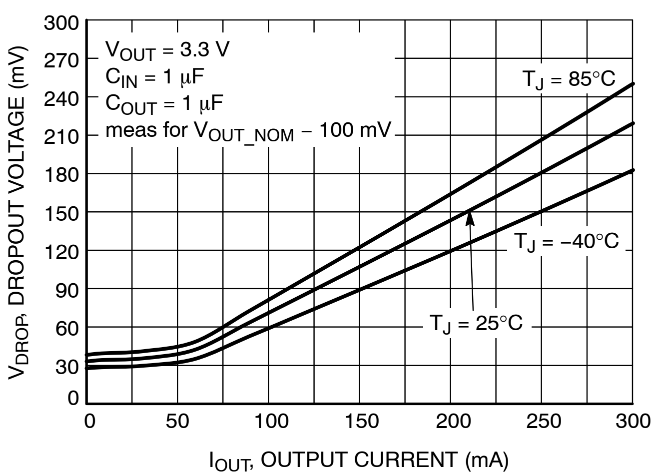


Figure 13. Dropout Voltage vs. Load Current – $V_{OUT} = 3.3$ V

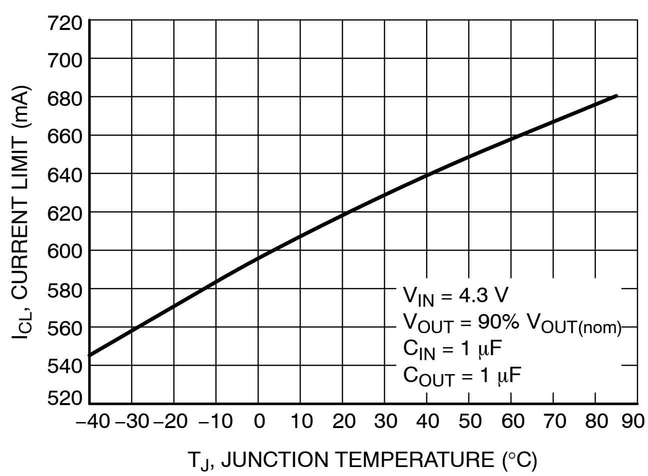


Figure 14. Current Limit vs. Temperature

TYPICAL CHARACTERISTICS (continued)

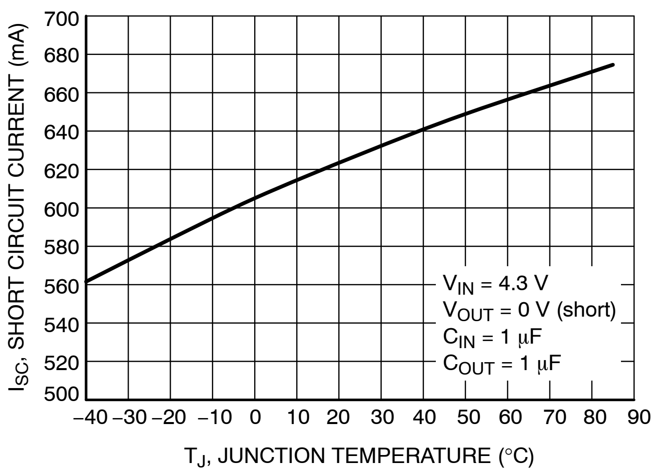


Figure 15. Short Circuit Current vs. Temperature

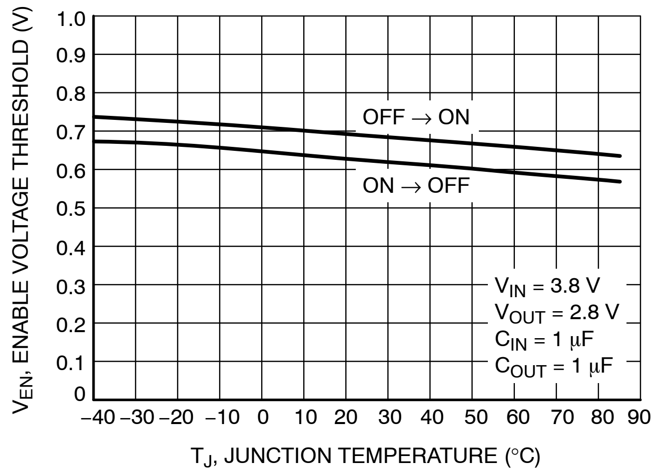


Figure 16. Enable Thresholds Voltage

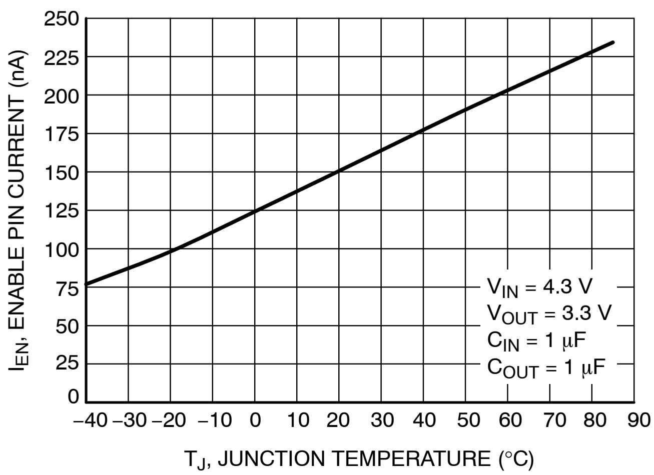


Figure 17. Current to Enable Pin vs. Temperature

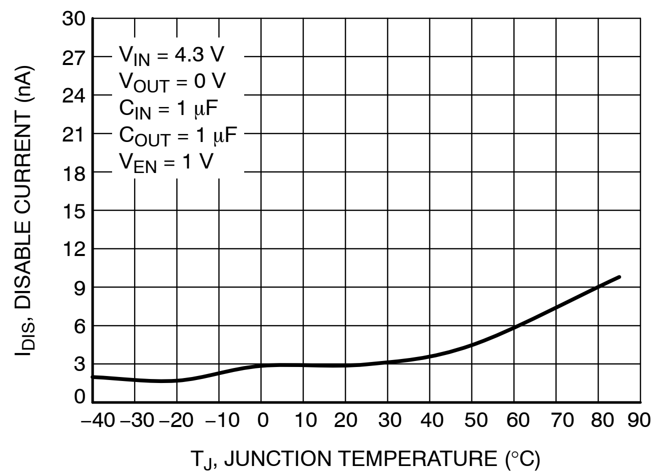


Figure 18. Disable Current vs. Temperature

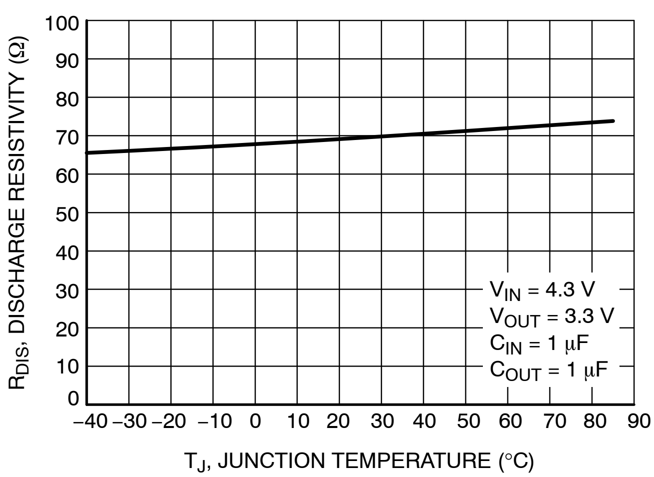


Figure 19. Discharge Resistance vs. Temperature

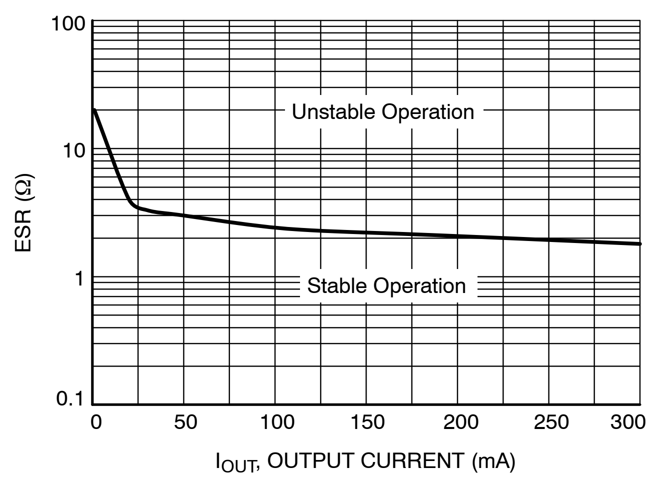
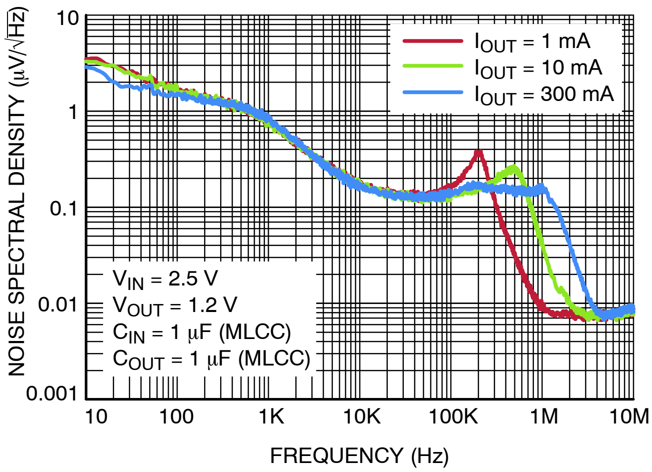


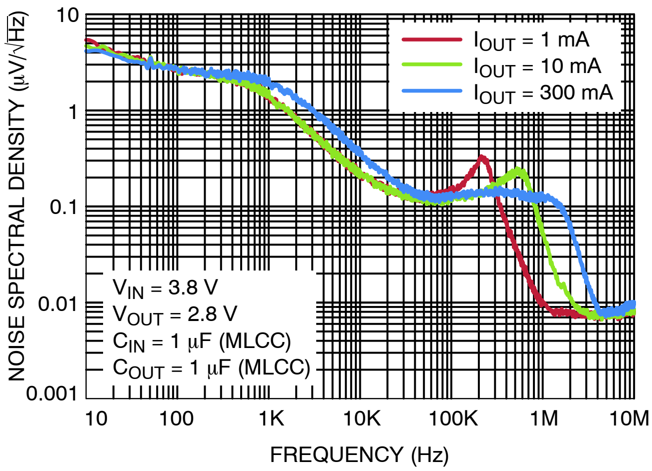
Figure 20. Maximum C_{OUT} ESR Value vs. Load Current

TYPICAL CHARACTERISTICS (continued)



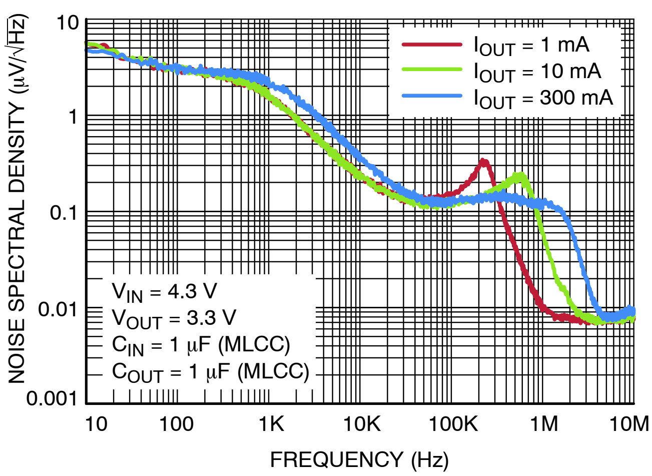
I_{OUT}	RMS Output Noise (μV_{RMS})	
	10 Hz – 100 kHz	100 Hz – 100 kHz
1 mA	65.6	61.9
10 mA	63.1	59.5
300 mA	62.3	60.3

Figure 21. Output Voltage Noise Spectral Density – V_{OUT} = 1.2 V



I_{OUT}	RMS Output Noise (μV_{RMS})	
	10 Hz – 100 kHz	100 Hz – 100 kHz
1 mA	93.4	87.9
10 mA	92.1	86.6
300 mA	119.3	115.6

Figure 22. Output Voltage Noise Spectral Density – V_{OUT} = 2.8 V



I_{OUT}	RMS Output Noise (μV_{RMS})	
	10 Hz – 100 kHz	100 Hz – 100 kHz
1 mA	104.0	98.0
10 mA	102.9	96.7
300 mA	131.4	127.0

Figure 23. Output Voltage Noise Spectral Density – V_{OUT} = 3.3 V

TYPICAL CHARACTERISTICS (continued)

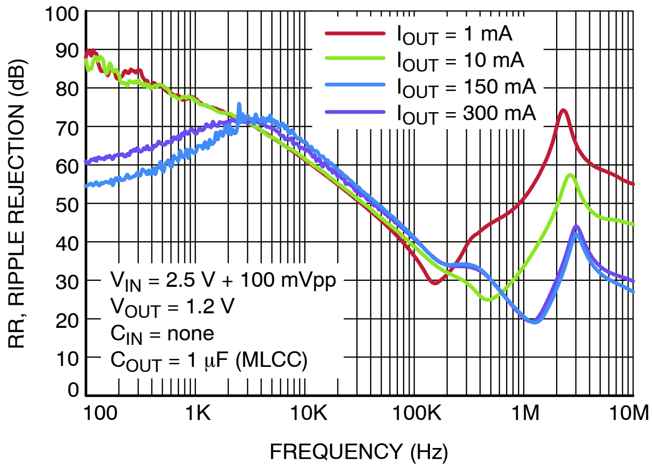


Figure 24. Power Supply Rejection Ratio, V_{OUT} = 1.2 V

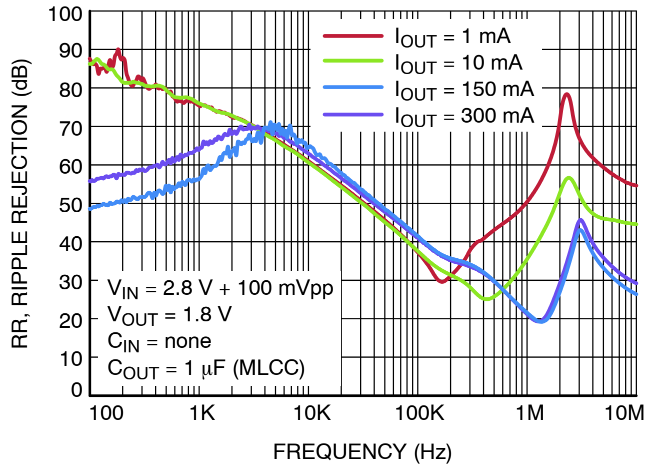


Figure 25. Power Supply Rejection Ratio, V_{OUT} = 1.8 V

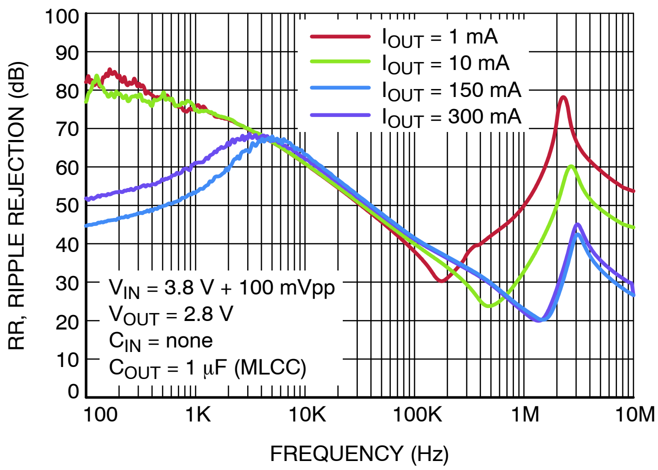


Figure 26. Power Supply Rejection Ratio, V_{OUT} = 2.8 V

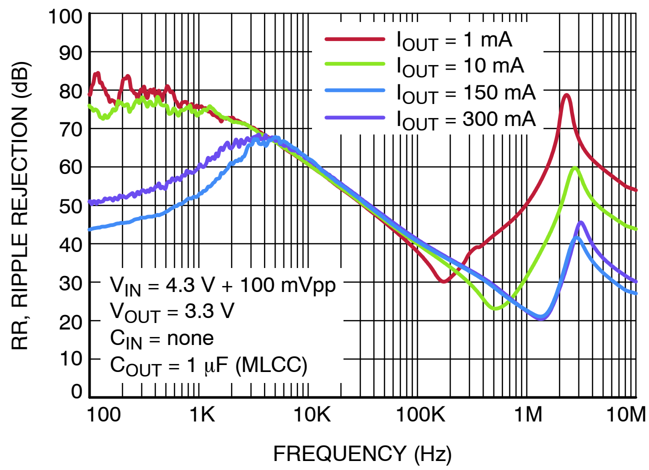


Figure 27. Power Supply Rejection Ratio, V_{OUT} = 3.3 V

TYPICAL CHARACTERISTICS (continued)

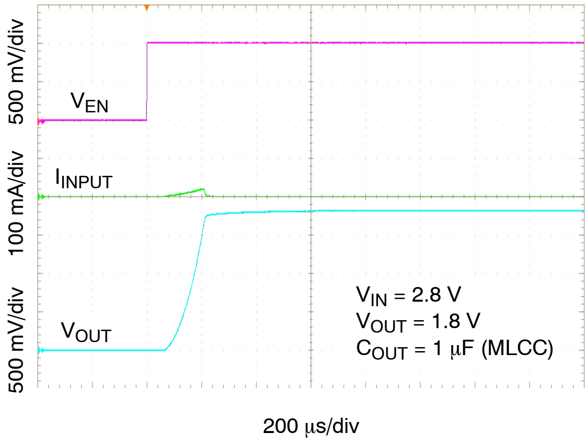


Figure 28. Enable Turn−on Response – I_{OUT} = 0 mA, Slow Option – C

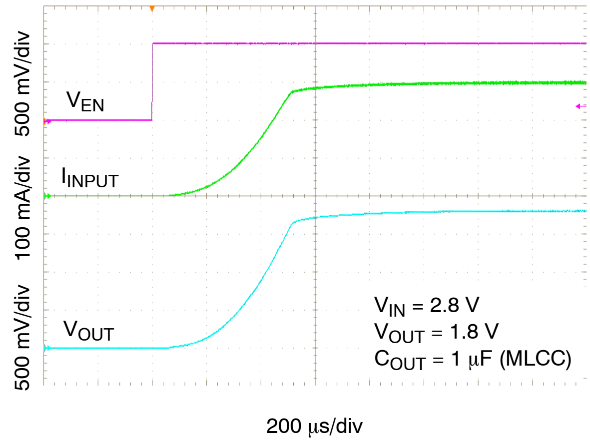


Figure 29. Enable Turn−on Response – I_{OUT} = 300 mA, Slow Option – C

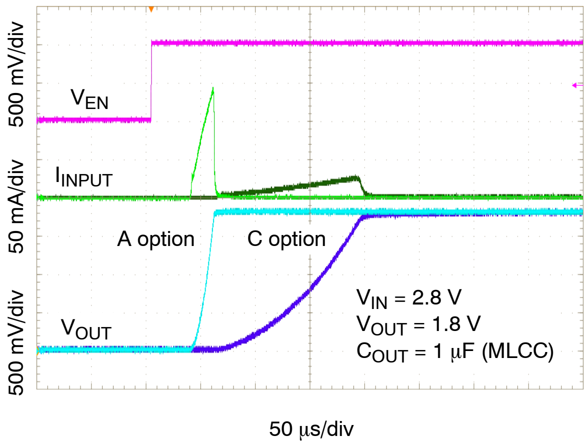


Figure 30. V_{OUT} Slew−Rate Comparison A and C option – I_{OUT} = 10 mA

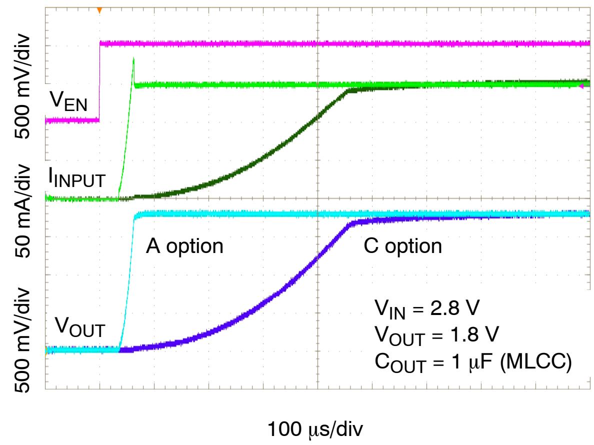


Figure 31. V_{OUT} Slew−Rate Comparison A and C option – I_{OUT} = 300 mA

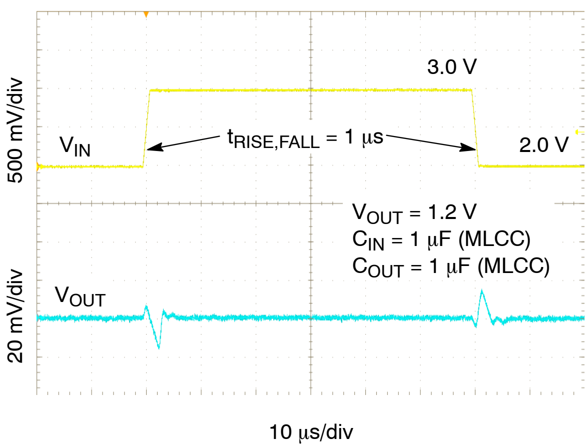


Figure 32. Line Transient Response – I_{OUT} = 10 mA

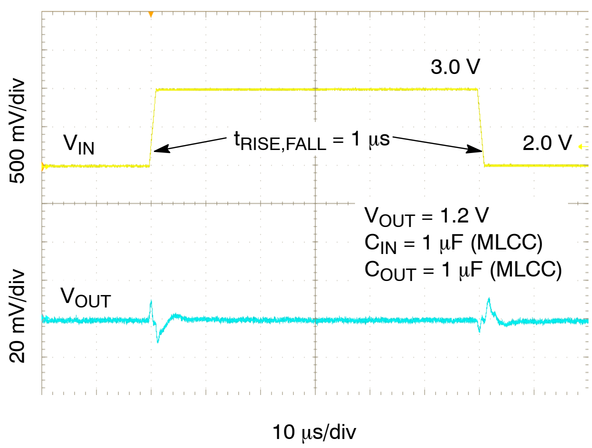


Figure 33. Line Transient Response – I_{OUT} = 300 mA

TYPICAL CHARACTERISTICS (continued)

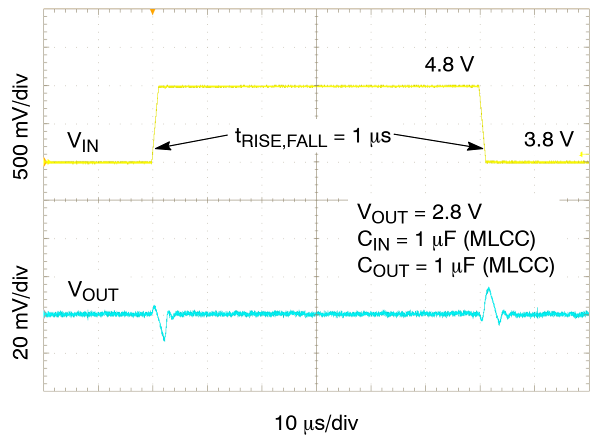


Figure 34. Line Transient Response – I_{OUT} = 10 mA

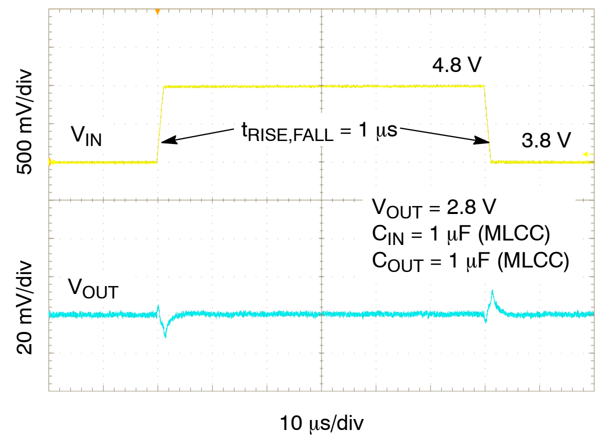


Figure 35. Line Transient Response – I_{OUT} = 300 mA

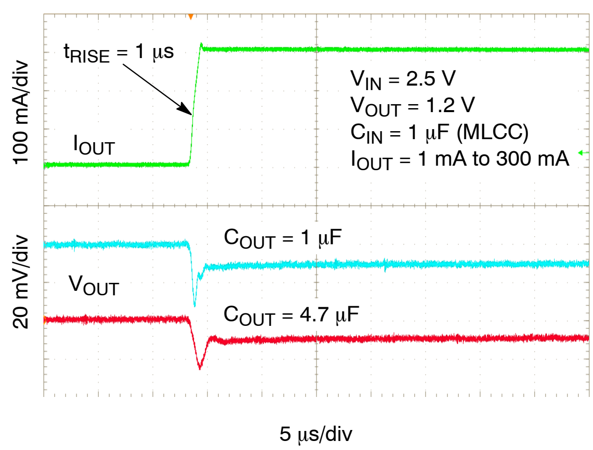


Figure 36. Load Transient Response – V_{OUT} = 1.2 V

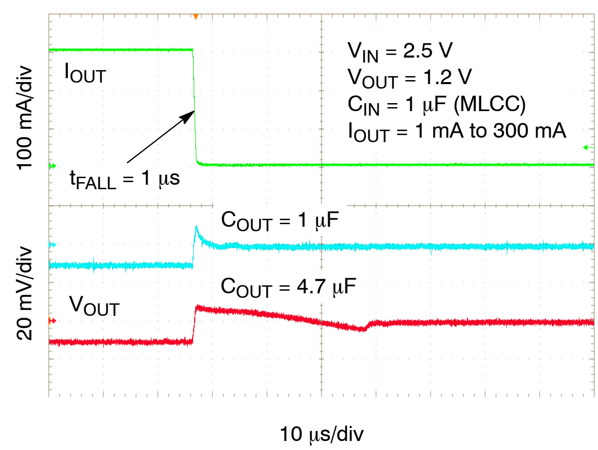


Figure 37. Load Transient Response – V_{OUT} = 1.2 V

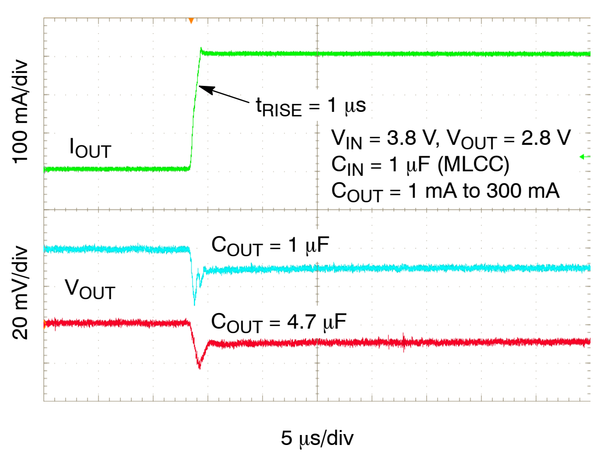


Figure 38. Load Transient Response – V_{OUT} = 2.8 V

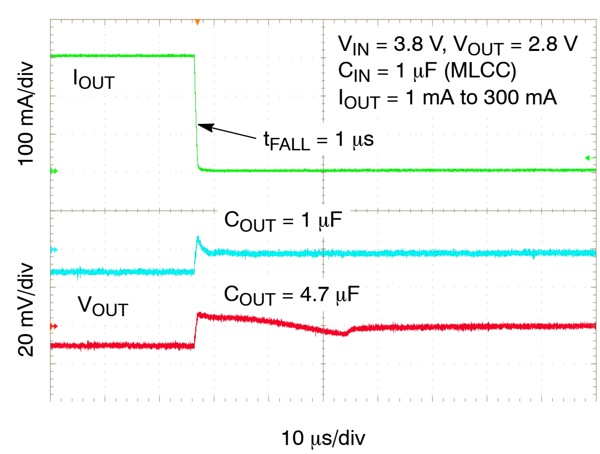


Figure 39. Load Transient Response – V_{OUT} = 2.8 V

TYPICAL CHARACTERISTICS (continued)

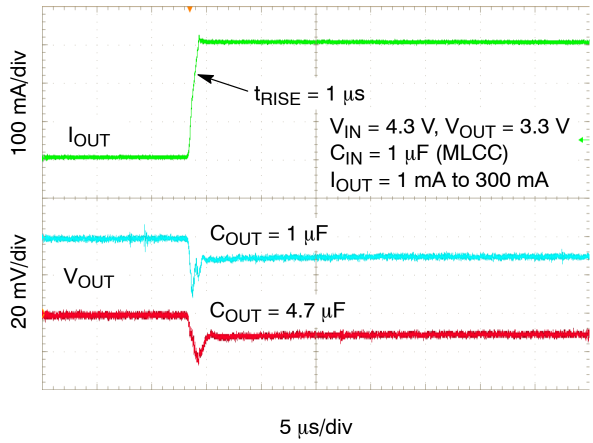


Figure 40. Load Transient Response – V_{OUT} = 3.3 V

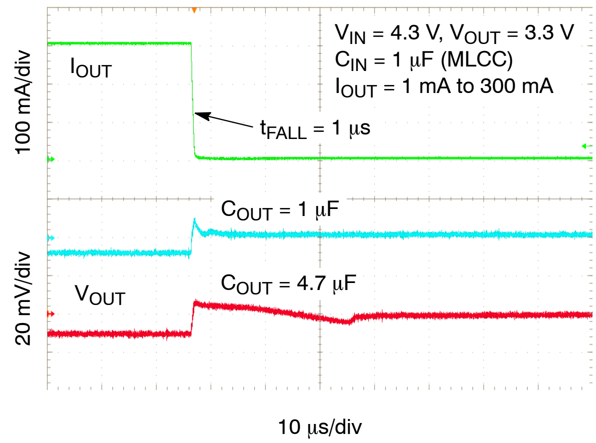


Figure 41. Load Transient Response – V_{OUT} = 3.3 V

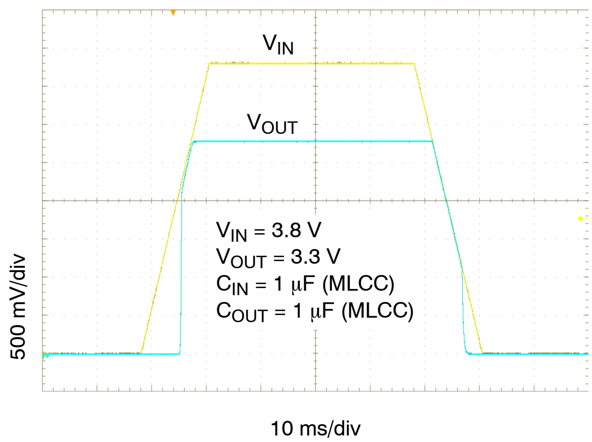


Figure 42. Turn−on/off – Slow Rising V_{IN} – I_{OUT} = 10 mA

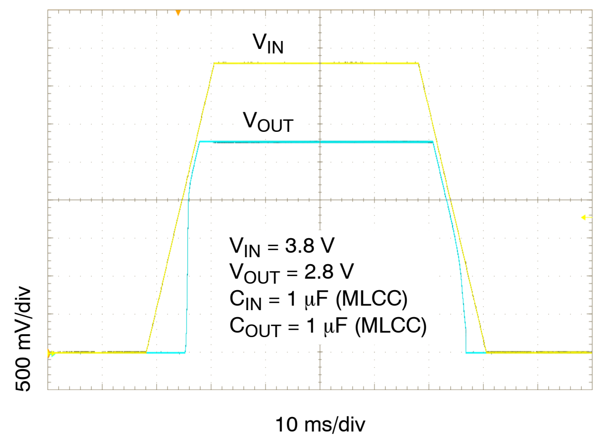


Figure 43. Turn−on/off – Slow Rising V_{IN} – I_{OUT} = 300 mA

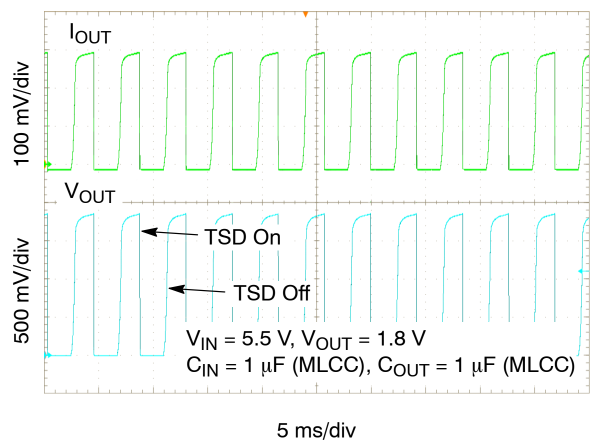


Figure 44. Overheating Protection – TSD

APPLICATIONS INFORMATION

General

The NCP115 is a high performance 300 mA Low Dropout Linear Regulator. This device delivers very high PSRR (over 70 dB at 1 kHz) and excellent dynamic performance as load/line transients. In connection with very low quiescent current this device is very suitable for various battery powered applications such as tablets, cellular phones, wireless and many others. The device is fully protected in case of output overload, output short circuit condition and overheating, assuring a very robust design.

Input Capacitor Selection (C_{IN})

It is recommended to connect at least a 1 μF Ceramic X5R or X7R capacitor as close as possible to the IN pin of the device. This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto constant input voltage. There is no requirement for the min. /max. ESR of the input capacitor but it is recommended to use ceramic capacitors for their low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and source resistance during sudden load current changes. Larger input capacitor may be necessary if fast and large load transients are encountered in the application.

Output Decoupling (C_{OUT})

The NCP115 requires an output capacitor connected as close as possible to the output pin of the regulator. The recommended capacitor value is 1 μF and X7R or X5R dielectric due to its low capacitance variations over the specified temperature range. The NCP115 is designed to remain stable with minimum effective capacitance of 0.47 μF to account for changes with temperature, DC bias and package size. Especially for small package size capacitors such as 0402 the effective capacitance drops rapidly with the applied DC bias.

There is no requirement for the minimum value of Equivalent Series Resistance (ESR) for the C_{OUT} but the maximum value of ESR should be less than 1.8 Ω. Larger output capacitors and lower ESR could improve the load transient response or high frequency PSRR. It is not recommended to use tantalum capacitors on the output due to their large ESR. The equivalent series resistance of tantalum capacitors is also strongly dependent on the temperature, increasing at low temperature.

Enable Operation

The NCP115 uses the EN pin to enable/disable its device and to deactivate/activate the active discharge function.

If the EN pin voltage is <0.4 V the device is guaranteed to be disabled. The pass transistor is turned−off so that there is virtually no current flow between the IN and OUT. The active discharge transistor is active so that the output voltage V_{OUT} is pulled to GND through a 100 Ω resistor. In the disable state the device consumes as low as typ. 10 nA from the V_{IN}.

If the EN pin voltage >0.9 V the device is guaranteed to be enabled. The NCP115 regulates the output voltage and the active discharge transistor is turned−off.

The EN pin has internal pull−down current source with typ. value of 300 nA which assures that the device is turned−off when the EN pin is not connected. In the case where the EN function isn’t required the EN should be tied directly to IN.

Output Current Limit

Output Current is internally limited within the IC to a typical 600 mA. The NCP115 will source this amount of current measured with a voltage drops on the 90% of the nominal V_{OUT}. If the Output Voltage is directly shorted to ground (V_{OUT} = 0 V), the short circuit protection will limit the output current to 630 mA (typ). The current limit and short circuit protection will work properly over whole temperature range and also input voltage range. There is no limitation for the short circuit duration.

Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold (T_{SD} − 160°C typical), Thermal Shutdown event is detected and the device is disabled. The IC will remain in this state until the die temperature decreases below the Thermal Shutdown Reset threshold (T_{SDU} − 140°C typical). Once the IC temperature falls below the 140°C the LDO is enabled again. The thermal shutdown feature provides the protection from a catastrophic device failure due to accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking.

Power Dissipation

As power dissipated in the NCP115 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part.

The maximum power dissipation the NCP115 can handle is given by:

$$P_{D(MAX)} = \frac{\left[85^{\circ}C - T_A\right]}{\theta_{JA}} \qquad \text{(eq. 1)}$$

The power dissipated by the NCP115 for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN}\left(I_{GND}@I_{OUT}\right) + I_{OUT}\left(V_{IN} - V_{OUT}\right) \qquad \text{(eq. 2)}$$

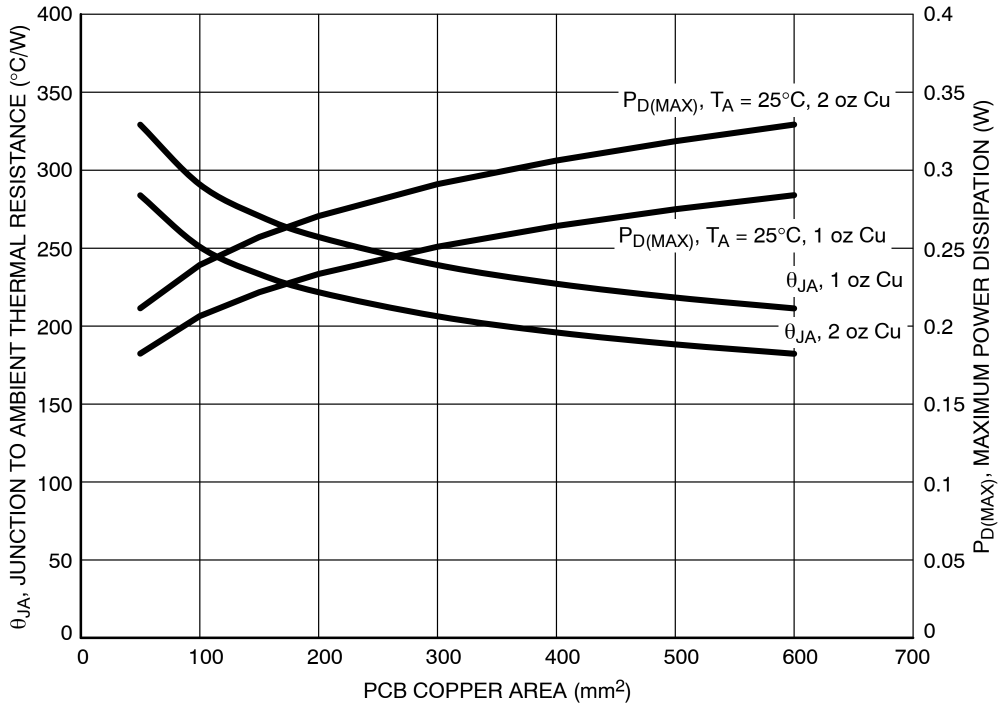


Figure 45. θ_{JA} and $P_{D\ (MAX)}$ vs. Copper Area (XDFN4)

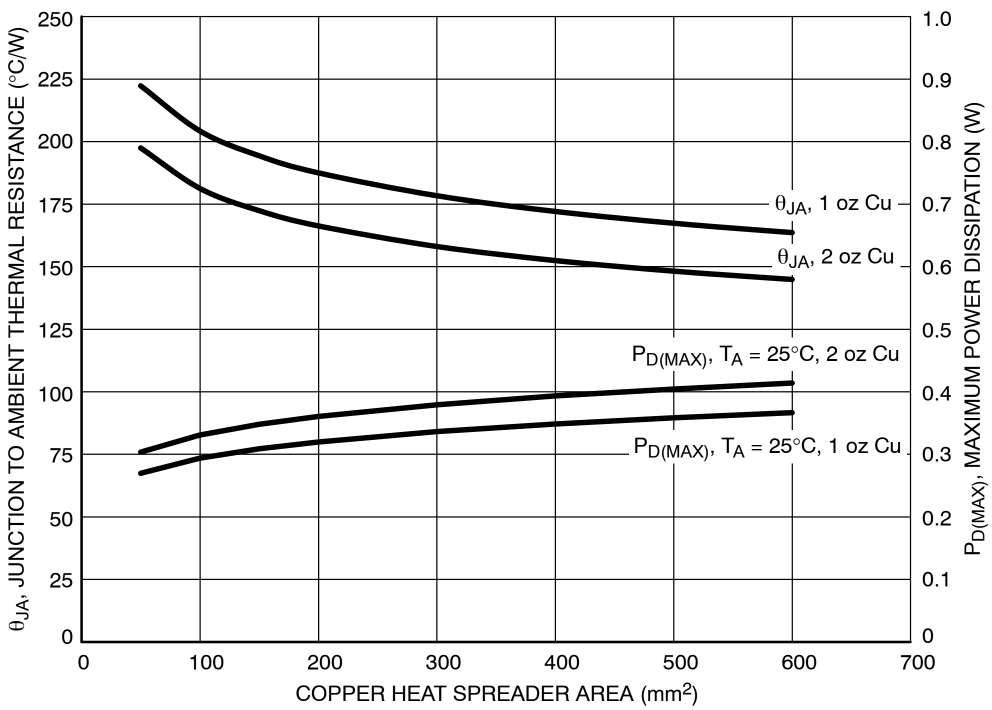


Figure 46. θ_{JA} and $P_{D\ (MAX)}$ vs. Copper Area (TSOP−5)

Reverse Current

The PMOS pass transistor has an inherent body diode which will be forward biased in the case that $V_{OUT} > V_{IN}$. Due to this fact in cases, where the extended reverse current condition can be anticipated the device may require additional external protection.

Power Supply Rejection Ratio

The NCP115 features very good Power Supply Rejection ratio. If desired the PSRR at higher frequencies in the range 100 kHz − 10 MHz can be tuned by the selection of C_{OUT} capacitor and proper PCB layout.

Turn−On Time

The turn−on time is defined as the time period from EN assertion to the point in which VOUT will reach 98% of its nominal value. This time is dependent on various application conditions such as $V_{OUT(NOM)}$ C_{OUT} and T_A.

The NCP115 provides two options of V_{OUT} ramp−up time. The NCP115A and NCP115B have normal slew rate, typical 190 mV/μs and NCP115C and NCP115D provide slower option with typical value 20 mV/μs which is suitable for camera sensor and other sensitive devices.

PCB Layout Recommendations

To obtain good transient performance and good regulation characteristics place C_{IN} and C_{OUT} capacitors close to the device pins and make the PCB traces wide. In order to minimize the solution size, use 0402 capacitors. Larger copper area connected to the pins will also improve the device thermal resistance. The actual power dissipation can be calculated from the equation above (Equation 2). Expose pad should be tied the shortest path to the GND pin.

ORDERING INFORMATION – XDFN4 PACKAGE

Device	Voltage Option	Marking	Description	Package	Shipping†
NCP115AMX100TCG (Note 7)	1.0 V	QN	300 mA, Active Discharge, Normal Slew−rate	XDFN4 (Pb−Free)*	3000 or 5000 / Tape & Reel (Note 7)
NCP115AMX105TCG (Note 7)	1.05 V	QM			
NCP115AMX110TBG (Note 7)	1.1 V	QL			
NCP115AMX110TCG (Note 7)					
NCP115AMX120TCG (Note 7)	1.2 V	QA			
NCP115AMX150TCG (Note 7)	1.5 V	QE			
NCP115AMX180TBG (Note 7)	1.8 V	QC			
NCP115AMX180TCG (Note 7)					
NCP115AMX250TCG (Note 7)	2.5 V	QF			
NCP115AMX280TBG (Note 7)	2.8 V	QG			
NCP115AMX280TCG (Note 7)					
NCP115AMX300TCG (Note 7)	3.0 V	QK			
NCP115AMX330TBG (Note 7)	3.3 V	QH			
NCP115AMX330TCG (Note 7)					
NCP115CMX120TCG (Note 7)	1.2 V	RE	300 mA, Active Discharge, Slow Slew−rate		3000 or 5000 / Tape & Reel (Note 7)
NCP115CMX150TCG (Note 7)	1.5 V	RG			
NCP115CMX180TCG (Note 7)	1.8 V	RA			
NCP115CMX250TCG (Note 7)	2.5 V	RH			
NCP115CMX280TBG (Note 7)	2.8 V	RC			
NCP115CMX280TCG (Note 7)					
NCP115CMX300TBG (Note 7)	3.0 V	RK			
NCP115CMX300TCG (Note 7)					
NCP115CMX330TCG (Note 7)	3.3 V	RD			

DISCONTINUED (Note 8)

NCP115AMX120TBG (Note 7)	1.2 V	QA	300 mA, Active Discharge, Normal Slew−rate	XDFN4 (Pb−Free)*	3000 or 5000 / Tape & Reel (Note 7)
NCP115CMX100TCG (Note 7)	1.0 V	RN	300 mA, Active Discharge, Slow Slew−rate		
NCP115CMX105TCG (Note 7)	1.05 V	RM			
NCP115CMX110TBG (Note 7)	1.1 V	RF			
NCP115CMX110TCG (Note 7)		RF			
NCP115CMX120TBG (Note 7)	1.2 V	RE			
NCP115CMX150TBG (Note 7)	1.5 V	RG			
NCP115CMX180TBG (Note 7)	1.8 V	RA			
NCP115CMX330TBG (Note 7)	3.3 V	RD			

ORDERING INFORMATION − TSOP−5 PACKAGE

Device	Voltage Option	Marking	Description	Package	Shipping†
NCP115ASN120T2G	1.2 V	QAE	300 mA, Active Discharge, Normal Slew−rate	TSOP−5 (Pb−Free)*	3000 / Tape & Reel
NCP115ASN150T2G	1.5 V	QAF			
NCP115ASN180T1G	1.8 V	QAA			
NCP115ASN180T2G	1.8 V	QAA			
NCP115ASN250T2G	2.5 V	QAG			
NCP115ASN280T2G	2.8 V	QAH			
NCP115ASN330T2G	3.3 V	QAK			

DISCONTINUED (Note 8)

NCP115ASN120T1G	1.2 V	QAE	300 mA, Active Discharge, Normal Slew−rate	TSOP−5 (Pb−Free)*	3000 / Tape & Reel
NCP115ASN150T1G	1.5 V	QAF			
NCP115ASN250T1G	2.5 V	QAG			

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
7. Product processed after October 1, 2022 are shipped with quantity 5000 units / Tape & Reel.
8. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

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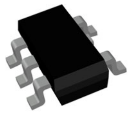
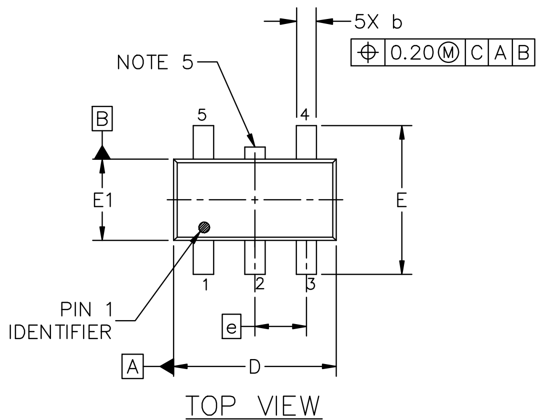
ZigBee is a registered trademark of ZigBee Alliance.



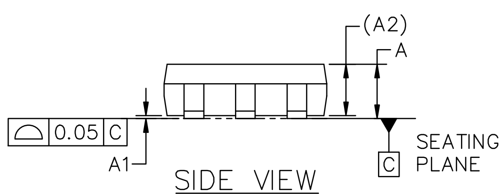
TSOP−5 3.00x1.50x0.95, 0.95P
CASE 483
ISSUE P

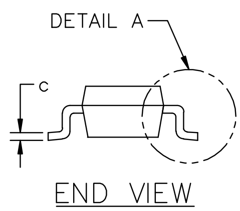
DATE 01 APR 2024



NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.





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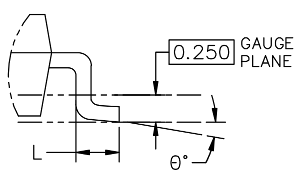
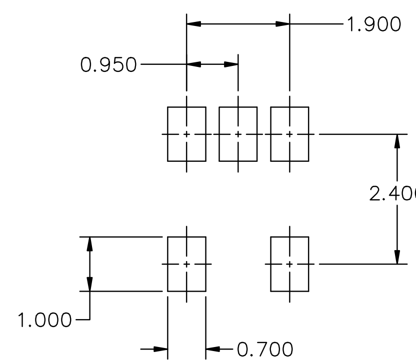
	MIN.	NOM.	MAX.
A	0.900	1.000	1.100
A1	0.010	0.055	0.100
A2	0.950 REF.		
b	0.250	0.375	0.500
c	0.100	0.180	0.260
D	2.850	3.000	3.150
E	2.500	2.750	3.000
E1	1.350	1.500	1.650
e	0.950 BSC		
L	0.200	0.400	0.600
θ	0°	5°	10°



DETAIL "A"
SCALE 2:1



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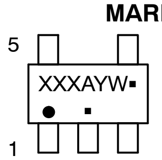
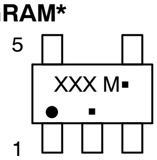


Analog

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package



Discrete/Logic

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

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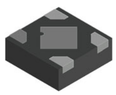
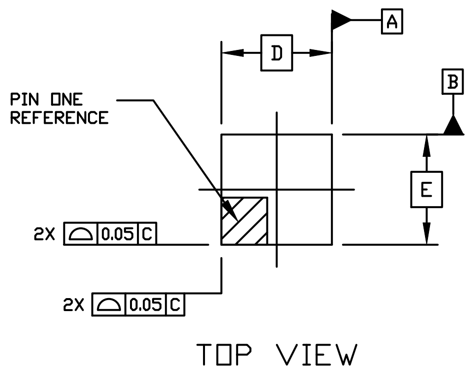
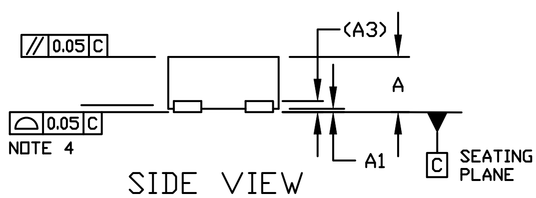


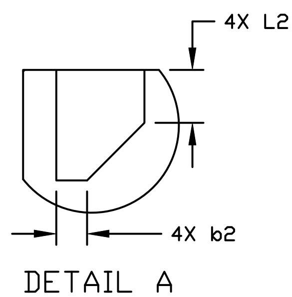
XDFN4 1.0x1.0, 0.65P
CASE 711AJ
ISSUE C

DATE 08 MAR 2022

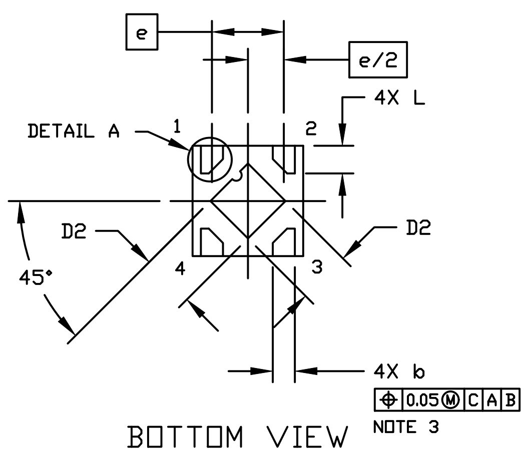


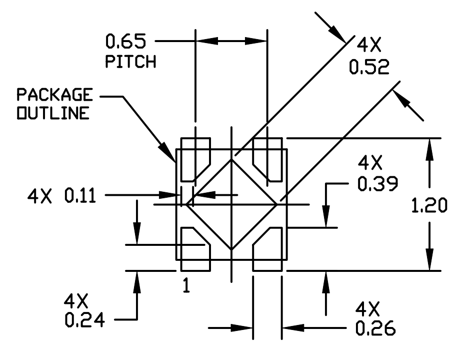


NOTES:
1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.20 FROM THE TERMINAL TIPS.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.33	0.38	0.43
A1	0.00	---	0.05
A3	0.10 REF		
b	0.15	0.20	0.25
b2	0.02	0.07	0.12
D	0.90	1.00	1.10
D2	0.43	0.48	0.53
E	0.90	1.00	1.10
e	0.65 BSC		
L	0.20		0.30
L2	0.07		0.17





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**GENERIC
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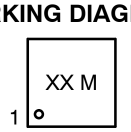

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M = Date Code

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