NCL30051

PFC and Half-Bridge Resonant Combo Controller for LED Lighting

The NCL30051 is a combination of PFC and half−bridge resonant controllers optimized for off−line LED lighting solutions. This device integrates all the features needed to implement a highly efficient and small form factor LED Driver/Power Supply. It contains a critical conduction mode (CrM) power factor correction (PFC) boost controller and a half−bridge resonant controller with a built−in 600 V driver. The half−bridge stage operates at a fixed frequency, greatly simplifying the control implementations. The output (current or voltage) regulation is achieved by adjusting the PFC stage output voltage − based on a control signal generated external to the NCL30051.

This device includes an enable input on the PFC feedback pin, open feedback loop protection and PFC overvoltage and undervoltage detectors. Other features included in the NCL30051 are a 600 V startup circuit and an adjustable frequency oscillator with a divide by 2 circuit to assure true symmetric duty ratio. The controllers are properly sequenced, simplifying system design.

Features

- Voltage Mode CrM Power Factor Correction Controller
- PFC Open Feedback Loop Protection
- PFC Undervoltage Detector
- PFC Overvoltage Detector
- Half−Bridge Stage with 600 V High Side Gate Drive
- State Machine Ensures Proper Turn−on and Turn−off of Half−Bridge Stage
- Controllers are Properly Sequenced for Fault Free Operation
- Non−Latching Fault Management
- Internal 600 V Startup Circuit
- Wide Temperature Range of −40°C to +125°C
- This is a Pb−Free Device

Typical Applications

- High Efficiency LED Drivers and Power Supplies
- Electronic Control Gear
- Lighting Ballasts

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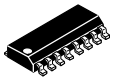
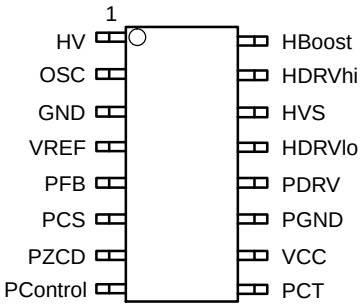
MARKING DIAGRAM



SOIC−16
D SUFFIX
CASE 751B

A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

PIN CONNECTIONS



SOIC−16

ORDERING INFORMATION

Device	Package	Shipping†
NCL30051DR2G	SOIC−16 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

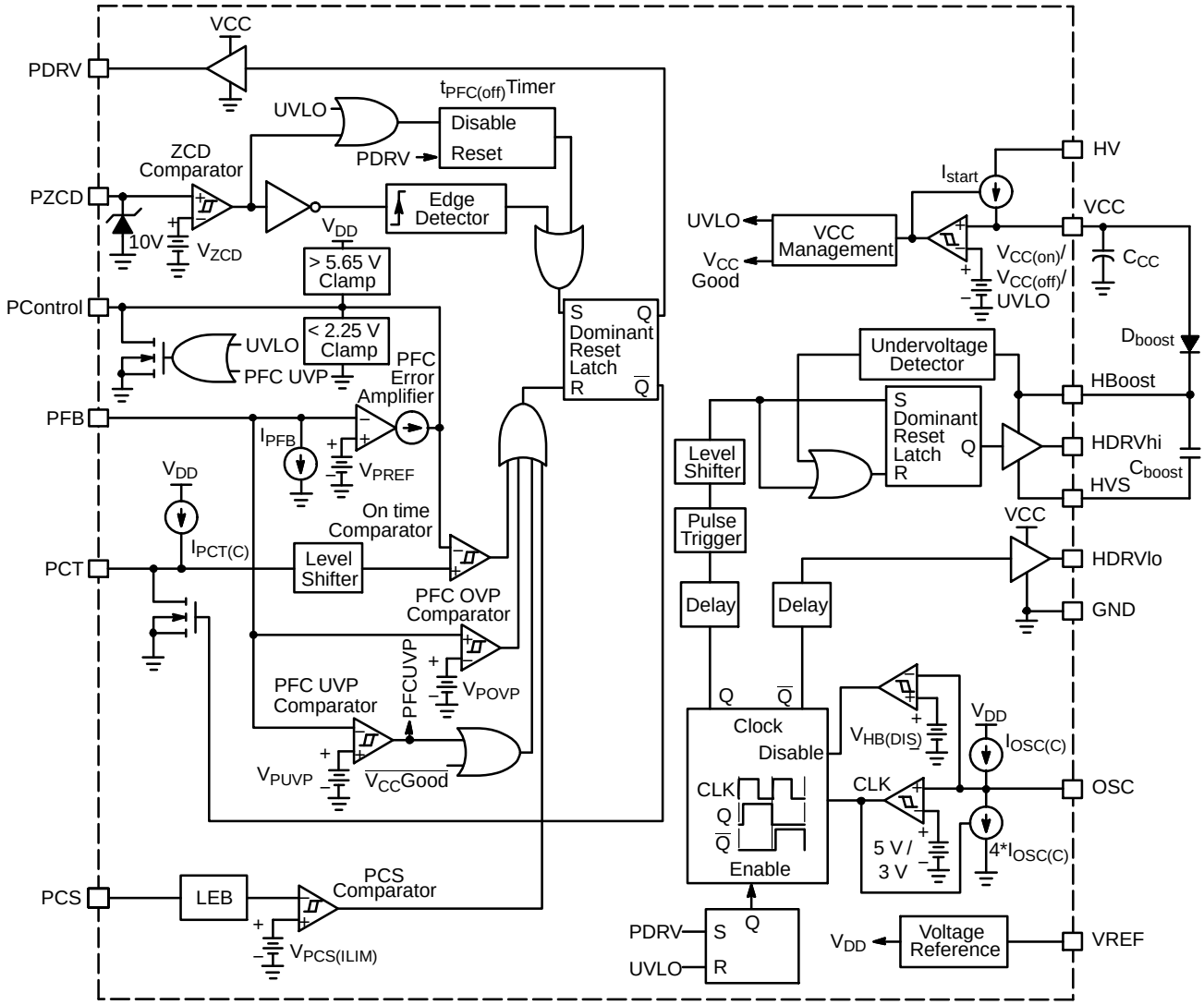


Figure 1. Functional Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	HV	This is the input of the high voltage startup regulator and connects directly to the bulk voltage. A constant current source supplies current from this pin to the V_{CC} capacitor, eliminating the need for an external startup resistor. The charge current is 7.5 mA (typical).
2	OSC	A capacitor on this pin adjusts the frequency of the internal oscillator. The oscillator sets the frequency of the half−bridge controller. Each half−bridge switch operates at half the oscillator frequency. The OSC pin also serves as a disable input for the half−bridge stage. The half−bridge stage is disabled by pulling down this pin below its disable threshold, $V_{HB(DIS)}$, typically 1.955 V.
3	GND	Analog ground.
4	VREF	Reference voltage. The capacitor on this pin decouples the internal reference. A 0.1 μF capacitor needs to be connected between this pin and ground.
5	PFB	PFC voltage feedback input. Connect to PFC output using a resistive divider network. The voltage on this pin is compared to a 2.5 V reference (typical) to regulate the PFC output voltage. The voltage on this pin is also used to detect PFC undervoltage and overvoltage conditions. In the typical intended application, the PFB pin voltage will set an upper bound on the PFC output voltage, while the actual PFC voltage control will be exercised by a control signal generated on the secondary side to provide accurate LED current/voltage control.
6	PCS	PFC regulator current sense input. A voltage ramp proportional to the PFC switch current is applied to this pin. The current sense threshold, $V_{PCS(ILIM)}$, is typically 0.84 V. A 110 ns (typical) leading edge blanking circuit filters the current sense signal at the start of each cycle.
7	PZCD	PFC inductor zero current detector. The inductor current is monitored using an auxiliary winding on the PFC inductor. The PFC drive signal is enabled during a high to low transition on the PZCD pin. A series resistor limits the current into the PZCD pin. The watchdog timer is disabled while the PZCD voltage is above the ZCD arming threshold, $V_{ZCD(high)}$. It is re−enabled once the voltage drops below the ZCD trigger threshold, $V_{ZCD(low)}$. This feature can be used to disable PFC drive pulses.
8	PControl	PFC control voltage. This pin connects to the output of the PFC error amplifier. The error amplifier is a transconductance amplifier. A compensation network between this pin and grounds sets the PFC loop bandwidth. The PFC control voltage is compared to a level shifted version of V_{PCT} to control the PFC duty ratio. In the typical intended application, the PControl voltage will be controlled by a secondary side control signal through an optocoupler. The optocoupler signal is diode ORed to the internally generated PControl signal and the lower of the two signals dictates the PFC on-time.
9	PCT	PFC on time control capacitor. A 270 μA (typical) current source charges a capacitor connected between this pin and ground. Once the level shifted PCT voltage reaches $V_{PControl}$, the PFC drive signal is disabled and the PCT capacitor is discharged.
10	VCC	Positive input supply. This pin connects to an external capacitor for energy storage. An internal current source supplies current from HV to this pin. Once the V_{CC} voltage reaches $V_{CC(on)}$ (15.3 V typical), the current source turns off and the controller is enabled. The current source turns on once V_{CC} falls to $V_{CC(off)}$ (9.3 V typical). During normal operation, power is supplied to the IC via this pin by means of an auxiliary winding.
11	PGND	Ground connection for PDRV and HDRVlo. Tie to the power stage return with a short trace.
12	PDRV	PFC switch gate drive control signal. The source and sink drive capability is limited to 60 Ω and 15 Ω (typical), respectively. A discrete driver may be needed to drive the external MOSFET.
13	HDRVlo	Half−bridge low side switch gate drive control signal. The source and sink drive capability is limited to 75 Ω and 15 Ω (typical), respectively. A discrete driver may be needed to drive the half bridge switch.
14	HVS	Half−bridge high side driver source connection. This pin connects directly to the bridge terminal and can float up to 600 V.
15	HDRVhi	Half−bridge high side switch gate drive control signal. The source and sink drive capability is limited to 75 Ω and 15 Ω (typical), respectively. The supply terminals of the high side driver connect to the HBoost and HVS pins. A discrete driver may be needed to drive the half bridge switch.
16	HBoost	Supply voltage of the high side gate driver. A charge pump generates a bootstrap voltage floating on top of the HVS voltage. A diode between the VCC and HBoost pins provides a charge path. The bootstrap voltage is V_{CC} minus a diode drop.

Table 2. MAXIMUM RATINGS (Notes 1 and 2)

Rating	Symbol	Value	Unit
High Voltage Input Voltage	V_{HV}	−0.3 to 600	V
High Voltage Input Current	I_{HV}	10	mA
Supply Input Voltage	V_{CC}	−0.3 to 20	V
Supply Input Current	I_{CC}	10	mA
Oscillator Input Voltage	V_{OSC}	−0.3 to V_{REF}	V
Oscillator Input Current	I_{OSC}	10	mA
Bandgap Reference Decoupling Output Voltage	V_{REF}	−0.3 to 9	V
Bandgap Reference Decoupling Output Current	I_{REF}	10	mA
PFC Feedback Voltage Input Voltage	V_{PFB}	−0.3 to 10	V
PFC Feedback Voltage Input Current	I_{PFB}	10	mA
PFC Current Sense Input Voltage	V_{PCS}	−0.3 to 10	V
PFC Current Sense Input Current	I_{PCS}	10	mA
PFC Zero Current Detection Input Voltage	V_{PZCD}	−0.3 to 10	V
PFC Zero Current Detection Input Current	I_{PZCD}	10	mA
PFC Control Input Voltage	$V_{PControl}$	−0.3 to V_{REF}	V
PFC Control Input Current	$I_{PControl}$	1.2	mA
PFC On Time Control Input Voltage	V_{PCT}	−0.3 to V_{REF}	V
PFC On Time Control Input Current	I_{PCT}	9	mA
PFC Drive Signal Voltage	V_{PDRV}	−0.3 to V_{CC}	V
PFC Drive Signal Current	I_{PDRV}	100	mA
Half−Bridge Low Side Driver Input Voltage	V_{HDRVlo}	−0.3 to V_{CC}	V
Half−Bridge Low Side Driver Input Current	I_{HDRVlo}	100	mA
Half−Bridge High Side Driver Source Connection Input Voltage	V_{HVS}	−1.0 to 600	V
Half−Bridge High Side Driver Source Connection Input Current	I_{HVS}	100	mA
Half−Bridge High Side Driver Input Voltage	V_{HDRVhi}	−1.3 to V_{HVS}+V_{CC}	V
Half−Bridge High Side Driver Input Current	I_{HDRVhi}	100	mA
Half−Bridge High Side Driver Charge Pump Input Voltage	V_{HBoost}	−0.3 to V_{HVS}+V_{CC}	V
Half−Bridge High Side Driver Charge Pump Input Current	I_{HBoost}	100	mA
High Side Boost Circuit Supply Voltage (between HBoost and HVS pins)	$V_{HBoost(supply)}$	−0.3 to V_{CC}	V
High Side Boost Circuit Supply Voltage (between HBoost and HVS pins)	$I_{HBoost(supply)}$	100	mA
Half−Bridge High Side Driver Source Connection Slew Rate	dV_{HVS}/dt	50	V/ns
Junction Temperature (Biased)	T_J	150	°C
Storage Temperature Range	T_{stg}	–60 to 150	°C
Power Dissipation (T_A = 25°C, 1 Oz Cu, 0.155 Sq Inch, Printed Circuit Copper Clad) D Suffix, Plastic Package Case 751B−05 (SOIC−16)	P_D	0.95	W
Thermal Resistance, Junction to Ambient (1 Oz Cu, 0.155 Sq Inch, Printed Circuit Copper Clad) D Suffix, Plastic Package Case 751B−05 (SOIC−16)	$R_{\theta JA}$	130	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device(s) contains ESD protection and exceeds the following tests:
   Pins 1, 14, 15 and 16 rated to the maximum voltage of the respective pins based on the maximum ratings table.
   All Other Pins: Human Body Model 1500 V per JEDEC Standard JESD22−A114E.
   Machine Model 150 V per JEDEC Standard JESD22−A115−A.
2. This device contains Latch−Up protection and exceeds ± 100 mA per JEDEC Standard JESD78.

Table 3. ELECTRICAL CHARACTERISTICS (V_{HV} = open, V_{PFB} = 2.4 V, V_{PCS} = 0 V, V_{PZCD} = 5 V, $V_{PControl}$ = open, V_{CC} = 15 V, V_{PDRV} = open, V_{HDRVlo} = open, V_{HVS} = 0 V, V_{HDRVhi} = open, V_{HBoost} = 15 V, C_{OSC} = 2200 pF, C_{VREF} = 0.1 μF, C_{PCT} = 1000 pF, for typical values T_J = 25°C, for min/max values, T_J is −40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
STARTUP AND SUPPLY CIRCUITS						
Supply Voltage						V
Startup Threshold	V_{CC} Increasing	$V_{CC(on)}$	14.3	15.3	16.3	
Minimum Enable Threshold	V_{CC} Decreasing	$V_{CC(enable)}$	13.6	14.6	15.6	
Minimum Operating Voltage	V_{CC} Decreasing	$V_{CC(off)}$	8.5	9.3	10.0	
Supply Current						mA
Device Disabled/Fault	$V_{PFB} = V_{PUVP(low)}$	I_{CC1}	0.8	1.4	1.8	
Device Switching	(Note 3)	I_{CC2}	1.8	2.4	3.0	
Startup Current	$V_{CC} = V_{CC\ (on)} - 0.2$ V, V_{HV} = 50 V	I_{start}	3.0	7.5	10.5	mA
Startup Circuit Off−State Leakage Current	V_{HV} = 600 V, $V_{CC} = V_{CC\ (on)} + 0.2$ V	$I_{HV(off)}$	–	15	50	μA
BANDGAP REFERENCE						
Reference Voltage	C_{REF} = 0.1 μF	V_{REF}	6.605	7.000	7.295	V
OSCILLATOR						
Half−Bridge Clock Frequency	V_{HVS} = 50 V	f_{clock}	13.5	15.5	16.5	kHz
Maximum Half−Bridge Clock Frequency	C_{OSC} = open	$f_{clock(MAX)}$	75	–	–	kHz
PFC ERROR AMPLIFIER						
PFC Feedback Voltage Reference		V_{PREF}				V
	0°C < T_J < 125°C		2.42	2.50	2.58	
	−40°C < T_J < 125°C		2.40	–	2.60	
PFC Feedback Voltage Reference Regulation with Line	$V_{CC(on)} + 0.2$ V < V_{CC} < 20 V	$V_{PREF(line)}$	−15	–	15	mV
Error Amplifier Drive Capability						μA
Sink	$V_{PControl}$ = 4 V, V_{PFB} = 5 V	$I_{EA(SNK)}$	60	80	–	
Source	$V_{PControl}$ = 4 V, V_{PFB} = 0.5 V	$I_{EA(SRC)}$	−60	−80	–	
Open Loop Error Amplifier Transconductance	$V_{PControl}$ = 4 V, V_{PFB} = 2.4 V and 2.6 V	Gm	60	95	–	μS
Feedback Input Pulldown Current Source	V_{PFB} = 3 V	I_{PFB}	0.5	1.2	1.5	μA
Error Amplifier Maximum Output Voltage	$I_{PControl}$ = 10 μA	$V_{EA(OH)}$	5.30	5.65	6.00	V
Error Amplifier Minimum Output Voltage	$I_{PControl}$ = −10 μA	$V_{EA(OL)}$	2.10	2.25	2.40	V
Error Amplifier Output Voltage Range	$V_{EA(OH)} - V_{EA(OL)}$	ΔV_{EA}	3.1	3.4	3.7	V

3. Resistor/capacitor parallel combination (39 pF || 20 kΩ) between drive pin and driver supply and between xDRVxx and GND pins.

Table 4. ELECTRICAL CHARACTERISTICS (V_{HV} = open, V_{PFB} = 2.4 V, V_{PCS} = 0 V, V_{PZCD} = 5 V, $V_{PControl}$ = open, V_{CC} = 15 V, V_{PDRV} = open, V_{HDRVlo} = open, V_{HVS} = 0 V, V_{HDRVhi} = open, V_{HBoost} = 15 V, C_{OSC} = 2200 pF, C_{VREF} = 0.1 μF, C_{PCT} = 1000 pF, for typical values T_J = 25°C, for min/max values, T_J is −40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
PFC CURRENT SENSE						
Current Sense Threshold Voltage		$V_{PCS(ILIM)}$	0.78	0.84	0.92	V
Current Sense Input Bias Current	V_{PCS} = 2 V	I_{PCS}	−1	0	1	μA
Leading Edge Blanking Duration		$t_{PCS(LEB)}$	40	110	200	ns
Propagation Delay	V_{PCS} = $V_{PCS(ILIM)}$ + 1 V	$t_{PCS(delay)}$	–	90	250	ns
PFC ZERO CURRENT DETECTION						
ZCD Threshold Voltage Arming Threshold Trigger Threshold	 V_{PZCD} increasing V_{PZCD} decreasing	 $V_{ZCD(high)}$ $V_{ZCD(low)}$	 1.9 1.3	 2.1 1.5	 2.3 1.7	V
ZCD Voltage Hysteresis		$V_{ZCD(HYS)}$	400	600	800	mV
ZCD Input Bias Current	V_{PZCD} = 1 V V_{PZCD} = 5 V	$I_{PZCD(bias1)}$ $I_{PZCD(bias2)}$	−1 −1	– –	1 1	μA
PFC MAXIMUM OFF TIME						
Maximum Off Time		$t_{PFC(off)}$	50	180	350	μs
PFC ON TIME RAMP GENERATOR						
ON time Capacitor Charge Current	V_{PCT} = 0 V	$I_{PCT(C)}$	220	270	300	μA
On Time Capacitor Discharge Time	V_{PCT} = 2.4 V to 0.6 V	$t_{PCT(D)}$	–	70	300	ns
ON Time Capacitor Peak Voltage		$V_{PCT(peak)}$	2.6	3.0	3.4	V
Minimum Duty Ratio	V_{PFB} = 3.0 V, V_{PZCD} = 0 V	D_{PMIN}	0	–	–	%
Maximum On Time Detect Delay	V_{PCT} = $V_{PCT(peak)}$ + 1 V	$t_{PCT(delay)}$	–	250	375	ns
Voltage Delta between PControl Voltage Needed to Generate PDRV Pulses and $V_{EA(OL)}$	ΔV_{EA} − $V_{PCT(peak)}$	$V_{PCT(offset)}$	250	400	550	mV
PFC OVERVOLTAGE and UNDERVOLTAGE						
Overvoltage Detector Threshold Voltage	Midpoint between high and low threshold, $V_{PControl}$ = 4 V	V_{POVP}	1.03* V_{PREF}	1.05* V_{PREF}	1.07* V_{PREF}	V
Overvoltage Comparator Hysteresis Window	$V_{PControl}$ = 4V	$V_{POVP(HYS)}$	5	30	60	mV
Propagation Delay	V_{PFB} = V_{PREF} + 1 V	$t_{POVP(delay)}$	–	400	800	ns
Undervoltage Detector Threshold Voltage	V_{PFB} increasing V_{PFB} decreasing	$V_{PUVP(high)}$ $V_{PUVP(low)}$	– 175	290 230	350 –	mV
Undervoltage Comparator Hysteresis	V_{PFB} increasing	$V_{PUVP(HYS)}$	20	60	100	mV
PFC DRIVER						
PFC Driver Rise Time	10% to 90% (Note 4)	$t_{PDRV(rise)}$	–	18	–	ns
PFC Driver Fall Time	90% to 10% (Note 4)	$t_{PDRV(fall)}$	–	9	–	ns
PFC Driver High State Voltage	I_{PDRV} = −8 mA	$V_{PDRV(OH)}$	14.00	14.55	–	V
PFC Driver Low State Voltage	I_{PDRV} = 8 mA	$V_{PDRV(OL)}$	–	0.12	0.50	V

4. Resistor/capacitor parallel combination (39 pF || 20 kΩ) between PDRV and driver supply and between PDRV and GND pins.

Table 5. ELECTRICAL CHARACTERISTICS (V_{HV} = open, V_{PFB} = 2.4 V, V_{PCS} = 0 V, V_{PZCD} = 5 V, $V_{PControl}$ = open, V_{CC} = 15 V, V_{PDRV} = open, V_{HDRVlo} = open, V_{HVS} = 0 V, V_{HDRVhi} = open, V_{HBoost} = 15 V, C_{OSC} = 2200 pF, C_{VREF} = 0.1 μF, C_{PCT} = 1000 pF, for typical values T_J = 25°C, for min/max values, T_J is −40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
HALF BRIDGE HIGH SIDE DRIVER						
Half−Bridge High Side Driver Rise Time	10% to 90% (Note 5)	$t_{HDRVhi(rise)}$	–	18	–	ns
Half−Bridge High Side Driver Fall Time	90% to 10% (Note 5)	$t_{HDRVhi(fall)}$	–	9	–	ns
High State Voltage	I_{HDRVhi} = −4 mA	$V_{HDRVhi(OH)}$	14.0	14.7	–	V
Low State Voltage	I_{HDRVhi} = 4 mA	$V_{HDRVhi(OL)}$	–	0.06	0.5	V
High Side Driver Duty Ratio	10 to 90% to 10% transitions, V_{HSVS} = 50 V (Note 5)	$D_{HDRVhiMAX}$	44	48	50	%
Boost Supply Undervoltage Threshold		$V_{HBoost(UVLO)}$	4	6.1	8.0	V
Boost Current Consumption	HDRVhi switching, between HDRVhi and HVS (Note 5)	$I_{CC(Boost)}$	–	0.1	0.5	mA
HVS Leakage Current	T_J = 25°C, V_{HVS} = 600 V, V_{HBoost} = 600 V	$I_{HVS(off)}$	–	0.1	1	μA
HALF BRIDGE LOW SIDE DRIVER						
Half−Bridge Low Side Driver Rise Time	10% to 90% (Note 5)	$t_{HDRVlo(rise)}$	–	18	–	ns
Half−Bridge Low Side Driver Fall Time	90% to 10% (Note 5)	$t_{HDRVhi(fall)}$	–	9	–	ns
Half−Bridge Low Side Driver High State Voltage	I_{HDRVlo} = −4 mA	$V_{HDRVlo(OH)}$	14	14.7	–	V
Half−Bridge Low Side Driver Low State Voltage	I_{HDRVlo} = 4 mA	$V_{HDRVlo(OL)}$	–	0.06	0.5	V
Half−Bridge Low Side Driver Duty Ratio	10 to 90% to 10% transitions (Note 5)	$D_{HDRVloMAX}$	44	48	50	%
CROSSOVER DEAD TIME						
Delay from HDRVlo high to low to HDRVhi low to high transition	V_{HVS} = 50 V	$t_{HDRVhi(h−l)}$	500	785	950	ns
Delay from HDRVhi high to low to HDRVlo low to high transition	V_{HVS} = 50 V	$t_{HDRVhi(h−l)}$	500	785	950	ns
HALF−BRIDGE DISABLE						
Half−Bridge Disable	V_{OSC} Decreasing	$V_{HB(DIS)}$	1.550	1.955	2.300	V
Half−Bridge Disable Hysteresis	V_{OSC} Increasing	$V_{HB(DIS−HYS)}$	−	130	−	mV

5. Resistor/capacitor parallel combination (39 pF || 20 kΩ) between drive pin and driver supply and between HDRVxx and GND pins.

DETAILED OPERATING DESCRIPTION

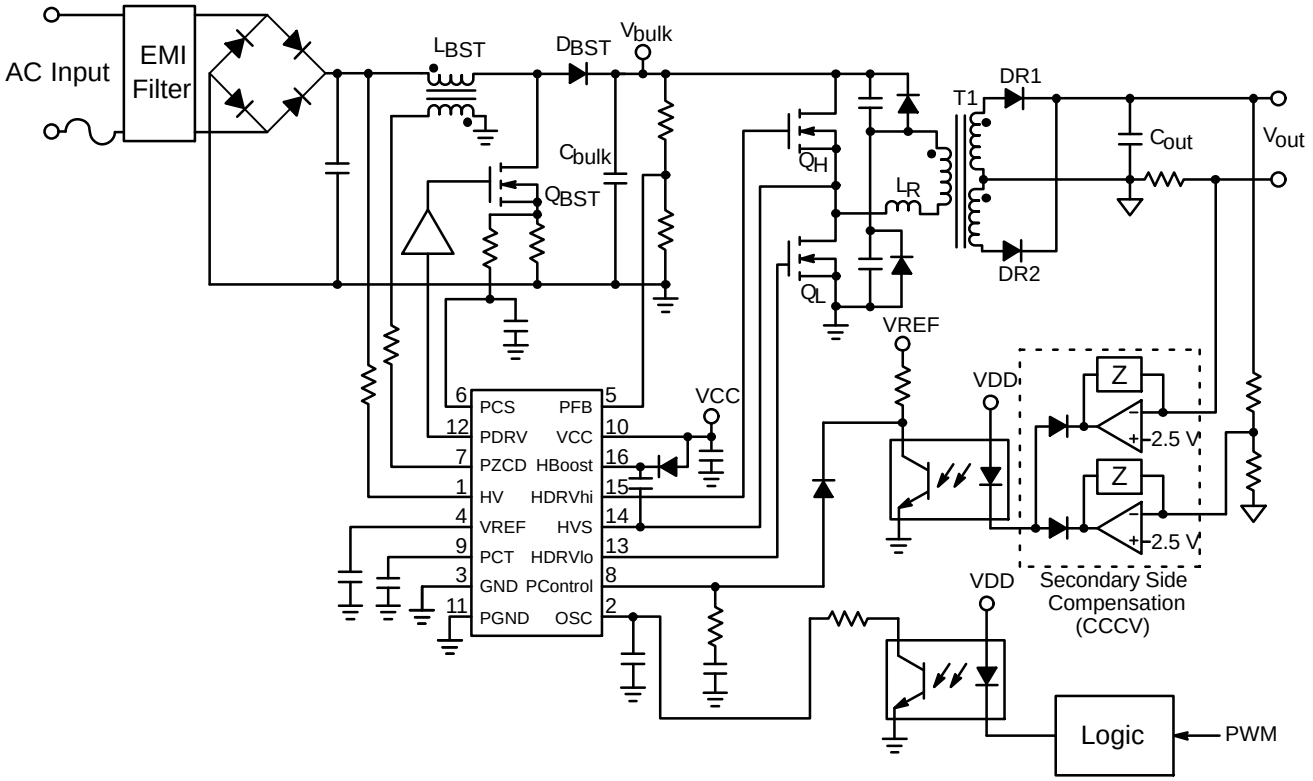


Figure 2. Simplified Application Block Diagram

OVERVIEW

The NCL30051 is a combination of a PFC boost controller and a half−bridge resonant controller optimized for off-line LED lighting solutions. This device integrates all the features needed to implement a highly efficient and small form factor LED driver. It contains a critical conduction mode (CrM) power factor correction (PFC) controller and a half−bridge resonant (HBR) controller with a built−in 600 V driver. The half−bridge stage operates at a fixed frequency − greatly simplifying the control implementation. Output (current or voltage) regulation can be achieved by adjusting the PFC stage output voltage based on a control signal generated external to the NCL30051.

This device includes an enable input on the PFC feedback pin, open feedback loop protection and PFC overvoltage and undervoltage detectors. Other features included in the NCL30051 are a 600 V startup circuit and an adjustable frequency oscillator. The controllers are properly sequenced, simplifying the system design.

THEORY OF OPERATION

The NCL30051 provides an innovative control mechanism compared to traditional two stage power conversion architectures. This unique regulation scheme offers extreme simplicity for certain applications, but at the same time places constraints that have to be taken into account during the converter design.

Traditional 2-stage converters have independent control loops for the PFC stage and the step-down stage, allowing each converter output to be regulated on its own. The PFC stage is often designed for critical conduction (CrM) or continuous conduction mode (CCM) operation and the step-down stage is typically a current-mode/voltage-mode PWM controller geared for forward or flyback applications. More recently, some solutions such as the NCP1910 CCM PFC two stage combo from ON Semiconductor have become available which incorporates the half-bridge resonant converter topology which offers significant efficiency and EMI advantages. However, this HBR topology involves varying the switching frequency to regulate the output and hence adds further complexity to such combination controllers.

In contrast, the NCL30051 simplifies the overall approach significantly by implementing the HBR approach for the second stage converter at a fixed frequency. This simply means that the second-stage converter now operates in a non-regulating fixed-ratio voltage conversion mode. The implication of this approach is that output regulation control has to be provided by adjusting the output of the PFC front-end converter. The benefits of this approach can be summarized as follows:

- Low pin-count of controller combines strong feature set
- Low external component count
- ZVS of the second stage FETs without any tuning requirements
- High efficiency facilitates improved thermal performance
- Low EMI and easy filtering due to fixed frequency
- Facilitation of synchronous rectification control design
- Easier design of magnetic components (esp. Resonant transformer and inductor)

While the above listed benefits make this approach a very interesting proposition for many isolated applications with PFC front-end, it has to be implemented with some additional considerations.

The fact that the output regulation is achieved by adjusting the PFC output voltage, places additional limits on the PFC stage that is not needed in the traditional approach. Depending on the application and output requirements, this may not be much of a constraint. However, if the output variation requirements are significant, the PFC stage may not have enough dynamic range to provide sufficient output power control.

The other consideration is related to the response time to any output variations. In a true 2-stage conversion, the decoupling of the two stages allows a better transient response. In that case the PFC converter is constrained to a bandwidth much below the line frequency (typically < 20 Hz), whereas the second stage can be optimized to have a very fast dynamic response. In the NCL30051 application, the second stage has no independent output regulation ability, so the dynamic response is constrained by the PFC stage bandwidth. This limitation means that the approach is not suited for very fast-transient loads. However, a large number of applications (such as LED drivers and battery chargers) can easily accept the response times offered by the NCL30051 approach.

Output voltage ripple is another consideration when designing with the NCL30051. The low frequency ripple on the PFC output stage is determined by the size of the PFC capacitor. With no compensation in the second stage, the final output voltage ripple is simply a scaled version of the PFC output ripple determined by the fixed ratio of the second stage. Normally this type of ripple is not a concern for lighting applications as the ripple frequency (100/120 Hz) is above the eye response frequency or in the case of fixed output LED power supplies, there are secondary side constant current regulators that further reduces the ripple.

Finally, hold-up time is another matter to be considered when using this fixed-ratio converter approach. When the input voltage droops, the output of the PFC starts dropping at a rate determined by the bulk capacitance value and the load current. The output voltage follows this discharge rate with a fixed ratio. By increasing the bulk capacitance value, this discharge rate can be slowed down increasing hold-up time. However, this approach has practical limits and is not recommended for applications requiring a long hold-up time with no output voltage variation.

Figure 2 illustrates a typical NCL30051 2-stage converter implementation. As seen in the figure, the isolated second stage converter output value is processed by a compensation circuit in the secondary and an error signal is generated and coupled to the primary using an opto-coupler. On the primary side, this signal is fed to the PControl pin of NCL30051 through a reverse ORing diode. The PControl pin also has a default error signal generated by the PFC error amplifier. The lower of these two signals dominates and helps set the fixed ON time for the PFC block as described in earlier sections. In the intended implementation, the NCL30051's PFC error amplifier should be configured to set the maximum value of the output voltage and the secondary side feedback should be allowed to control it lower based on the output conditions.

DESIGN CONSIDERATIONS – POWER STAGE

Given the unique nature of the NCL30051, certain power stage design considerations are applicable (for PFC and second-stage) as below. These design considerations are described for a constant current LED lighting application, but can also apply to constant voltage applications with minor variations.

PFC Output (Vbulk) Voltage Range

The minimum bulk voltage setting is dictated by the requirement that the PFC output voltage be higher than the peak of the input line voltage at all times. Even though many lighting applications operate from a single voltage range which simplifies the analysis, we will consider an input range of 85-265 Vac which covers most regional requirements, this means the minimum bulk voltage is set in the range of 385-400 Vdc. However, if the circuit has to handle 277 Vac ±10% input also (as in the case of US commercial lighting applications), the minimum bulk setting goes up to 435 Vdc. The maximum bulk setting is limited by component stress factors and other considerations. The major constraints are bulk capacitor, output (boost) diode, boost FET and the NCL30051 voltage rating.

While other power stage considerations are covered in the paragraphs below, the application of NCL30051 requires that the bulk voltage be limited to below 600 V maximum under all conditions. The NCL30051 high-voltage section is rated at 600 V − this includes pins HV and HVS. The HBoost and HDRVhi pins see the highest potential, given by Vbulk+Vcc. In normal operation the bulk is limited to 540 V based on the derating criteria. This is the same derating which would be applied to the 600 V output rectifier in the PFC stage.

PFC Output Capacitor - Cbulk

The bulk capacitor is one of the most critical components in the PFC design. High value, high voltage capacitors are expensive and take up a large space. In traditional PFC applications, the voltage rating of this capacitor is about 450 V (some designers cut it to 420 V for cost savings), but for 277 Vac lighting applications, 450 V rating is not sufficient. As shown in the table above, if the output voltage is allowed to vary, the bulk voltage can go even higher. Availability of bulk capacitors above 450 V is limited. One solution is to take two capacitors and put them in series. The effective value of two series capacitors is lower, but for low-medium power applications, this should not be a big issue. For 600 V maximum bulk voltage, two 400 V capacitors need to be used, but for 90−135 Vac only applications, lower rated capacitors can be used. When putting capacitors in series, it is required to have a parallel high value resistor pair in order to ensure voltage sharing.

The effective bulk capacitance value also depends on the application requirements. Normal rule of thumb for traditional PFC circuits is to use around 1 μF/W to achieve desired hold-up time and ripple performance. In this approach, due to absence of a regulated second stage, it may be prudent to increase the capacitance value if low ripple or fast transient response is required. Another factor in selecting the capacitor is that it handles high ripple current due to the CrM topology implemented here. The equations for ripple current through the capacitor are derived in ON Semiconductor application note AND8123 and should be used to determine that the selected capacitor can handle the ripple current without overheating or lifetime degradation.

PFC Diode (D_{BST})

The PFC diode provides the rectification function and has to be rated above the peak value of Vbulk. In the CrM operation, with the diode current going to zero every cycle prior to its turn-off, the reverse recovery is not that prominent and an ultrafast diode can be used. In addition, there is little or no overshoot caused by the reverse recovery, so the FET voltage is also well contained. In most cases a 600 V diode is sufficient depending on the derating criteria.

PFC Switch (Q_{BST})

Typically, the PFC switch is a MOSFET rated anywhere from 500 V to 650 V. Better commercial availability of higher voltage rated FETs in recent years has meant that the QBST is not a major constraint in implementation of variable Vbulk approach offered by NCL30051. However, depending on derating guidelines and practices, the 600 V rating of the FET may not be sufficient. In that case, a higher voltage FET is required.

PFC Inductor (L_{BST})

The PFC inductor is designed using the standard CrM design equations. When the output voltage goes up from 390 V to 540 V, there is about 20% increase in value of inductance required. Thus, variation in PFC voltage results in higher boost inductor value and size (and/or higher ripple current when the output voltage is higher).

HBR Converter Design

The half-bridge resonant converter utilizes an LLC resonant circuit to achieve the ZVS of the primary switches and also to reduce the transition losses in the secondary. Additionally, this circuit offers a major benefit wherein the output inductor can be eliminated.

In traditional LLC approaches, when the second stage converter is regulated, the switching frequency of the HBR converter has to be varied to respond to load or line changes. As a result, operation near the resonant frequency is not always guaranteed and the efficiency takes a hit. Also, varying the frequency imposes additional design burden on the designer to ensure that the control circuit is stable and provides desired results over the full load and line range. The feedback design and loop closure is more challenging in this type of converter.

By keeping a constant switching frequency, not only is the control circuit simplified, the magnetics design also becomes easier. The transformer size can be reduced as it is designed for a single frequency and full optimization is available. Studies have shown that this approach leads to about 25-40% reduction in total magnetics area-product. Other design considerations for the LLC resonant converter remain the same as given in ON Semiconductor application note AND8311 and are not repeated here.

The power conversion architecture of the NCL30051 is ideal for many LED Lighting applications since it provides higher efficiency and power factor correction. Since hold-up time and output ripple are not major considerations in these applications, NCL30051 fits in very well. This means that it is ideal for fixed output voltage LED power supplies (ex: 24 Vdc and 48 Vdc) as well as constant current schemes where the output voltage varies depending on the number of LEDs and the variation of the LED forward voltage. This topology is best suited for applications where the output voltage variation is constrained to a ratio of about 1.5 for designs that require operation at 230 Vac.

Supply Sequencing

The error amplifier of the PFC controller is enabled once V_{CC} reaches $V_{CC(on)}$ and the PFB voltage exceeds $V_{PUVP(high)}$, typically 290 mV. Once enabled, the PControl voltage starts rising and when it exceeds $V_{EA(OL)}$ and V_{CC} is above $V_{CC(enable)}$, the first PFC drive pulse is generated. The half-bridge driver is enabled after the first PFC drive pulse is generated. This ensures a monotonic output voltage rise as the input voltage to the half bridge stage is regulated.

In the event that V_{CC} falls below $V_{CC(enable)}$ before the control voltage exceeds $V_{EA(OL)}$, the error amplifier will remain on and V_{CC} will fall to $Vcc_{(OFF)}$ at which time the HV startup circuit will be enabled and a new startup sequence will be initiated.

High Voltage Startup Circuit

The NCL30051 internal startup regulator eliminates the need for external startup components. In addition, this regulator increases the efficiency of the supply as it uses no power when in the normal mode of operation, but instead uses power supplied by an auxiliary winding. The startup regulator consists of a constant current source that supplies current from the high voltage line (V_{in}) to the supply capacitor on the V_{CC} pin (C_{CC}). The startup current (I_{start}) is typically 7.5 mA. The startup circuit is rated at a maximum voltage of 600 V.

Once C_{CC} is charged to 15.3 V ($V_{CC(on)}$), the startup regulator is disabled and the PFC controller is enabled if the PFB voltage exceeds $V_{PUVP(high)}$. The startup regulator remains disabled until the lower supply threshold, $V_{CC(off)}$, (typically 9.3 V) is reached. Once reached, the drive outputs are disabled and the startup current source is enabled. Once the outputs are disabled, the bias current of the NCL30051 is reduced, allowing V_{CC} to charge back up.

The supply capacitor provides power to the controller while operating in the power up or self−bias mode. During the converter power up, C_{CC} must be sized such that a V_{CC} voltage greater than $V_{CC(off)}$ is maintained while the auxiliary supply voltage is building up. Otherwise, V_{CC} will collapse and the controller will turn off. The IC bias current and gate charge load at the drive outputs must be considered to correctly size C_{CC}. The increase in current consumption due to external gate charge is calculated using Equation 1.

$$I_{CC(gate\ charge)} = f \cdot Q_G \qquad \text{(eq. 1)}$$

where, f is the operating frequency and Q_G is the gate charge of the external MOSFETs.

Main Oscillator

The oscillator frequency is set by the oscillator capacitor, C_{OSC}, on the OSC pin. The oscillator operates at a fixed 80% duty ratio. A current source charges C_{OSC} to its peak voltage, typically 5 V. Once the peak voltage is reached, the charge current is disabled and C_{OSC} is discharged down to 3 V by another current source. The charge and discharge currents are typically 173 and 692 μA, respectively. The oscillator frequency vs oscillator capacitance graph is shown in Figure 3.

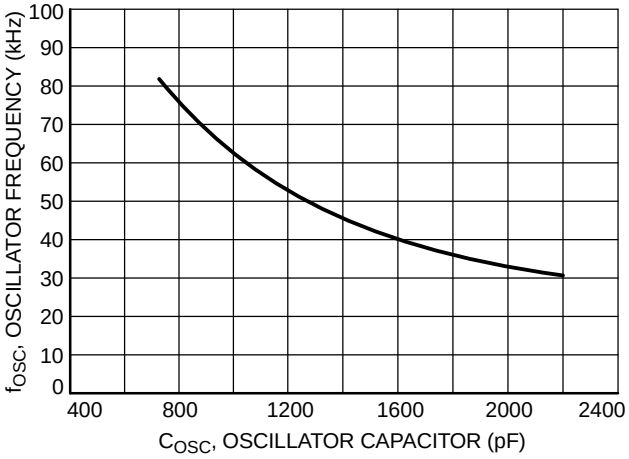


Figure 3. Oscillator Frequency vs. Oscillator Capacitor

An internal clock signal is generated by dividing the oscillator frequency by two. This clock signal is used to control the half−bridge driver. The half−bridge duty ratio is limited to 50%. The PFC is not synchronized to the oscillator as it operates in variable frequency mode.

Half−Bridge Disable

The half−bridge oscillator and the half−bridge low and high side drivers are disabled once the voltage on the OSC pin is brought below the half−bridge disable threshold, $V_{HB(DIS)}$ (typically 1.955 V). This can be accomplished by pulling down on the oscillator pin using a transistor or open collector/drain device. Once the oscillator pin is released the oscillator capacitor returns to its normal operating range and the half bridge is re−enabled. The low side half−bridge driver generates the first drive pulse during initial power up or re−starting of the half−bridge. This ensures boost voltage is generated to supply the high side driver.

Voltage Reference

The internal voltage reference, V_{REF}, is brought out of the controller to ease compensation requirements. The reference voltage is typically 7.0 V. A 0.1 μF bypass capacitor is required for stability. The reference should not be loaded with external circuitry.

PFC Regulator

The PFC inductor current, $I_{L(t)}$, reaches zero at the end of the switch cycle as shown in Figure 4 and the average input current, $I_{in(t)}$, is in phase with the ac line voltage, $V_{in(t)}$.

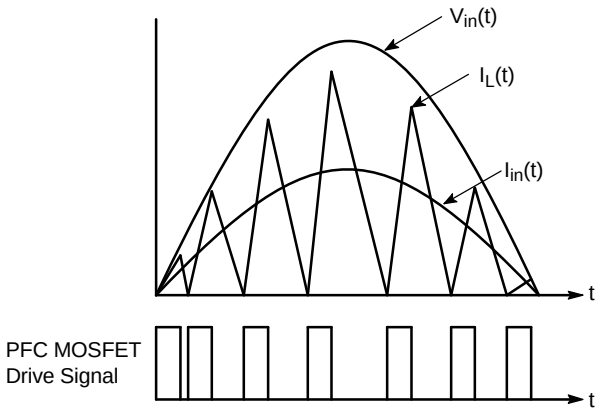


Figure 4. Inductor Current in CrM

High power factor is achieved in CrM by maintaining a constant on time (t_{on}) for a given RMS input voltage ($V_{ac(RMS)}$) and load conditions. Equation 2 shows the relationship between on time and system operating conditions.

$$t_{on} = \frac{2 \cdot P_{out} \cdot L}{\eta \cdot V_{ac(RMS)}^{2}} \qquad \text{(eq. 2)}$$

where, P_{out} is the output power, L is the PFC inductor inductance and η is the system efficiency.

On Time Control

The NCL30051 controls the on time by charging an external timing capacitor on the PCT pin, C_T, with a constant current source, $I_{PCT(C)}$. The C_T ramp is then compared to the control voltage, $V_{PControl}$. The control voltage is constant for a given RMS line voltage and output load, satisfying Equation 2. The block diagram of the constant on time section is shown in Figure 5.

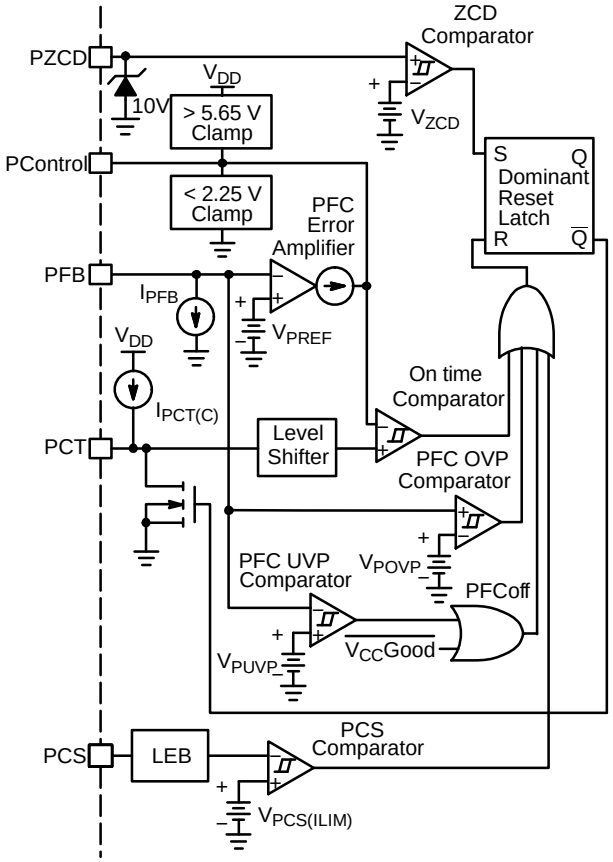


Figure 5. Constant On Time Control Block Diagram

The PControl voltage is internally clamped between 2.25 V and 5.65 V. A voltage offset, $V_{PCT(offset)}$, is added to the C_T ramp to account for the control voltage range. This allows the PFC stage to stop the drive pulses (0% duty ratio) and regulate at light loads. The delta between the PControl voltage needed to generate a PDRV pulse and the minimum PControl Clamp voltage is $V_{PCT(offset)}$.

The timing capacitor is discharged and held low once the C_T ramp voltage plus offset reaches $V_{PControl}$. The PFC drive pulse terminates once the C_T voltage reaches its peak voltage threshold, $V_{PCT(peak)}$. A new cycle starts once the inductor current reaches zero detected by a transition on the ZCD pin or the maximum off time has been reached.

The timing capacitor is sized such that the C_T ramp peak voltage is reached at low line and full load. In this operating mode $V_{PControl}$ is at its maximum. Equation 3 is used to calculate the on time for a given C_T.

$$t_{on(MAX)} = \frac{C_T \cdot V_{PCT(peak)}}{I_{PCT(C)}} \qquad \text{(eq. 3)}$$

Substituting t_{on} in Equation 2 with Equation 3 and rearranging Equation 4 provides a maximum value for C_T.

$$C_T \geq \frac{2 \cdot P_{out} \cdot L \cdot I_{PCT(C)}}{\eta \cdot V_{ac(RMS)}^{2} \cdot V_{PCT(peak)}} \qquad \text{(eq. 4)}$$

where, $V_{PCT(peak)}$, is the maximum PCT voltage, typically 3.0 V.

PFC Startup

The output of the error amplifier is pulled low with an internal pull down transistor when the supply voltage has not reached $V_{CC(on)}$ or if there is a PFC undervoltage fault. This ensures a soft−start sequence once the PFC is enabled and eliminates output voltage overshoot during on/off tests. Once the error amplifier is enabled the output of the error amplifier charges quickly to the minimum clamp voltage.

Off Time Control

The PFC off time varies with the instantaneous line voltage and it is adjusted every cycle to allow the inductor current to reach zero before the next switch cycle begins. The inductor is demagnetized once its current reaches zero. Once the inductor is demagnetized the drain voltage of the PFC switch begins to drop. The inductor demagnetization is detected by sensing the voltage across the inductor using an auxiliary winding. This winding is commonly known as a zero crossing detector (ZCD) winding. This winding provides a scaled version of the inductor voltage. Figure 6 shows the ZCD winding arrangement.

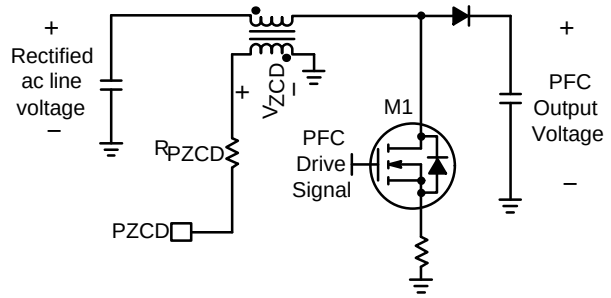


Figure 6. ZCD Winding Implementation

A negative voltage appears on the ZCD winding while the PFC switch is on. The PZCD voltage is positive while the PFC switch is off and current is flowing through the inductor. The PZCD voltage drops to and rings around zero volts once the inductor is demagnetized. Once a negative transition is detected in the PZCD pin the next switch cycle commences. A positive transition (corresponding to the PFC switch turn off) arms the ZCD detector to prevent false triggering. The arming of the ZCD detector is typically 2.1 V (V_{PZCD} increasing) and the triggering is typically 1.5 V (V_{PZCD} decreasing).

The PZCD pin is internally clamped to 10 V with a zener diode. A resistor in series with the ZCD pin is required to limit the current into the PZCD pin. The zener diode prevents the voltage from exceeding the 10 V clamp or going below ground. Figure 7 shows typical ZCD waveforms.

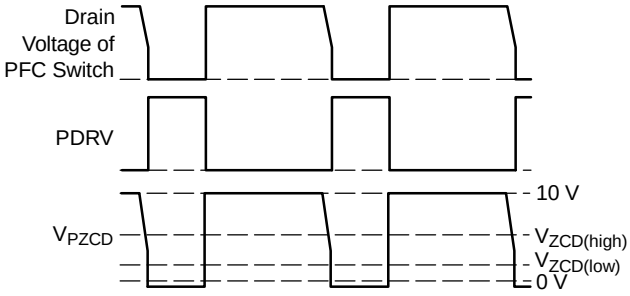


Figure 7. ZCD Winding Waveforms

During startup there are no ZCD transitions to enable the PFC switch. A watchdog timer enables the PFC controller if no switch pulses are detected for a period of 180 μs (typical). The watchdog timer is also useful while operating at light load because the amplitude of the ZCD signal may be very small to cross the ZCD thresholds. The watchdog timer is reset at the beginning of a PFC drive pulse and in a PFC undervoltage fault.

The watchdog timer is disabled if the voltage on the PZCD pin is above $V_{ZCD(high)}$. It is re−enabled once the voltage on the PZCD pin drops below $V_{ZCD(low)}$. Disabling the watchdog timer allows the PFC to be disabled by pulling up on the PZCD pin. Care should be taken to limit the current into the PZCD pin to prevent exceeding the internal 10 V zener clamp.

PFC Compensation

A transconductance error amplifier regulates the PFC output voltage, Vbulk, by comparing the PFC feedback signal to an internal 2.5 V reference. As shown in Figure 8 a resistor divider from the PFC output voltage consisting of R1 and R2 generates the PFC feedback signal.

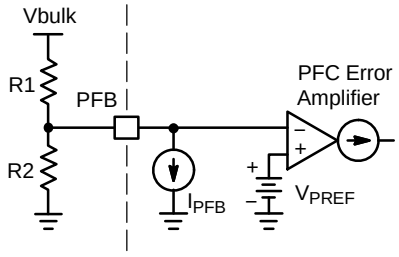


Figure 8. PFC Voltage Sensing

The feedback signal is applied to the amplifier inverting input. The internal 2.5 V reference, V_{PREF}, is applied to the amplifier non−inverting input. The reference is trimmed during manufacturing to achieve an accuracy of ±3.2%. Figure 8 shows the PFC error amplifier and sensing network. Equation 5 is used to calculate the values of the PFC feedback network.

$$V_{PFC} = V_{PREF} \cdot \frac{R_1 + R_2}{R_2} + I_{PFB} \cdot R_1 \quad \text{(eq. 5)}$$

A transconductance amplifier has a voltage−to−current gain, gm. That is, the output current is controlled by the differential input voltage. The NCL30051 amplifier has a typical gm of 95 μS. The PControl pin provides access to the amplifier output for compensation. The compensation network is ground referenced allowing the PFC feedback signal to be used to detect an overvoltage condition.

The compensation network on the PControl pin is selected to filter the bulk voltage ripple such that a constant control voltage is maintained across the ac line cycle. A capacitor between the PControl pin and ground sets a pole. A pole at or below 20 Hz is enough to filter the ripple voltage for a 50 and 60 Hz system. The low frequency pole, f_p, of the system is calculated using Equation 6.

$$f_p = \frac{gm}{2\pi C_{PControl}} \quad \text{(eq. 6)}$$

where, $C_{PControl}$ is the capacitor on the PControl pin to ground.

A key feature to using a transconductance type amplifier, is that the input is allowed to move independently with respect to the output, since the compensation capacitor is connected to ground. This allows dual usage of the feedback pin by the error amplifier and by the overvoltage comparator.

PFC Undervoltage

The NCL30051 safely disables the controller if the PFB pin is left open. An undervoltage detector disables the controller if the voltage on the PFB pin is below $V_{PUVP(low)}$, typically 0.23 V. A 1.2 μA (typical) pull down current source, I_{PFB}, ensures V_{PFB} falls below $V_{PUVP(low)}$ if the PFB pin is floating. The PFB pull down current source affects the PFC output voltage regulation setpoint.

PFC Overvoltage

An overvoltage detector monitors the PFC feedback voltage and disables the PFC driver if an overvoltage condition is detected. This is set internal to the IC at 5% above the nominal setting of the PFC voltage If an OVP event is detected, drive pulses are suppressed until the over voltage condition is removed. The overvoltage detector tolerance is better than ±2%. The overvoltage detector threshold, V_{POVP}, is the midpoint between the PFC driver disable and enable thresholds. The overvoltage comparator hysteresis is the voltage difference between the disable and enable thresholds. An overvoltage condition is detected once V_{PFB} exceeds V_{POVP} by half of $V_{POVP(HYS)}$. The controller is re-enabled once V_{PFB} drops below V_{POVP} by half of $V_{POVP(HYS)}$.

PFC Overcurrent

The PFC current is monitored by means of an overcurrent detector. The PCS pin provides access to the overcurrent detector. The PFC drive pulse is terminated if the voltage on the PCS pin exceeds the overcurrent threshold, $V_{PCS(ILIM)}$. This comparison is done on a cycle by cycle basis. The overcurrent threshold is typically 0.84 V.

The current sense signal is prone to leading edge spikes caused by the power switch transitions. The NCL30051 has leading edge blanking circuitry that blocks out the first 110 ns (typical) of each current pulse.

PFC Driver

The PFC driver source and sink impedances are typically 60 and 15 Ω, respectively. Depending on the external MOSFET gate charge requirements, an external driver may be needed to drive the PFC power switch. A driver such as the one shown in Figure 9 can be easily implemented using small bipolar transistors.

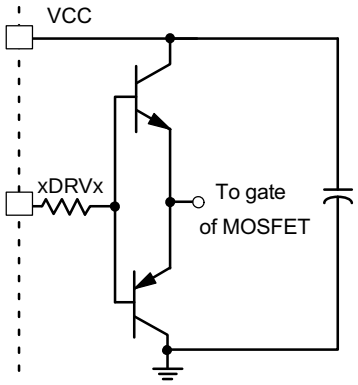


Figure 9. External Driver

Half−Bridge Driver

The half−bridge stage operates at a fixed 50% duty ratio. The oscillator frequency is divided by two before it is applied to the half−bridge controller.

The half−bridge controller has a low side driver, HDRVlo, and a 600 V high side driver, HDRVhi. The built in high voltage driver eliminates the need for an external transformer or dedicated driver. A built−in delay between each drive transition eliminates the risk of cross conduction. The delay is typically 785 ns. The typical duty ratio of each half−bridge driver is 48%.

The high side driver is connected between the HBoost and the HVS pins as shown in Figure 10.

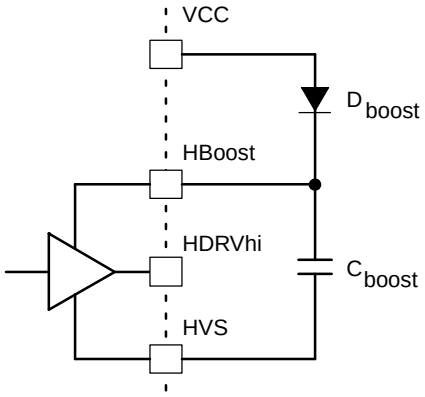


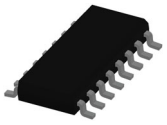
Figure 10. Half−bridge High Side Driver

A boost circuit comprised of D_{boost} and C_{boost} generates the supply voltage for the high side driver. Once HDRVlo turns on, the HVS pin is effectively grounded through the external power switch. This allows C_{boost} to charge to V_{CC}. Once HDRVlo turns off, HVS floats high and D_{boost} is reversed biased. An undervoltage detector monitors the HBoost voltage. Once the HBoost voltage is greater than $V_{Boost(UV)}$, typically, 6.1 V, the high side driver is enabled. The low side driver generally starts before the high side driver because the boost voltage is generated by the low side driver switch transitions.

The half−bridge low side driver source and sink impedances are typically 75 and 15 Ω, respectively. The half−bridge high side driver source and sink impedances are typically 75 and 15 Ω, respectively. Depending on the external MOSFETs gate charge requirements, an external driver may be needed to drive the low and high side power switches.

Analog and Power Ground

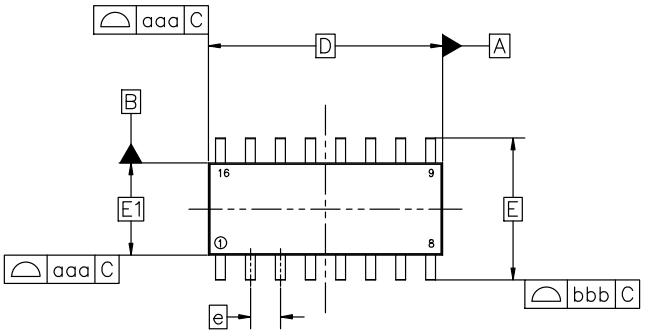
The NCL30051 has an analog ground, GND, and a power ground, PGND, terminal. GND is used for analog connections such as VREF and OSC. PGND is used for high current connections such as the gate drivers. It is recommended to have independent analog and power ground planes and connect them at a single point, preferably at the ground terminal of the system. This will prevent high current flowing on PGND from injecting noise in GND. The PGND connection should be as short and wide as possible to reduce inductance−induced spikes.



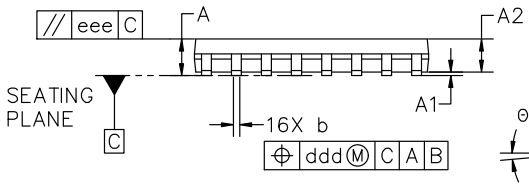
SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

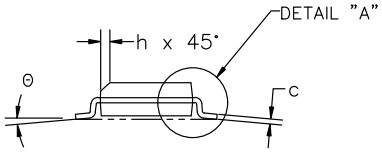
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



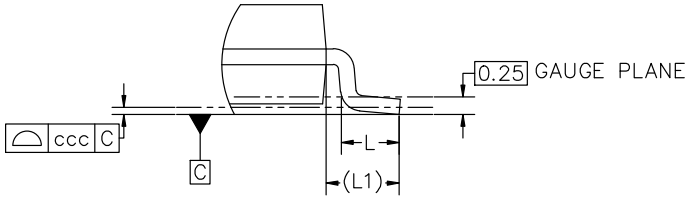
TOP VIEW



SIDE VIEW

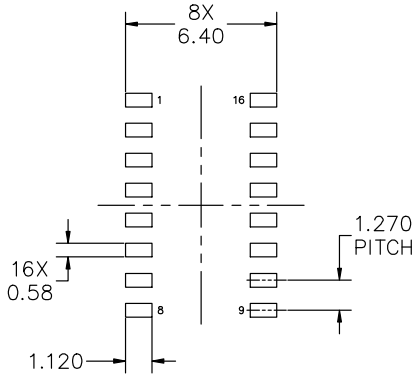


END VIEW



DETAIL "A"
Scale 3:1

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
Θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

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DESCRIPTION:	**SOIC−16 9.90X3.90X1.37 1.27P**		**PAGE 1 OF 2**

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CASE 751B
ISSUE M

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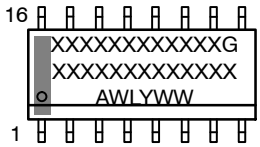
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

PIN	
1.	COLLECTOR
2.	BASE
3.	EMITTER
4.	NO CONNECTION
5.	EMITTER
6.	BASE
7.	COLLECTOR
8.	COLLECTOR
9.	BASE
10.	EMITTER
11.	NO CONNECTION
12.	EMITTER
13.	BASE
14.	COLLECTOR
15.	EMITTER
16.	COLLECTOR

STYLE 2:

PIN	
1.	CATHODE
2.	ANODE
3.	NO CONNECTION
4.	CATHODE
5.	CATHODE
6.	NO CONNECTION
7.	ANODE
8.	CATHODE
9.	CATHODE
10.	ANODE
11.	NO CONNECTION
12.	CATHODE
13.	CATHODE
14.	NO CONNECTION
15.	ANODE
16.	CATHODE

STYLE 3:

PIN	
1.	COLLECTOR, DYE #1
2.	BASE, #1
3.	EMITTER, #1
4.	COLLECTOR, #1
5.	COLLECTOR, #2
6.	BASE, #2
7.	EMITTER, #2
8.	COLLECTOR, #2
9.	COLLECTOR, #3
10.	BASE, #3
11.	EMITTER, #3
12.	COLLECTOR, #3
13.	COLLECTOR, #4
14.	BASE, #4
15.	EMITTER, #4
16.	COLLECTOR, #4

STYLE 4:

PIN	
1.	COLLECTOR, DYE #1
2.	COLLECTOR, #1
3.	COLLECTOR, #2
4.	COLLECTOR, #2
5.	COLLECTOR, #3
6.	COLLECTOR, #3
7.	COLLECTOR, #4
8.	COLLECTOR, #4
9.	BASE, #4
10.	EMITTER, #4
11.	BASE, #3
12.	EMITTER, #3
13.	BASE, #2
14.	EMITTER, #2
15.	BASE, #1
16.	EMITTER, #1

STYLE 5:

PIN	
1.	DRAIN, DYE #1
2.	DRAIN, #1
3.	DRAIN, #2
4.	DRAIN, #2
5.	DRAIN, #3
6.	DRAIN, #3
7.	DRAIN, #4
8.	DRAIN, #4
9.	GATE, #4
10.	SOURCE, #4
11.	GATE, #3
12.	SOURCE, #3
13.	GATE, #2
14.	SOURCE, #2
15.	GATE, #1
16.	SOURCE, #1

STYLE 6:

PIN	
1.	CATHODE
2.	CATHODE
3.	CATHODE
4.	CATHODE
5.	CATHODE
6.	CATHODE
7.	CATHODE
8.	CATHODE
9.	ANODE
10.	ANODE
11.	ANODE
12.	ANODE
13.	ANODE
14.	ANODE
15.	ANODE
16.	ANODE

STYLE 7:

PIN	
1.	SOURCE N-CH
2.	COMMON DRAIN (OUTPUT)
3.	COMMON DRAIN (OUTPUT)
4.	GATE P-CH
5.	COMMON DRAIN (OUTPUT)
6.	COMMON DRAIN (OUTPUT)
7.	COMMON DRAIN (OUTPUT)
8.	SOURCE P-CH
9.	SOURCE P-CH
10.	COMMON DRAIN (OUTPUT)
11.	COMMON DRAIN (OUTPUT)
12.	COMMON DRAIN (OUTPUT)
13.	GATE N-CH
14.	COMMON DRAIN (OUTPUT)
15.	COMMON DRAIN (OUTPUT)
16.	SOURCE N-CH

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

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