Field Stop Trench IGBT Die with Sinterable Top Metal

750 V, 225 A

NCG225L75NF8M1

ON Semiconductor®

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V_{CES} = 750 V
I_C = Limited by $T_{j(max)}$

Features

- AEC−Q101 Qualified and PPAP Capable
- Maximum Junction Temperature 175°C
- Advanced FS4 Trench Technology
- Positive Temperature Coefficient
- Easy Paralleling
- Short Circuit Rated
- Very Low Saturation Voltage:
  $V_{CE(SAT)}$ = 1.45 V (Typ.) @ I_C = 225 A
- Optimized for Motor Control Applications
- Emitter Pad Covered with Sinterable Metal Layer

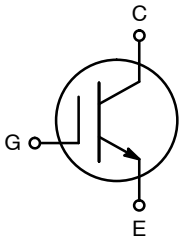
Applications

- Automotive Traction Modules
- General Power Modules

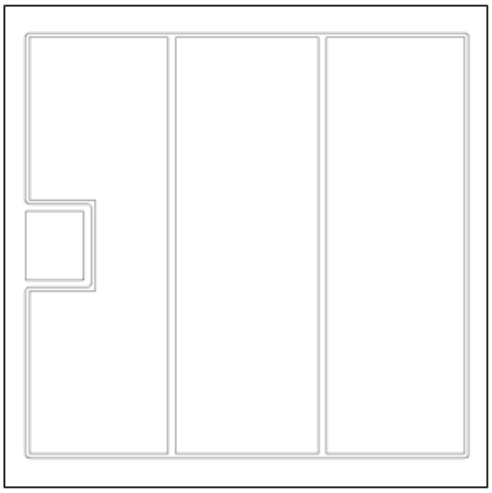
MECHANICAL PARAMETERS

Parameter	Mils	μm
Die Size	394 × 394	10,000 × 10,000
Emitter Pad Size	See chip drawing	See chip drawing
Gate Pad Size	47 × 56	1,200 × 1,430
Scribe Lane Width	3.14	80
Die Thickness	3.4	88
Top Metal	5 μm AlSiCu + 0.95 μm Ti/NiV/Ag (STM)	
Back Metal	0.85 μm Al/NiV/Ag	
Topside Passivation	Silicon Nitride plus Polyimide	
Wafer Diameter	200 mm	
Max Possible Die Per Wafer	226	
Recommended Storage Environment	In original container, in dry nitrogen, < 3 months at an ambient temperature of 23°C	

IGBT DIE



DIODE OUTLINE



ORDERING INFORMATION

Device	Inking?	Shipping
NCG225L75NF8M1	Yes	Sawn Wafer on Tape

ABSOLUTE MAXIMUM RATINGS (T_{VJ} = 25°C unless otherwise noted)

Parameter	Symbol	Ratings	Unit
Collector−Emitter Voltage	V_{CES}	750	V
Gate−Emitter Voltage	V_{GES}	±20	V
DC Collector Current, Limited by T_{VJ} max	I_C	(Note 1)	A
Pulsed Collector Current, V_{GE} = 15 V, tp Limited by $T_{VJ\ max}$ (Note 2)	I_{CM}	675	A
Short Circuit Withstand Time, V_{GE} = 15 V, $V_{CE} \le$ 400 V, $T_{VJ} \le$ 175°C	t_{sc}	4	μs
Operating Junction Temperature	T_{VJ}	−40 to +175	°C
Storage Temperature Range	Tstg	+18 to +28	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Depends on the thermal properties of assembly.
2. Not subject to production test − verified by design/characterization.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
STATIC CHARACTERISTICS (Tested on Wafers)							
Collector−Emitter Breakdown Voltage	BV_{CES}	V_{GE} = 0 V, I_C = 1 mA		750	–	–	V
Collector−Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 200 A, V_{GE} = 15 V		–	1.30	1.75	V
Gate−Emitter Threshold Voltage	$V_{GE(th)}$	V_{GE} = V_{CE}, I_C = 200 mA		4.8	6.0	7.2	V
Collector Cut−off Current	I_{CES}	V_{CE} = V_{CES}, V_{GE} = 0 V		–	–	40	μA
Gate Leakage Current	I_{GES}	V_{GE} = V_{GES}, V_{CE} = 0 V		–	–	±600	nA
ELECTRICAL CHARACTERISTICS (Not Subjected to Production Test – Verified by Design/Characterization)							
Collector−Emitter Breakdown Voltage	BV_{CES}	V_{GE} = 0V, I_C = 1 mA	T_{VJ} = −40°C	700	810	–	V
Collector Cut−off Current	I_{CES}	V_{CE} = V_{CES}, V_{GE} = 0 V	T_{VJ} = 150°C	–	0.2	–	mA
			T_{VJ} = 175°C	–	1.5	–	mA
Collector−Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 225 A, V_{GE} = 15 V	T_{VJ} = 150°C	–	1.65	–	V
			T_{VJ} = 175°C	–	1.75	–	V
Input Capacitance	C_{IES}	V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz		–	21000	–	pF
Output Capacitance	C_{OES}			–	370	–	pF
Reverse Transfer Capacitance	C_{RES}			–	83	–	pF
Internal Gate Resistance	R_G	f = 1 MHz		–	2.3	–	Ω
Total Gate Charge	$Q_{G(Total)}$	V_{CE} = 400 V, I_C = 225 A, V_{GE} = −8 V to +15 V		–	690	–	nC
Gate−Emitter Charge	Q_{GE}			–	360	–	nC
Gate−Collector Charge	Q_{GC}			–	158	–	nC
Turn−On Delay Time	$t_{d(on)}$	V_{CE} = 400 V, I_C = 225 A, R_G = 2 Ω, V_{GE} = +15/−8 V, Inductive Load, T_{VJ} = 25°C		–	104	–	ns
Rise Time	t_r			–	364	–	ns
Turn−Off Delay Time	$t_{d(off)}$			–	122	–	ns
Fall Time	t_f			–	176	–	ns
Turn−On Delay Time	$t_{d(on)}$	V_{CE} = 400 V, I_C = 225 A, R_G = 2 Ω, V_{GE} = +15/−8 V, Inductive Load, T_{VJ} = 150°C		–	112	–	ns
Rise Time	t_r			–	356	–	ns
Turn−Off Delay Time	$t_{d(off)}$			–	130	–	ns
Fall Time	t_f			–	270	–	ns

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
ELECTRICAL CHARACTERISTICS (Not Subjected to Production Test – Verified by Design/Characterization)						
Turn−On Delay Time	$t_{d(on)}$	V_{CE} = 400 V, I_C = 225 A, R_G = 2 Ω, V_{GE} = +15/−8 V, Inductive Load, T_{VJ} = 175°C	–	112	–	ns
Rise Time	t_r		–	356	–	ns
Turn−Off Delay Time	$t_{d(off)}$		–	136	–	ns
Fall Time	t_f		–	288	–	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Switching characteristics and thermal properties are depending strongly on module design and mounting technology.

For ordering, technique and other information on automotive bare die products from ON Semiconductor, please contact automotivebaredie@onsemi.com

DIE LAYOUT

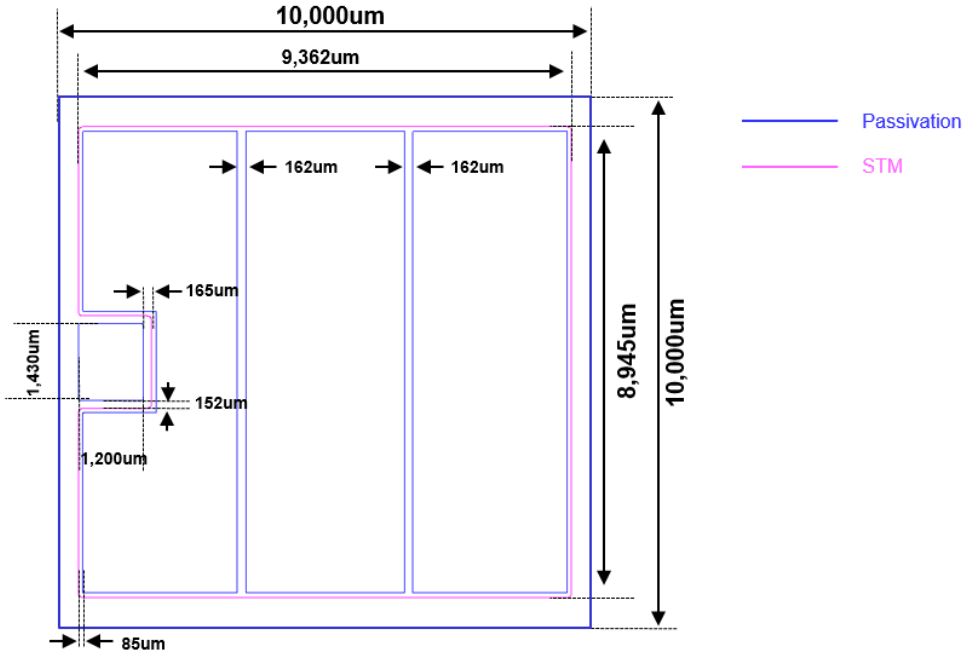


Figure 1. DIE Layout

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
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