

# Isolated High Current IGBT Gate Driver

## Product Preview

### NCD57100, NCD57101, NCV57100, NCV57101

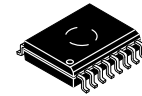
NCx5710y is a high-current single channel IGBT driver with internal galvanic isolation, designed for high system efficiency and reliability in high power applications. Its features include complementary inputs, open drain FAULT and READY outputs, active MILLER CLAMP, accurate UVLOs, DESAT protection and DESAT diagnostic function, soft turn-off at DESAT, Disable output function and separate high and low (OUTH and OUTL) driver outputs (NCx57100) for system design convenience. NCx5710y accommodates both 5 V and 3.3 V signals on the input side and wide bias voltage range on the driver side including negative voltage capability. NCx5710y provides > 5 kVrms (UL1577 rating) galvanic isolation and > 1424 V<sub>PK</sub> (working voltage) capabilities. NCx5710y is available in the wide-body SOIC-16 package with guaranteed 8 mm creepage distance between input and output to fulfill reinforced safety insulation requirements.

#### Features

- High Current Peak Output ( $\pm 7$  A)
- Low Output Impedance for Enhanced IGBT Driving
- Short Propagation Delays with Accurate Matching
- Active Miller Clamp to Prevent Spurious Gate Turn-on
- DESAT Protection with Programmable Delay
- DESAT Diagnostic Function (DSCHK)
- Output Disable Function
- Negative Voltage (Down to  $-8$  V) Capability for DESAT
- Soft Turn Off During IGBT Short Circuit
- IGBT Gate Clamping During Short Circuit
- Tight UVLO Thresholds for Bias Flexibility
- Wide Bias Voltage Range including Negative VEE2
- 3.3 V to 5 V Input Supply Voltage
- Designed for AEC-Q100 Certification
- 5000 V Galvanic Isolation (to meet UL1577 Requirements)
- 1424 V<sub>PK</sub> / 1000 V<sub>RMS</sub> Working Voltage (per VDE0884-11 Requirements)
- High Transient Immunity
- High Electromagnetic Immunity
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

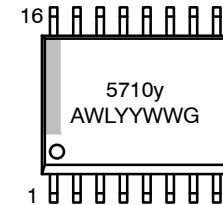
#### Typical Applications

- Automotive Applications
- Motor Control
- Industrial Power Supplies
- Solar Inverters
- Welding
- Uninterruptible Power Supplies (UPS)



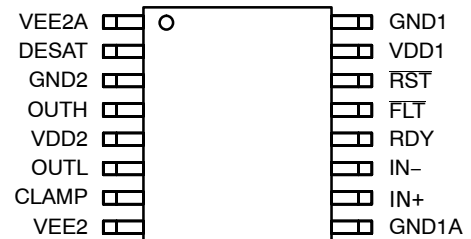
SOIC-16 WB  
CASE 751G-03

#### MARKING DIAGRAM

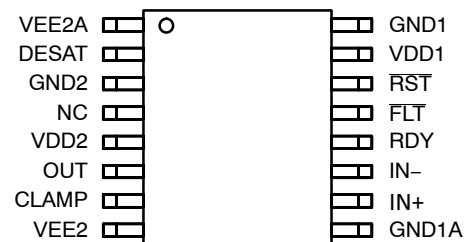


- 5710y = Specific Device Code (y = 0 or 1)  
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

#### PIN ASSIGNMENTS



NCx57100 (x = D or V)



NCx57101 (x = D or V)

#### ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

This document contains information on a product under development. onsemi reserves the right to change or discontinue this product without notice.

NCD57100, NCD57101, NCV57100, NCV57101

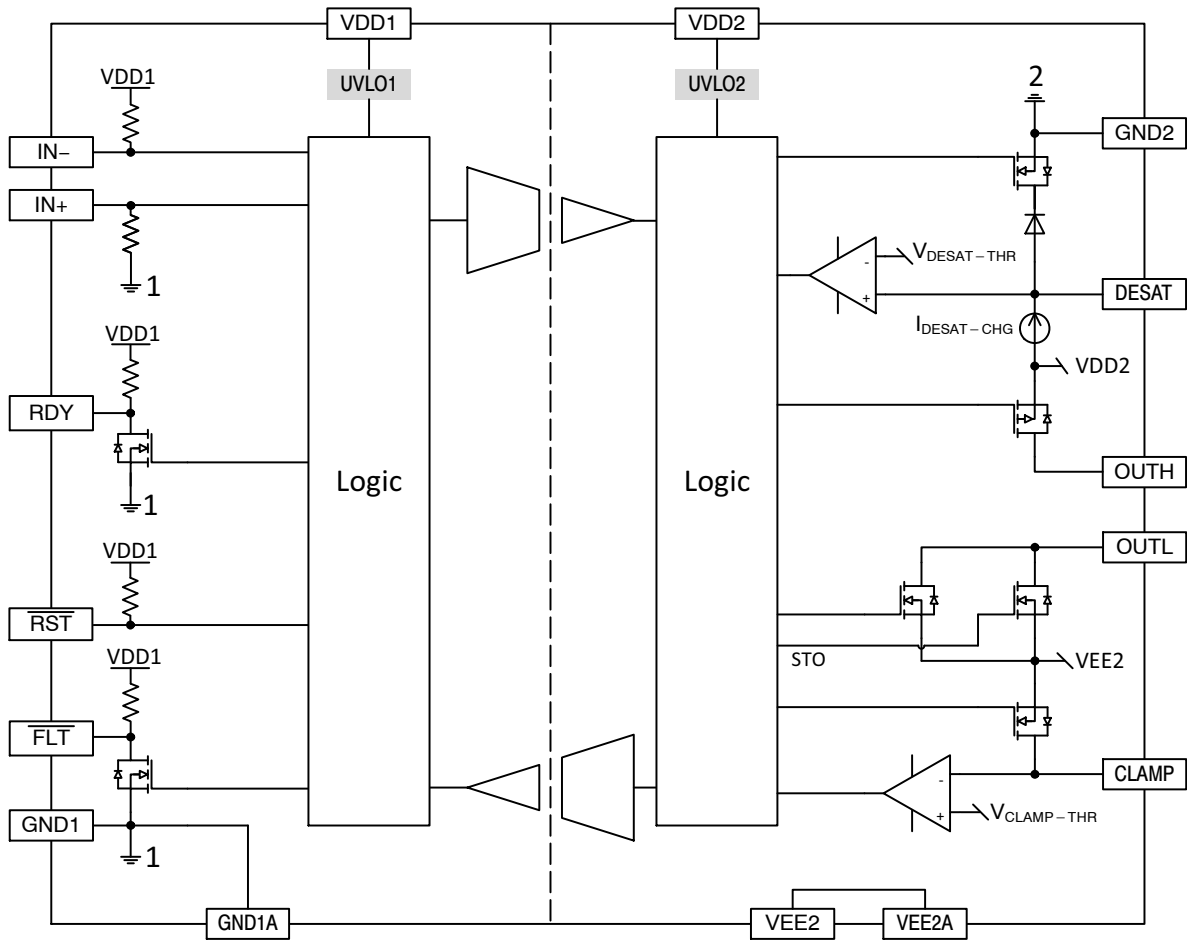


Figure 1. Simplified Block Diagram NCx57100

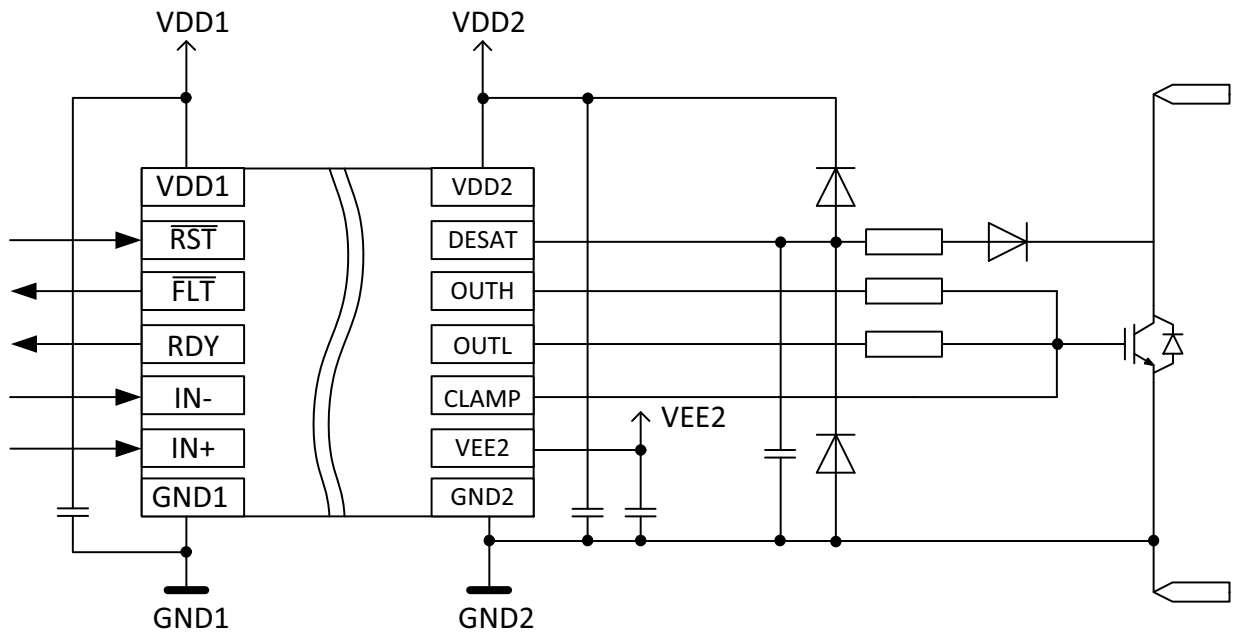


Figure 2. Simplified Application Schematics NCx57100

NCD57100, NCD57101, NCV57100, NCV57101

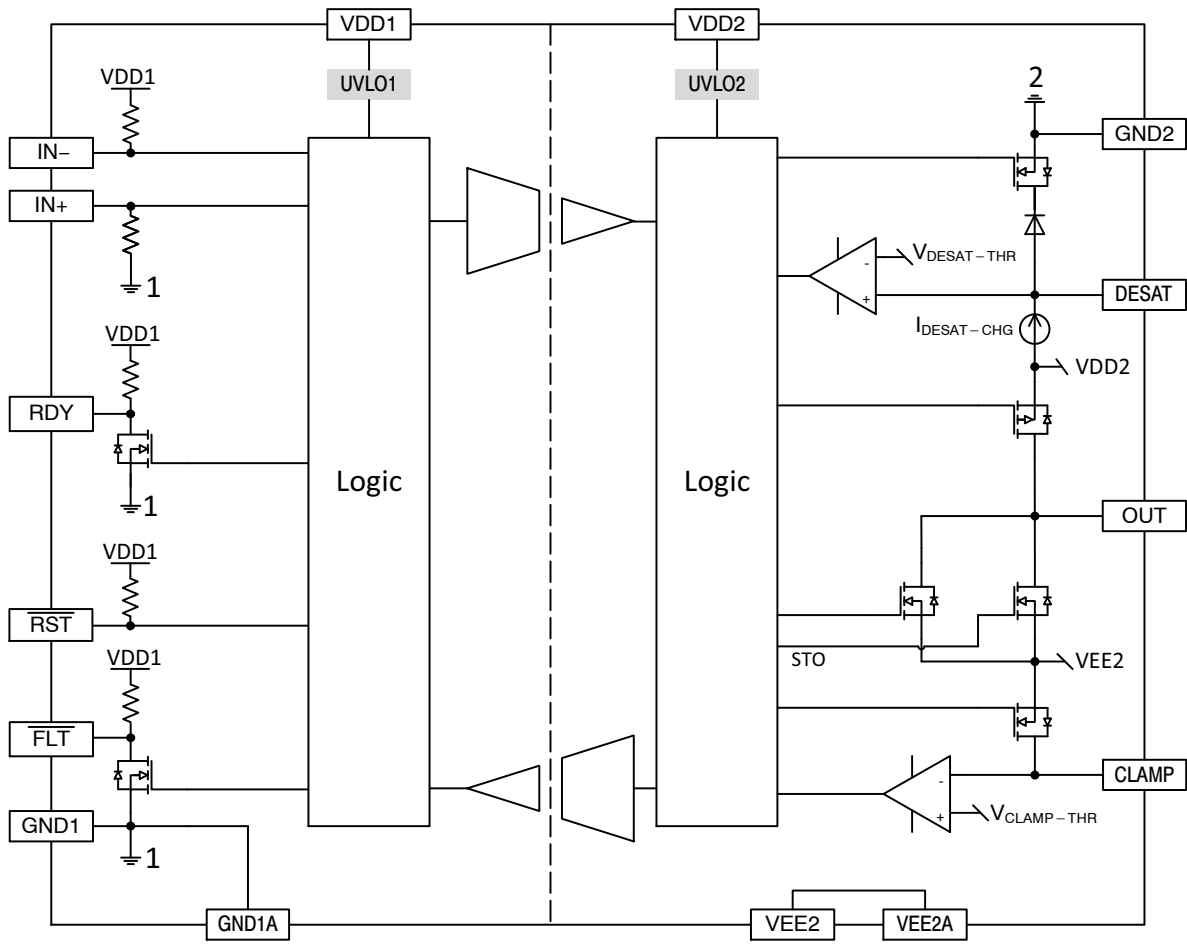


Figure 3. Simplified Block Diagram NCx57101

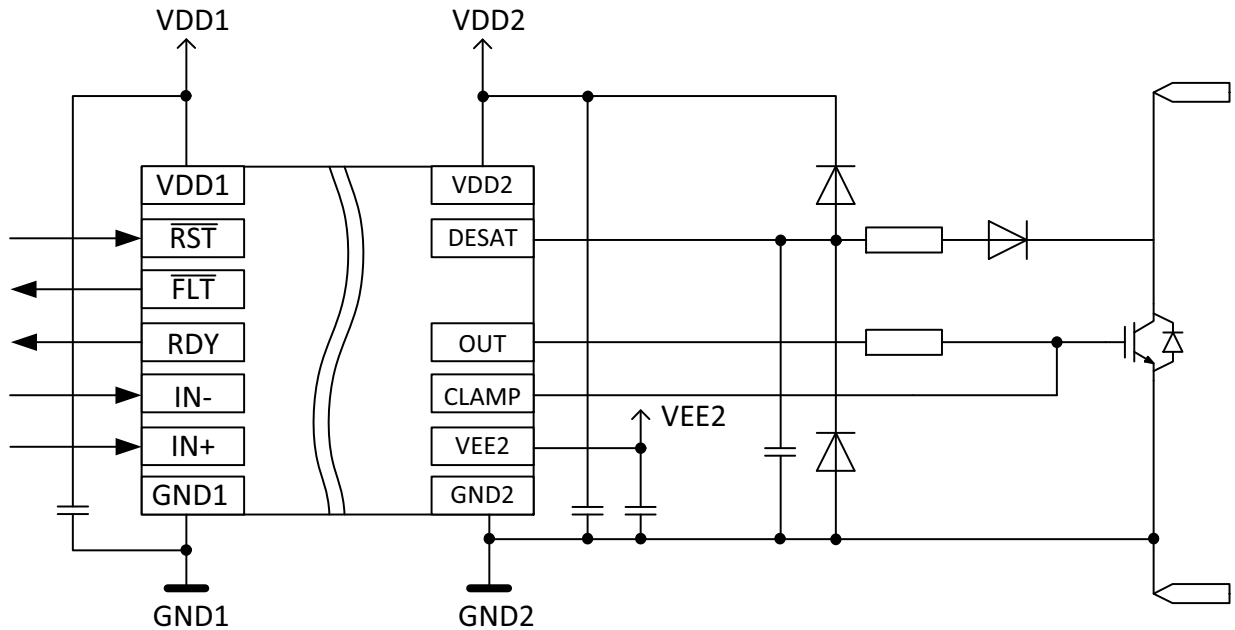


Figure 4. Simplified Application Schematics NCx57101

## NCD57100, NCD57101, NCV57100, NCV57101

### PIN DESCRIPTION

Pin Name	No.	I/O	Description
V <sub>EE2A</sub>	1	Power	Output side negative power supply. A good quality bypassing capacitor is required from these pins to GND2 and should be placed close to the pins for best results. Connect it to GND2 for unipolar supply application. VEE2 and VEE2A pins are internally connected together, for better package cooling of the driver, reduction of interference and negative effects of the floating pins, an external connection is recommended. Thermal cooling polygons should be applied to these pins for better cooling of the case.
V <sub>EE2</sub>	8		
DESAT	2	I/O	Input for detecting the desaturation of IGBT due to a short circuit condition. An internal constant current source I <sub>DESAT-CHG</sub> charging an external capacitor connected to this pin allows a programmable blanking delay every ON cycle before DESAT fault is processed, thus preventing false triggering. When the DESAT voltage goes up and reaches V <sub>DESAT-THR</sub> , the output is driven low. Further, the /FLT output is activated, please refer to Figure 7 on page 13.  A 5 μs mute time applies to IN+ and IN- once DESAT occurs.
GND2	3	Power	Output side gate drive reference connecting to IGBT emitter or FET source.
OUTH (NCx57100)	4	O	Driver high output that provides the appropriate drive voltage and source current to the IGBT/FET gate.
N/C (NCx57101)			Not Connected
V <sub>DD2</sub>	5	Power	Output side positive power supply. The operating range for this pin is from UVLO2 to its maximum allowed value. A good quality bypassing capacitor is required from this pin to GND2 and should be placed close to the pins for best results.
OUTL (NCx57100)	6	O	Driver low output that provides the appropriate drive voltage and sink current to the IGBT/FET gate.
OUT (NCx57101)			Driver low output that provides the appropriate drive voltage and sink current to the IGBT/FET gate.
CLAMP	7	I/O	Provides clamping for the IGBT/FET gate during the off period to protect it from parasitic turn-on. Its internal NFET is turned on when the voltage of this pin falls below V <sub>EE2</sub> + V <sub>CLAMP-THR</sub> . It is to be tied directly to IGBT/FET gate with minimum trace length for best results.
GND1A	9	Power	Input side ground reference. GND1 and GND1A pins are internally connected together, for better package cooling of the driver, reduction of interference and negative effects of the floating pins, an external connection is recommended. Thermal cooling polygons should be applied to these pins for better cooling of the case.
GND1	16		
IN+	10	I	Non inverted gate driver input. It is internally clamped to V <sub>DD1</sub> and has a pull-down resistor of 50 kΩ to ensure that output is low in the absence of an input signal. A minimum positive or negative going pulse-width is required at IN+ before OUTx respond.
IN-	11	I	Inverted gate driver input. It is internally clamped to V <sub>DD1</sub> and has a pull-up resistor of 50 kΩ to ensure that output is low in the absence of an input signal. A minimum positive or negative going pulse-width is required at IN- before OUTx respond.
RDY	12	O	Power good indication output, active high when V <sub>DD1</sub> and V <sub>DD2</sub> are both good. There is an internal 50 kΩ pull-up resistor connected to this pin. Multiple of them from different drivers can be "OR"ed together. OUTx remain low when RDY is low. Short time delays may apply. See Figure 6 on page 12 for details.
/FLT	13	O	Fault output (active low) that allows communication to the main controller that the driver has encountered a desaturation condition and has deactivated the output. There is an internal 50 kΩ pull-up resistor connected to this pin. Multiple of them from different drivers can be "OR"ed together.
/RST	14	I	1) RESET: Reset input with an internal 50 kΩ pull-up resistor, active low to reset fault latch. 2) DISABLE: Active low to disable output function 3) DSCHK: Activation of DESAT comparator check function. The DSCHK is activated after input of 15 pulses with 200 ns Low pulse width and 10 μs High pulse width (see Page 23)
V <sub>DD1</sub>	15	Power	Input side power supply (3.3 V to 5 V).

# NCD57100, NCD57101, NCV57100, NCV57101

## SAFETY AND INSULATION RATINGS

Symbol	Parameter	Value	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1 Rated Mains Voltage	< 150 V <sub>RMS</sub>	I – IV
		< 300 V <sub>RMS</sub>	I – IV
		< 450 V <sub>RMS</sub>	I – IV
		< 600 V <sub>RMS</sub>	I – IV
		< 1000 V <sub>RMS</sub>	I – III
CTI	Comparative Tracking Index (DIN IEC 112/VDE 0303 Part 1)	600	
	Climatic Classification	40/125/21	
	Polution Degree (DIN VDE 0110/1.89)	2	
V <sub>PR</sub>	Input-to-Output Test Voltage, Method B, V <sub>IORM</sub> × 1.875 = V <sub>PR</sub> , 100% Production Test with tm = 1 s, Partial Discharge < 5 pC	2670	V <sub>pk</sub>
V <sub>IORM</sub>	Maximum Repetitive Peak Voltage	1424	V <sub>pk</sub>
V <sub>IOWM</sub>	Maximum Working Voltage	1000	V <sub>RMS</sub>
V <sub>IOTM</sub>	Highest Allowable Over Voltage	8490	V <sub>pk</sub>
E <sub>CR</sub>	External Creepage	8.0	mm
E <sub>CL</sub>	External Clearance	8.0	mm
DTI	Insulation Thickness	17.3	um
T <sub>Case</sub>	Safety Limit Values – Maximum Values in Failure; Case Temperature	150	°C
P <sub>S,INPUT</sub>	Safety Limit Values – Maximum Values in Failure; Input Power	36	mW
P <sub>S,OUTPUT</sub>	Safety Limit Values – Maximum Values in Failure; Output Power	1364	mW
R <sub>IO</sub>	Insulation Resistance at TS, V <sub>IO</sub> = 500 V	10 <sup>9</sup>	Ω

# NCD57100, NCD57101, NCV57100, NCV57101

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted) (Note 1)

Symbol	Parameter	Minimum	Maximum	Unit
$V_{DD1-GND1}$	Supply voltage, input side	-0.3	6	V
$V_{DD2-GND2}$	Positive Power Supply, output side	-0.3	36	V
$V_{EE2-GND2}$	Negative Power Supply, output side	-18	0.3	V
$V_{DD2-VEE2} (V_{MAX2})$	Differential Power Supply, output side	-0.3	36	V
$V_{OUTH}$	Positive gate-driver output voltage	$V_{EE2} - 0.3$	$V_{DD2} + 0.3$	V
$V_{OUTL}$	Negative gate-driver output voltage	$V_{EE2} - 0.3$	$V_{DD2} + 0.3$	V
$I_{PK-SRC}$	Gate-driver output sourcing current (maximum pulse width = 10 $\mu$ s, maximum duty cycle = 0.2%, $V_{DD2} = +15$ V, $V_{EE2} = -8$ V)	-	7.8	A
$I_{PK-SNK}$	Gate-driver output sinking current (maximum pulse width = 10 $\mu$ s, maximum duty cycle = 0.2%, $V_{DD2} = +15$ V, $V_{EE2} = -8$ V)	-	7.1	A
$I_{PK-CLAMP}$	Clamp sinking current (maximum pulse width = 10 $\mu$ s, maximum duty cycle = 0.2%, $V_{CLAMP} = 2.5$ V)	-	2.5	A
$t_{CLP}$	Maximum Short Circuit Clamping Time ( $I_{OUTH\_CLAMP} = 500$ mA)	-	10	$\mu$ s
$V_{LIM-GND1}$	Voltage at IN+, IN-, /RST, /FLT, RDY	-0.3	$V_{DD1} + 0.3$	V
$I_{LIM-GND1}$	Output current of /FLT, RDY	-	10	mA
$V_{DESAT-GND2}$	Desat Voltage (Note 2)	-9	$V_{DD2} + 0.3$	V
$V_{CLAMP-VEE2}$	Clamp Voltage	$V_{EE2} - 0.3$	$V_{DD2} + 0.3$	V
$P_D$	Power Dissipation (Note 3)	-	1400	mW
$T_{J(max)}$	Maximum Junction Temperature	-40	150	$^{\circ}$ C
$T_{STG}$	Storage Temperature Range	-65	150	$^{\circ}$ C
$ESD_{HBM}$	ESD Capability, Human Body Model (Note 4)	-	$\pm 2$	kV
$ESD_{CDM}$	ESD Capability, Charged Device Model (Note 4)	-	$\pm 1.5$	kV
MSL	Moisture Sensitivity Level	-	1	-
$T_{SLD}$	Lead Temperature Soldering Reflow, Pb-Free Versions (Note 5)	-	260	$^{\circ}$ C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. The minimum value is verified by characterization with a single pulse of 1.5 mA for 300  $\mu$ s.
3. The value is estimated for ambient temperature 25 $^{\circ}$ C and junction temperature 150 $^{\circ}$ C, 650 mm<sup>2</sup>, 1 oz copper, 2 surface layers and 2 internal power plane layers. Power dissipation is affected by the PCB design and ambient temperature.
4. This device series incorporates ESD protection and is tested by the following methods:  
 ESD Human Body Model tested per AEC-Q100-002 (EIA/JESD22-A114)  
 ESD Charged Device Model tested per AEC-Q100-011 (EIA/JESD22-C101)  
 Latchup Current Maximum Rating:  $\leq 100$  mA per JEDEC standard: JESD78, 25 $^{\circ}$ C
5. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## THERMAL CHARACTERISTICS

Symbol	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Air	100 mm <sup>2</sup> , 2 oz Copper, 1 Surface Layer	95	$^{\circ}$ C/W
		100 mm <sup>2</sup> , 2 oz Copper, 2 Surface Layers and 2 Internal Power Plane Layers	71	

# NCD57100, NCD57101, NCV57100, NCV57101

## RECOMMENDED OPERATING RANGES (Note 6)

Symbol	Parameter	Min	Max	Unit
V <sub>DD1-GND1</sub>	Supply voltage, input side	UVLO1	5.5	V
V <sub>DD2-GND2</sub>	Positive Power Supply, output side	UVLO2	32	V
V <sub>EE2-GND2</sub>	Negative Power Supply, output side	-16	0	V
V <sub>DD2-V<sub>EE2</sub> (V<sub>MAX2</sub>)</sub>	Differential Power Supply, output side	0	32	V
V <sub>IL</sub>	Low level input voltage at IN+, IN-, /RST	0	0.3 X V <sub>DD1</sub>	V
V <sub>IH</sub>	High level input voltage at IN+, IN-, /RST	0.7 X V <sub>DD1</sub>	V <sub>DD1</sub>	V
dV <sub>ISO</sub> /dt	Common Mode Transient Immunity (Note 10)	150	-	kV/μs
T <sub>A</sub>	Ambient Temperature	-40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

## ISOLATION CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>ISO, input-output</sub>	Input-Output Isolation Voltage	T <sub>A</sub> = 25°C, Relative Humidity < 50%, t = 1.0 minute, I <sub>I-O</sub> < 30 μA, 50 Hz (Note 7, 8, 9)	5000	-	-	V <sub>RMS</sub>
R <sub>ISO</sub>	Isolation Resistance	V <sub>I-O</sub> = 500 V (Note 7)	-	10 <sup>11</sup>	-	Ohm

7. Device is considered a two-terminal device: pins 1 to 8 are shorted together and pins 9 to 16 are shorted together.

8. 5,000 V<sub>RMS</sub> for 1-minute duration is equivalent to 6,000 V<sub>RMS</sub> for 1-second duration.

9. The input-output isolation voltage is a dielectric voltage rating per UL1577. It should not be regarded as an input-output continuous voltage rating. For the continuous working voltage rating, refer to equipment-level safety specification or DIN VDE V 0884-11 Safety and Insulation Ratings Table.

**ELECTRICAL CHARACTERISTICS** (V<sub>DD1</sub> = 5 V, V<sub>DD2</sub> = 15 V, V<sub>EE2</sub> = -8 V. For typical values T<sub>A</sub> = 25°C, for min/max values, T<sub>A</sub> is the operating ambient temperature range that applies, unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
--------	-----------	----------------	-----	-----	-----	------

### VOLTAGE SUPPLY

V <sub>UVLO1-OUT-ON</sub>	UVLO1 Output Enabled		-	-	3.05	V
V <sub>UVLO1-OUT-OFF</sub>	UVLO1 Output Disabled		2.4	-	-	V
V <sub>UVLO1-HYST</sub>	UVLO1 Hysteresis		0.1	0.125	-	V
V <sub>UVLO2-OUT-ON</sub>	UVLO2 Output Enabled		12.7	13	13.3	V
V <sub>UVLO2-OUT-OFF</sub>	UVLO2 Output Disabled		11.7	12	12.3	V
V <sub>UVLO2-HYST</sub>	UVLO2 Hysteresis		0.8	1		V
I <sub>DD1-0</sub>	Input Supply Quiescent Current Output Low	IN+ = Low, IN- = Low RDY = High, /FLT = High	-	1	2	mA
I <sub>DD1-100</sub>	Input Supply Quiescent Current Output High	IN+ = High, IN- = Low RDY = High, /FLT = High	-	6	7.5	mA
I <sub>DD2-0</sub>	Output Positive Supply Quiescent Current, Output Low	IN+ = Low, IN- = Low RDY = High, /FLT = High, no load	-	3.3	4	mA
I <sub>DD2-100</sub>	Output Positive Supply Quiescent Current, Output High	IN+ = High, IN- = Low RDY = High, /FLT = High, no load	-	3.6	4	mA
I <sub>EE2-0</sub>	Output Negative Supply Quiescent Current, Output Low	IN+ = Low, IN- = High, no load	-	0.2	2	mA
I <sub>EE2-100</sub>	Output Negative Supply Quiescent Current, Output High	IN+ = High, IN- = Low, no load	-	0.2	2	mA

### LOGIC INPUT AND OUTPUT

V <sub>IL</sub>	IN+, IN-, /RST Low Input Voltage		-	-	0.3 x V <sub>DD1</sub>	V
-----------------	----------------------------------	--	---	---	------------------------	---

# NCD57100, NCD57101, NCV57100, NCV57101

**ELECTRICAL CHARACTERISTICS** ( $V_{DD1} = 5\text{ V}$ ,  $V_{DD2} = 15\text{ V}$ ,  $V_{EE2} = -8\text{ V}$ . For typical values  $T_A = 25^\circ\text{C}$ , for min/max values,  $T_A$  is the operating ambient temperature range that applies, unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
$V_{IH}$	IN+, IN-, /RST High Input Voltage		$0.7 \times V_{DD1}$	-	-	V
$V_{IN-HYST}$	Input Hysteresis Voltage		-	$0.15 \times V_{DD1}$	-	V
$I_{IN-L}$ , $I_{RST-L}$	IN-, /RST Input Current (50 k $\Omega$ pull-up resistor)	$V_{IN-}$ , $V_{RST} = 0\text{ V}$	-	-100	-	$\mu\text{A}$
$I_{IN+H}$	IN+ Input Current (50 k $\Omega$ pull-down resistor)	$V_{IN+} = 5\text{ V}$	-	100	-	$\mu\text{A}$
$I_{RDY-L}$ , $I_{FLT-L}$	RDY, /FLT Pull-up Current (50 k $\Omega$ pull-up resistor)	$V_{RDY}$ , $V_{FLT} = \text{Low}$	-	100	-	$\mu\text{A}$
$V_{RDY-L}$ , $V_{FLT-L}$	RDY, /FLT Low Level Output Voltage	$I_{RDY}$ , $I_{FLT} = 5\text{ mA}$	-	-	0.3	V
$t_{MIN1}$	Input Pulse Width of IN+, IN-, /RST for No Response at Output		-	-	10	ns
$t_{MIN2}$	Input Pulse Width of IN+, IN-, /RST for Guaranteed Response at Output		40	-	-	ns
$t_{RST-MIN}$	Pulse Width of /RST for Resetting /FLT		800	-	-	ns

## DRIVER OUTPUT

$V_{OUTL1}$	Output Low State ( $V_{OUTL} - V_{EE2}$ )	$I_{SINK} = 200\text{ mA}$	-	0.1	0.2	V
$V_{OUTL3}$		$I_{SINK} = 1.0\text{ A}$ , $T_A = 25^\circ\text{C}$	-	0.7	0.8	
$V_{OUTL4}$		$I_{SINK} = 1.0\text{ A}$ , $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$	-	-	1	
$V_{OUTH1}$	Output High State ( $V_{DD2} - V_{OUTH}$ )	$I_{SRC} = 200\text{ mA}$	-	0.3	0.5	V
$V_{OUTH3}$		$I_{SRC} = 1.0\text{ A}$ , $T_A = 25^\circ\text{C}$	-	0.9	1	
$V_{OUTH4}$		$I_{SRC} = 1.0\text{ A}$ , $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$	-	-	1.5	
$I_{PK-SNK1}$	Peak Driver Current, Sink (Note 10)		-	7.1	-	A
$I_{PK-SRC1}$	Peak Driver Current, Source (Note 10)		-	7.8	-	A
$I_{PK-SNK-STO}$	Soft Turn Off Sinking Current (Note 10)	$V_{EE2} = -8\text{ V}$ , $T_A = 25^\circ\text{C}$ , $C_G = 100\text{ nF}$ , $R_G = 0\ \Omega$	-	200	-	mA

## MILLER CLAMP

$V_{CLAMP}$	Clamp Voltage ( $V_{CLAMP} - V_{EE2}$ )	$I_{CLAMP} = 2.5\text{ A}$ , $T_A = 25^\circ\text{C}$	-	1.7	1.9	V
		$I_{CLAMP} = 2.5\text{ A}$ , $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$	-	-	2.7	
$V_{CLAMP-THR}$	Clamp Activation Threshold ( $V_{CLAMP} - V_{EE2}$ )		1.5	2	2.5	V

## IGBT SHORT CIRCUIT CLAMPING

$V_{CLAMP-OUT}$	Clamping Voltage, Sourcing (NCx57100: $V_{OUTH} - V_{DD2}$ , NCx57101: $V_{OUT} - V_{DD2}$ )	$I_{CLAMP-OUT} = 500\text{ mA}$ (pulse test, $t_{CLPmax} = 10\ \mu\text{s}$ )	-	0.9	1.1	V
-----------------	--	---	---	-----	-----	---

## DESAT PROTECTION

$V_{DESAT-THR}$	DESAT Threshold Voltage		8.5	9	9.5	V
$V_{DESAT-NEG}$	DESAT Negative Voltage	$I_{DESAT} = 1.5\text{ mA}$	-8	-	-	V
$I_{DESAT-CHG}$	Blanking Charge Current	$V_{DESAT} = 7\text{ V}$	0.4	0.5	0.6	mA
$I_{DESAT-DIS}$	Blanking Discharge Current		-	50	-	mA

## DESAT CHECK FUNCTIONS (DSCHK)

$t_{RST-ACT1}$	Negative Input Pulse Width to activate DSCHK function	(see Figure 9)	-	200	-	ns
----------------	---	----------------	---	-----	---	----



# NCD57100, NCD57101, NCV57100, NCV57101

**ELECTRICAL CHARACTERISTICS** ( $V_{DD1} = 5\text{ V}$ ,  $V_{DD2} = 15\text{ V}$ ,  $V_{EE2} = -8\text{ V}$ . For typical values  $T_A = 25^\circ\text{C}$ , for min/max values,  $T_A$  is the operating ambient temperature range that applies, unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
$t_{\text{RST-ACT}}$	Input Pulse Width to activate DSCHK function	15 LOW pulses $t_{\text{RST-ACT}}$ on /RST pin (see Figure 9)	8	-	10	$\mu\text{s}$

## DISABLE OUTPUT

$t_{\text{RST-DIS}}$	Output disable function propagation delay (Note 10)	$V_{\text{IL}}$ pulse width higher than $t_{\text{MIN2}}$ on /RST pin to 90% of OUTx to disable output	-	-	90	ns
----------------------	---	--	---	---	----	----

## DYNAMIC CHARACTERISTICS

$t_{\text{PD-ON}}$	IN+, IN- to Output High Propagation Delay	$C_{\text{LOAD}} = 10\text{ nF}$ $V_{\text{IH}}$ to 10% of pulse width higher than $t_{\text{MIN2}}$ . OUTx and CLAMP pins are connected together	50	70	90	ns
$t_{\text{PD-OFF}}$	IN+, IN- to Output Low Propagation Delay	$C_{\text{LOAD}} = 10\text{ nF}$ $V_{\text{IL}}$ to 90% of pulse width higher than $t_{\text{MIN2}}$ . OUTx and CLAMP pins are connected together	50	70	90	ns
$t_{\text{DISTORT}}$	Propagation Delay Distortion (= $t_{\text{PD-ON}} - t_{\text{PD-OFF}}$ )	$T_A = 25^\circ\text{C}$ , pulse width higher than $t_{\text{MIN2}}$	-15	0	15	ns
		$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$ , pulse width higher than $t_{\text{MIN2}}$	-25	-	25	
$t_{\text{DISTORT\_TOT}}$	Prop Delay Distortion between Parts	PW > 150 ns	-30	0	30	ns
$t_{\text{RISE}}$	Rise Time (see Fig. 5) (Note 10)	$C_{\text{LOAD}} = 1\text{ nF}$ , 10% to 90% of Output Change	-	15	-	ns
$t_{\text{FALL}}$	Fall Time (see Fig. 5) (Note 10)	$C_{\text{LOAD}} = 1\text{ nF}$ , 90% to 10% of Output Change	-	15	-	ns
$t_{\text{LEB}}$	DESAT Leading Edge Blanking Time (see Fig. 7)		-	400	-	ns
$t_{\text{FILTER}}$	DESAT Threshold Filtering Time (see Fig. 7)		-	360	-	ns
$t_{\text{FLT}}$	Delay after $t_{\text{FILTER}}$ to /FLT		-	450	-	ns
$t_{\text{MUTE}}$	DESAT Mute time after $t_{\text{FILTER}}$		-	5	-	$\mu\text{s}$
$t_{\text{RST}}$	/RST Rise to /FLT Rise Delay		-	23	100	ns
$t_{\text{UV1F}}$	UVLO1 Filter time (see Fig. 6) (Note 10)		-	1	-	$\mu\text{s}$
$t_{\text{UV1R}}$	$V_{\text{UVLO1\_OUT\_ON}}$ to RDY High Delay (see Fig. 6) (Note 10)		-	250	-	ns
$t_{\text{RDY1F}}$	UVLO1 to RDY Low Delay (see Fig. 6) (Note 10)		-	10	-	ns
$t_{\text{RDY1O}}$	RDY High to Output High Delay (see Fig. 6)		-	55	-	ns
$t_{\text{RDY2O}}$						
$t_{\text{UV2R}}$	UVLO2 Filter time (see Fig. 6)		-	2.5	-	$\mu\text{s}$
$t_{\text{UV2F}}$						
$t_{\text{RDY2F}}$	$V_{\text{UVLO2\_OUT\_OFF}}$ to RDY Low Delay (see Fig. 6)		-	5	-	$\mu\text{s}$
$t_{\text{RDY2R}}$	$V_{\text{UVLO2\_OUT\_ON}}$ to RDY High Delay (see Fig. 6) (Note 10)		-	2.6	-	$\mu\text{s}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

10. Values based on design and/or characterization.

# NCD57100, NCD57101, NCV57100, NCV57101

## ORDERING INFORMATION

Device	Qualification	Package Type	Shipping <sup>†</sup>
NCD57100DWR2G	NCD – Industry NCV – Automotive	SOIC-16 Wide Body (Pb-Free)	1,000 / Tape & Reel
NCV57100DWR2G			
NCD57101DWR2G			
NCV57101DWR2G			

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

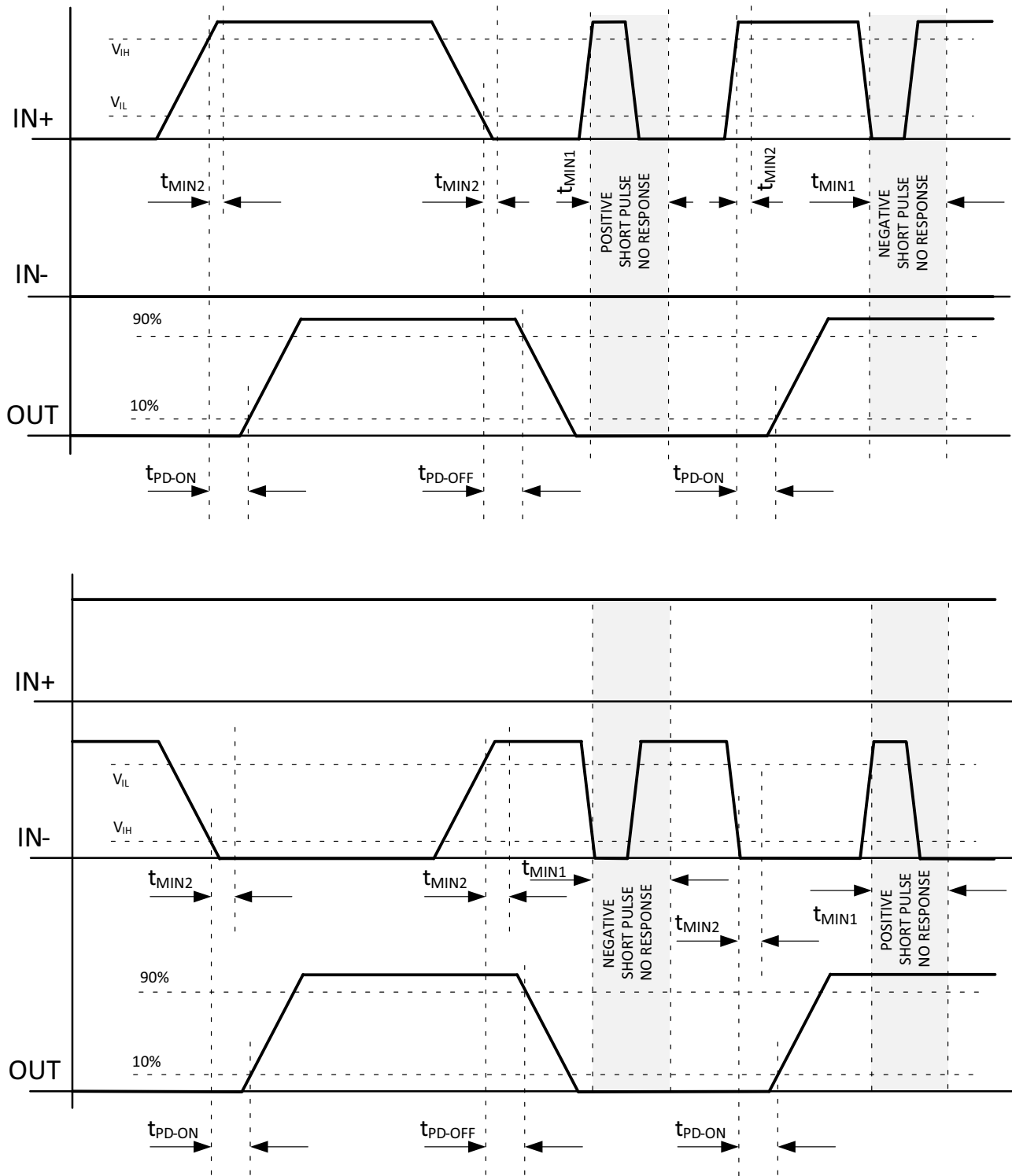


Figure 5. Propagation Delay, Rise and Fall Time

NCD57100, NCD57101, NCV57100, NCV57101

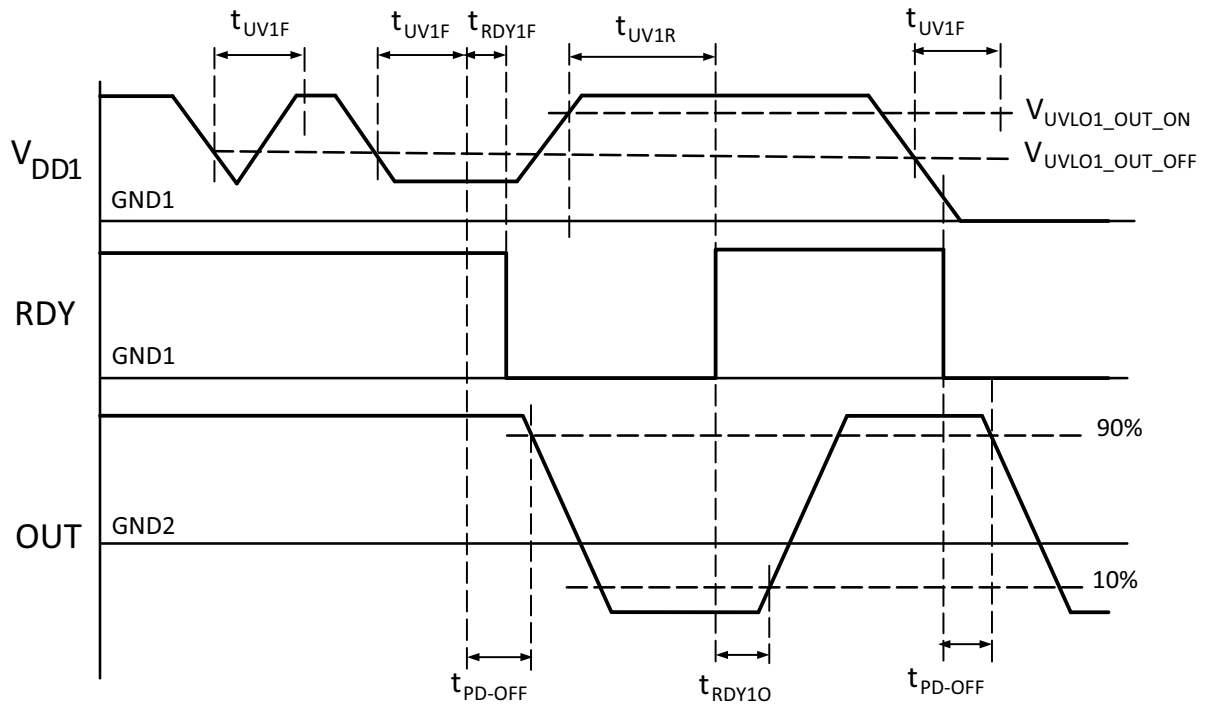


Figure 6a. UVLO1 Waveform

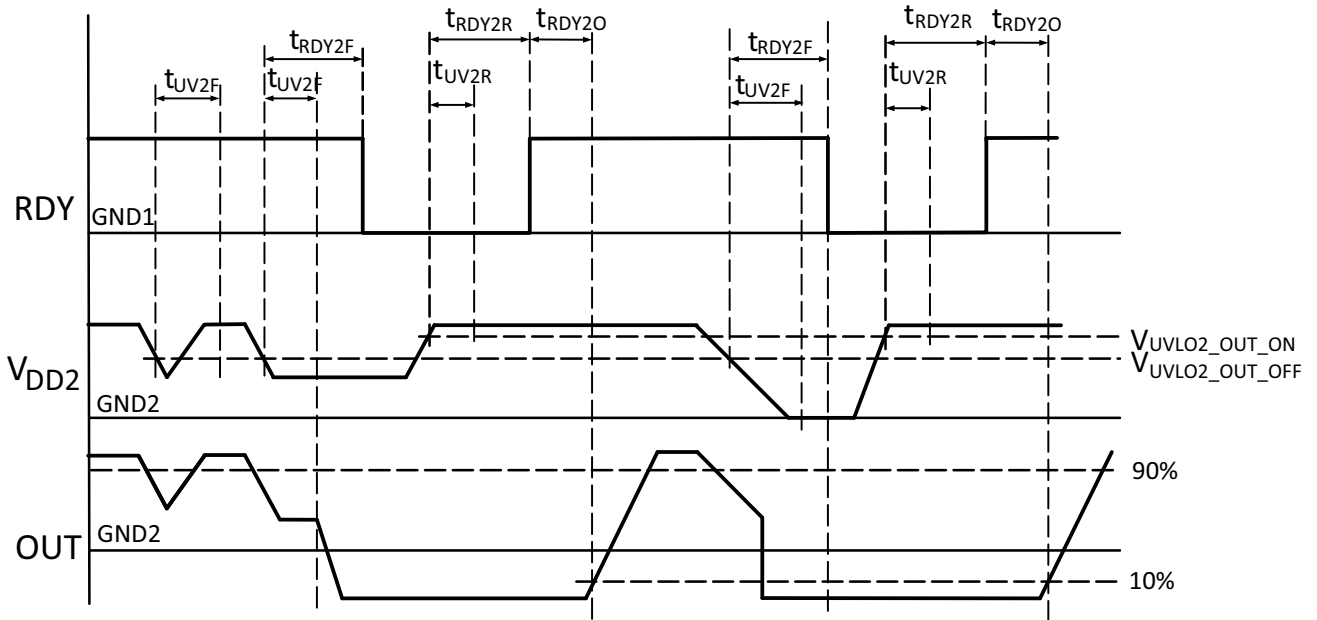


Figure 6b. UVLO2 Waveform

NCD57100, NCD57101, NCV57100, NCV57101

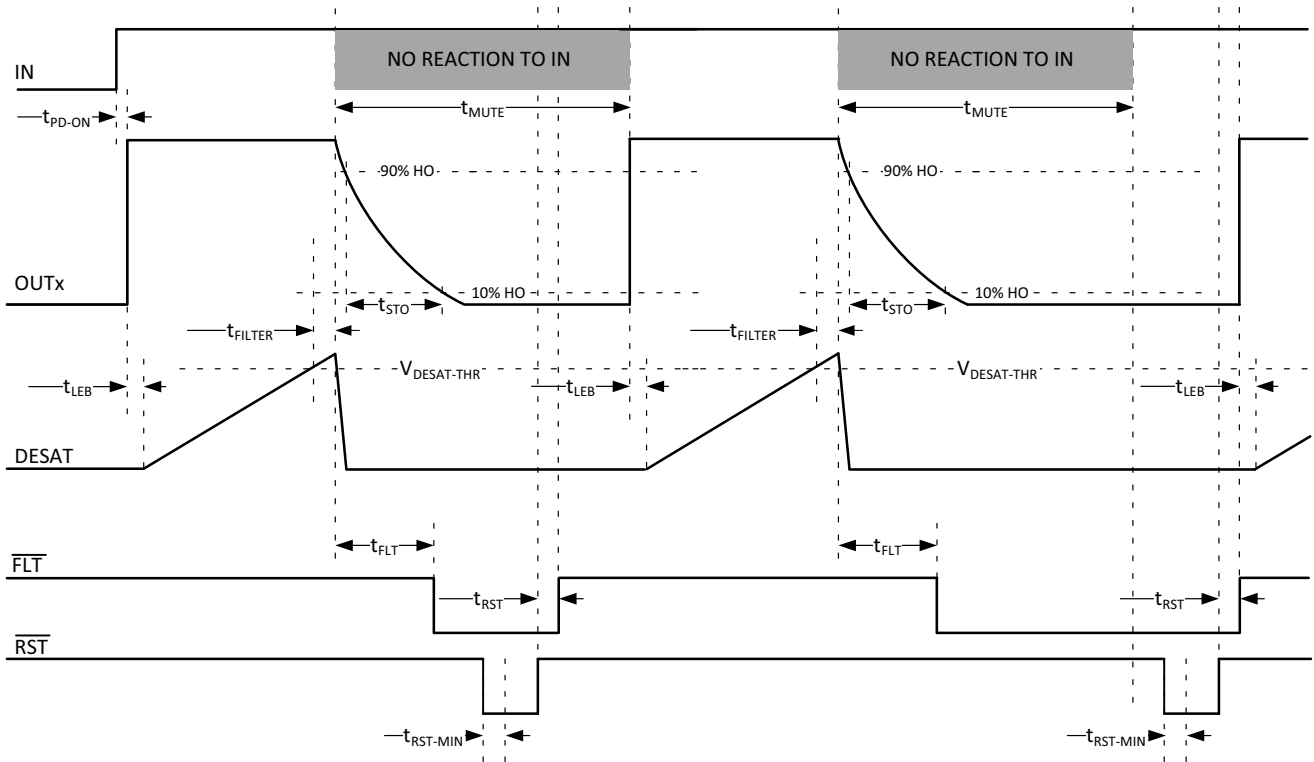


Figure 7. DESAT Response Waveform

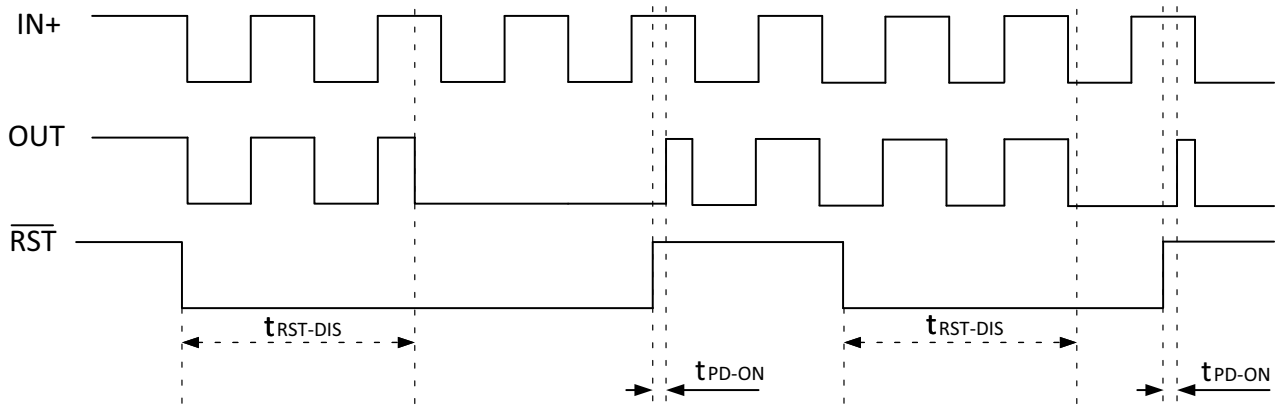


Figure 8. DISABLE

NCD57100, NCD57101, NCV57100, NCV57101

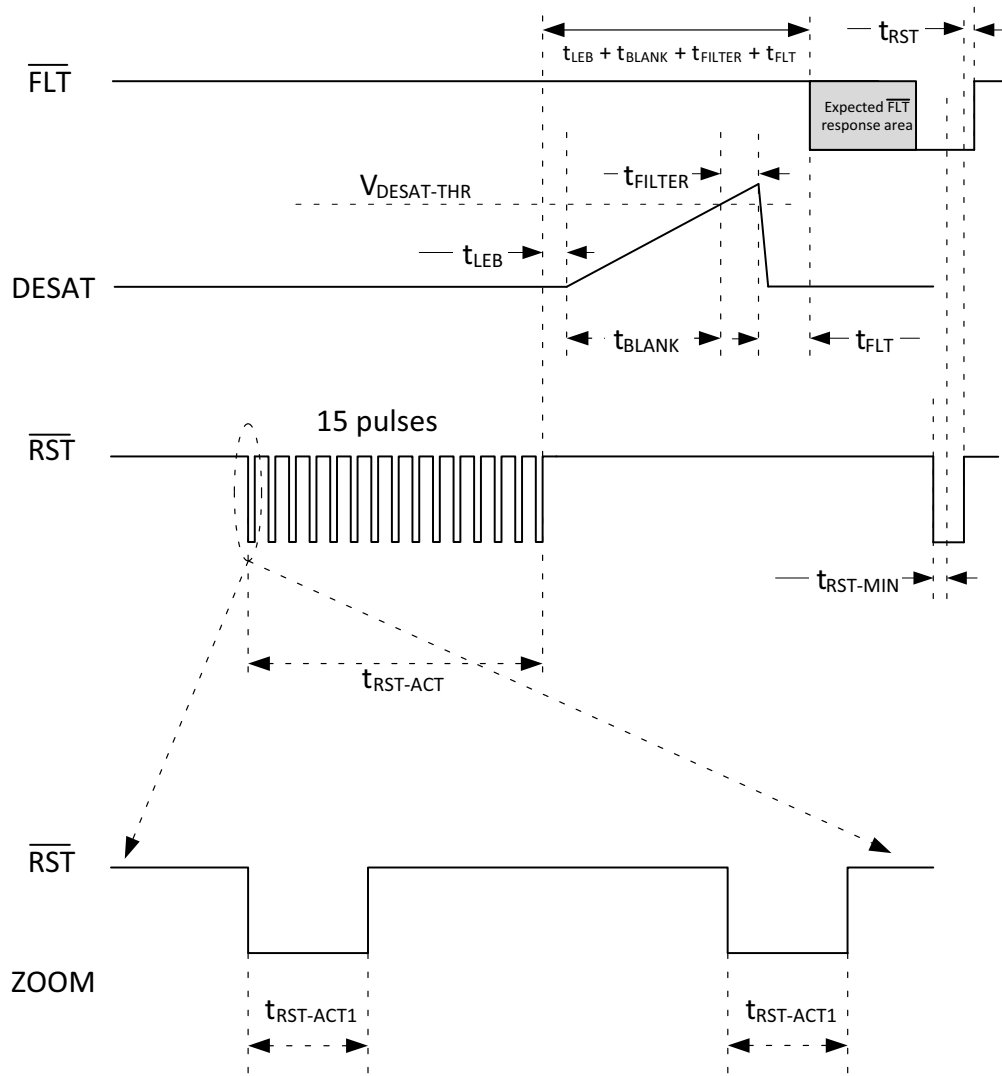


Figure 9. DESAT Check Functions (DSCHK)

TRUTH TABLE

IN	UVLO1	UVLO2	DESAT*	OUT	/RST	RDY	/FLT	Notes
L	Inactive	Inactive	L	L	X	↗	↗	Initial condition after power up $V_{DD1}$ and $V_{DD2}$
↗	Inactive	Inactive	L	↗	X	H	H	Initial condition – IN First Rising edge
H	Inactive	Inactive	L	H	X	H	H	Normal Operation – Output High
L	Inactive	Inactive	L	L	X	H	H	Normal Operation – Output Low
X	Active	Inactive	X	L	X	L	L	UVLO1 Activated – RDY Low ( $t_{RDY1F}$ ), /FLT Low, Output Low
X	Inactive	Inactive	X	X	X	H	H	UVLO1 Recovered – RDY High, /FLT High
X	Inactive	Active	X	L	X	L	H	UVLO2 Activated – RDY Low ( $t_{RDY2F}$ ), Output Low
X	Inactive	Inactive	X	X	X	H	H	UVLO2 Recovered – RDY High, /FLT High
H	Inactive	Inactive	H ( $>t_{FILTER}$ )	L	X	H	L	DESAT Activated – /FLT Low ( $t_{FLT}$ ), Output Low
X	Inactive	Inactive	L	X	↘ ( $>t_{RST}$ )	H	↗	/FLT reset, DESAT conditions disappear, $t_{RST}$ pulse applied
↗ ↘	Inactive	Inactive	L	L	L ( $>t_{RST-DIS}$ )	H	H	Output DISABLED
L	Inactive	Inactive	X	L	$15 \times t_{RST-ACT1}$	H	L	DESAT circuit check function activated

\* L =  $V_{DESAT} < V_{DESAT-THR}$ , H =  $V_{DESAT} > V_{DESAT-THR}$

# NCD57100, NCD57101, NCV57100, NCV57101

## TYPICAL CHARACTERISTICS

(Conditions for the following figures are the same as stated for ELECTRICAL CHARACTERISTICS Table unless otherwise noted. Typical and/or average values are used.)

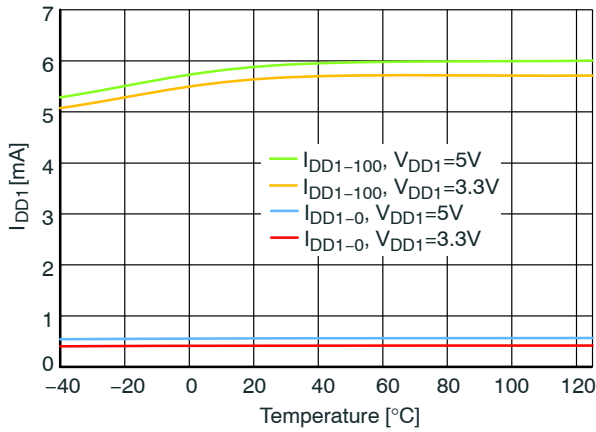


Figure 10.  $V_{DD1}$  Supply Current

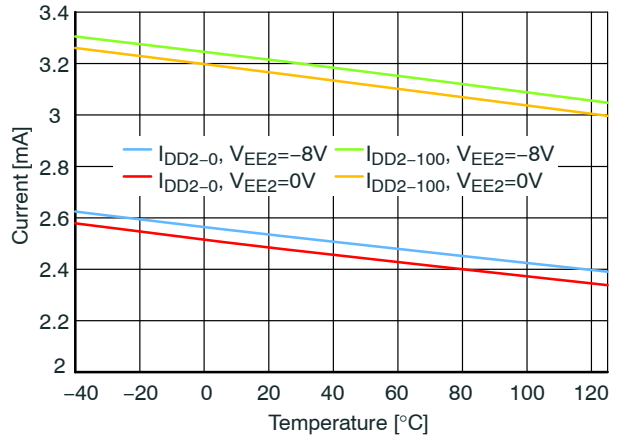


Figure 11.  $V_{DD2}$  Supply Current

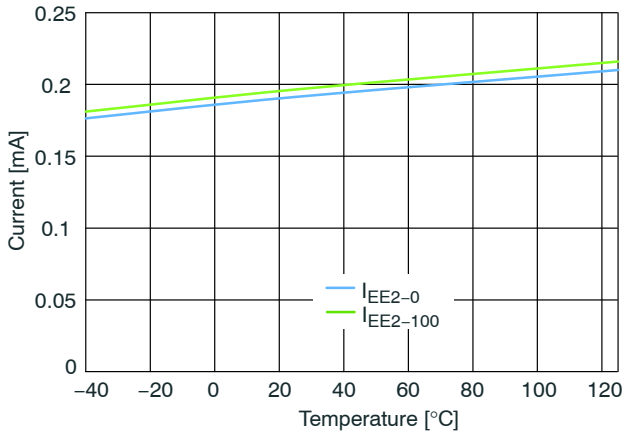


Figure 12.  $V_{EE2}$  Supply Current

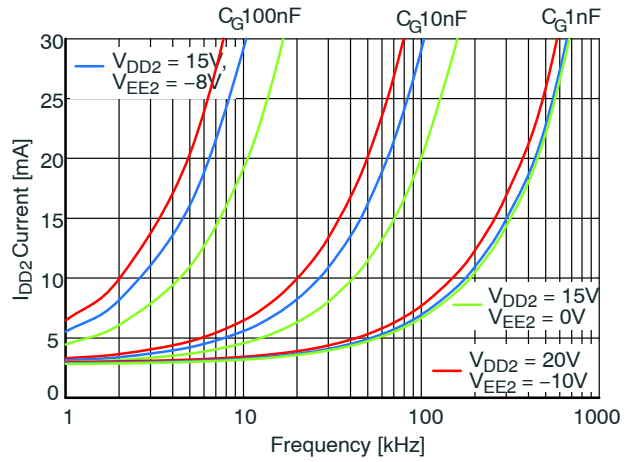


Figure 13.  $V_{DD2}$  Supply Current vs. Frequency

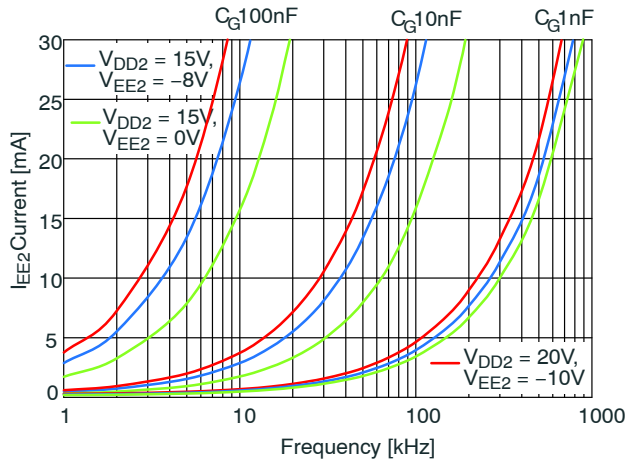


Figure 14.  $V_{EE2}$  Supply Current vs. Frequency

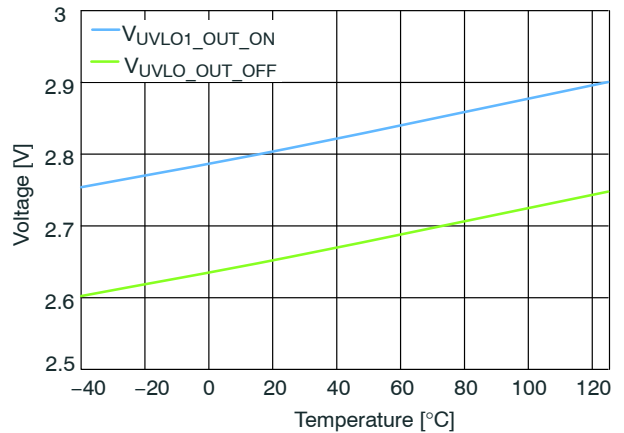


Figure 15. UVLO1 Threshold Voltage

# NCD57100, NCD57101, NCV57100, NCV57101

## TYPICAL CHARACTERISTICS

(Conditions for the following figures are the same as stated for ELECTRICAL CHARACTERISTICS Table unless otherwise noted. Typical and/or average values are used.) (continued)

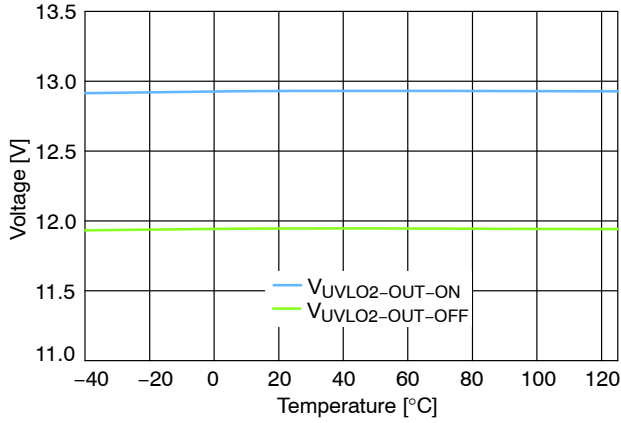


Figure 16. UVLO2 Threshold Voltage

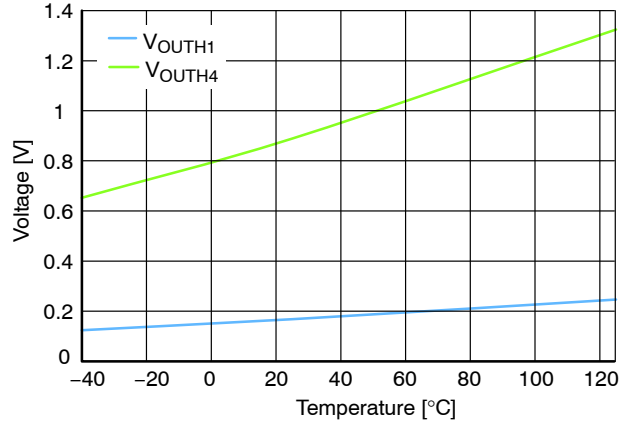


Figure 17. Output Voltage Drop, Sourcing

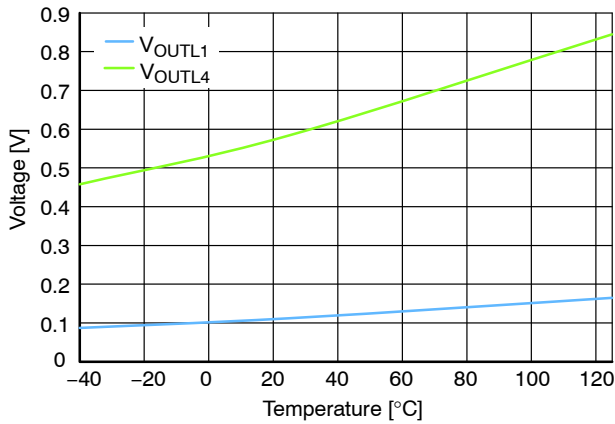


Figure 18. Output Voltage Drop, Sinking

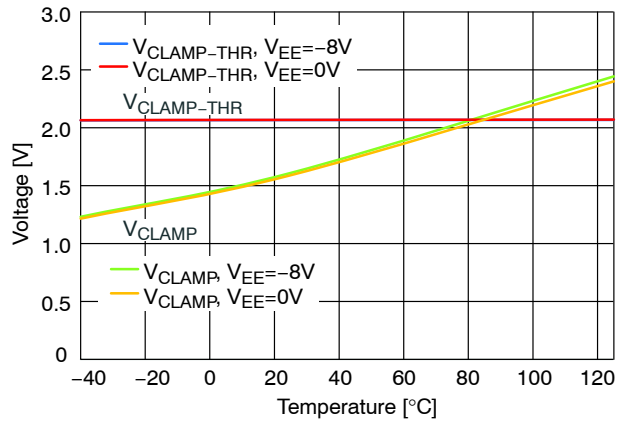


Figure 19. CLAMP Voltage Drop

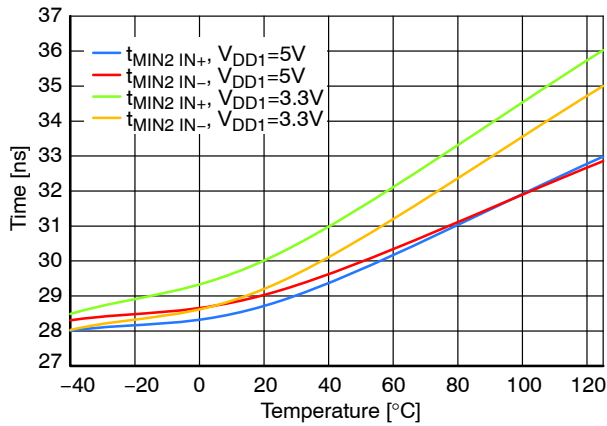


Figure 20. Minimum Pulse Width For Guaranteed Response

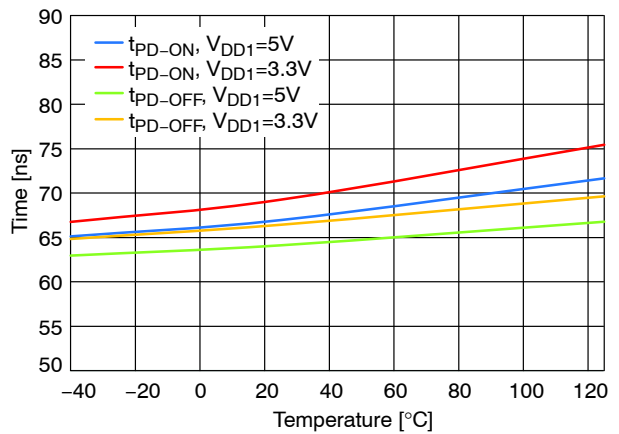


Figure 21. Propagation Delay



# NCD57100, NCD57101, NCV57100, NCV57101

## TYPICAL CHARACTERISTICS

(Conditions for the following figures are the same as stated for ELECTRICAL CHARACTERISTICS Table unless otherwise noted. Typical and/or average values are used.) (continued)

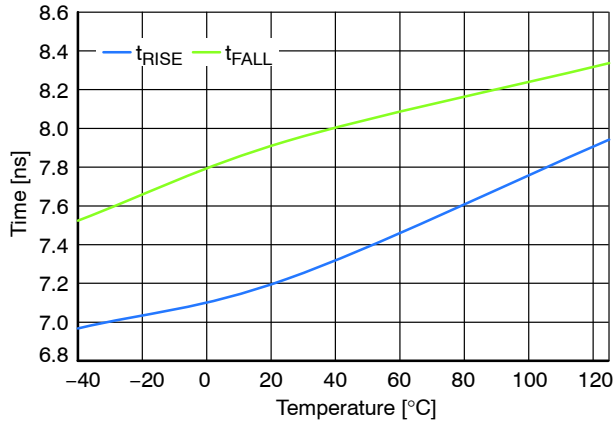


Figure 22. Rise and Fall Time

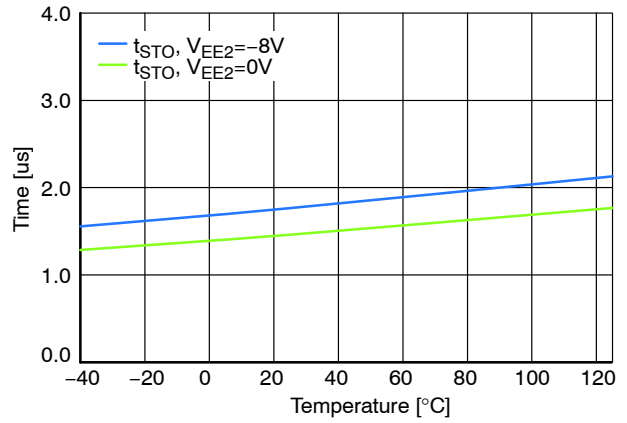


Figure 23. Soft Turn Off Time

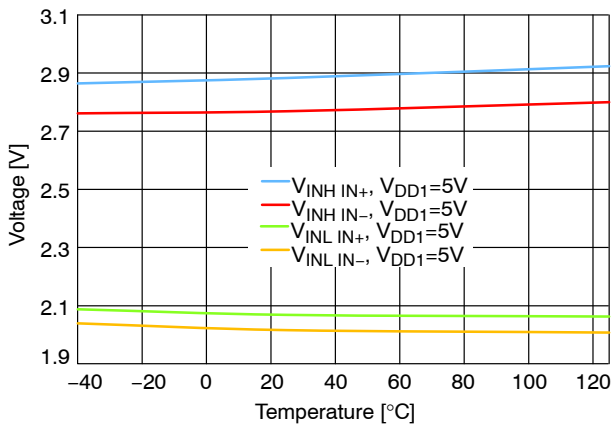


Figure 24. Input High Voltage Level, V<sub>DD1</sub> = 5 V

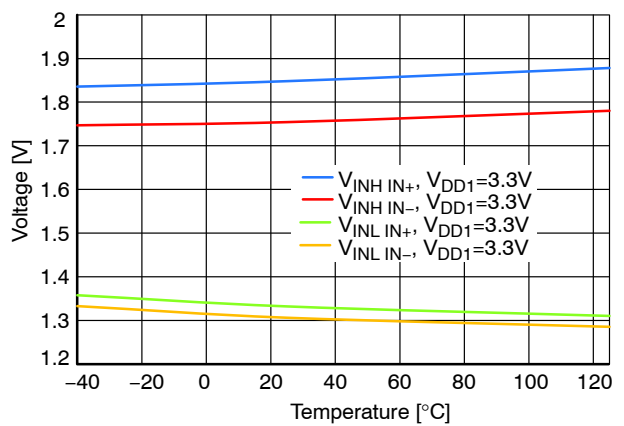


Figure 25. Input High Voltage Level, V<sub>DD1</sub> = 3.3 V

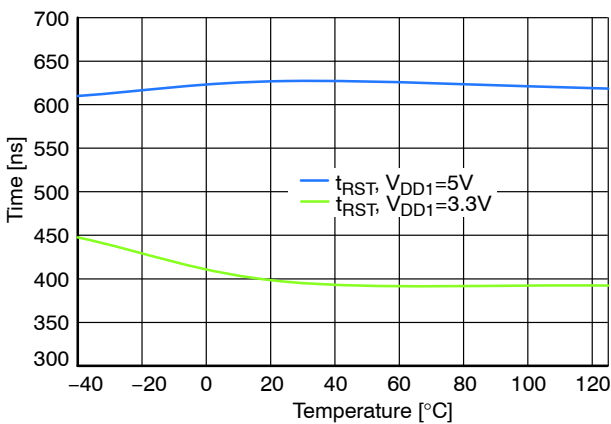


Figure 26. Minimum Fault Reset Time

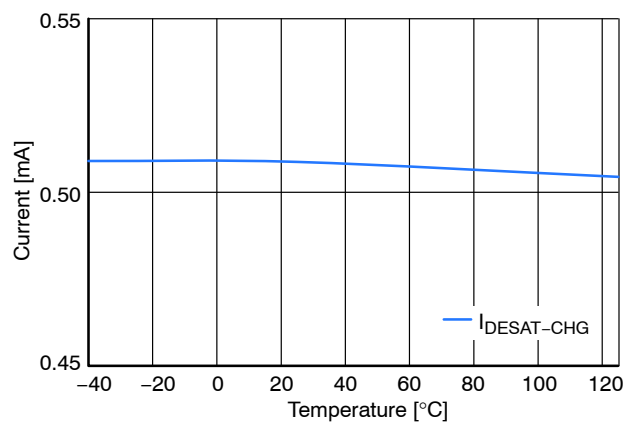


Figure 27. Desat Charge Current

TYPICAL CHARACTERISTICS

(Conditions for the following figures are the same as stated for ELECTRICAL CHARACTERISTICS Table unless otherwise noted. Typical and/or average values are used.) (continued)

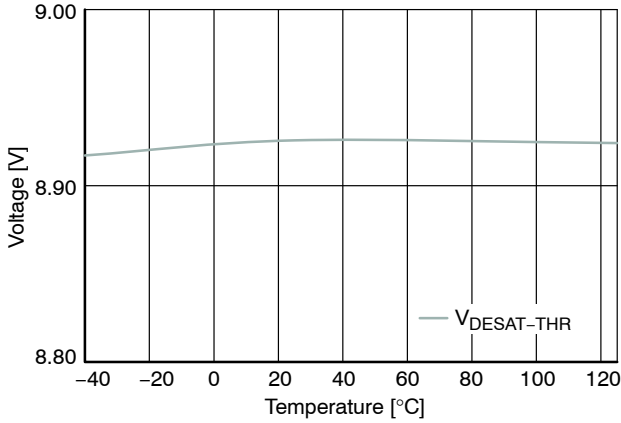


Figure 28. Desat Threshold Voltage

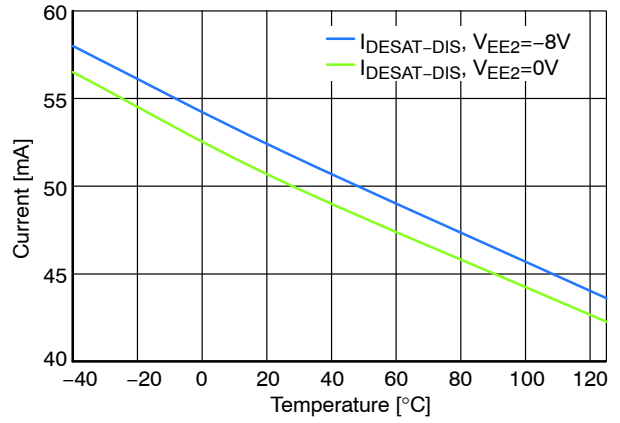


Figure 29. Desat Discharge Current

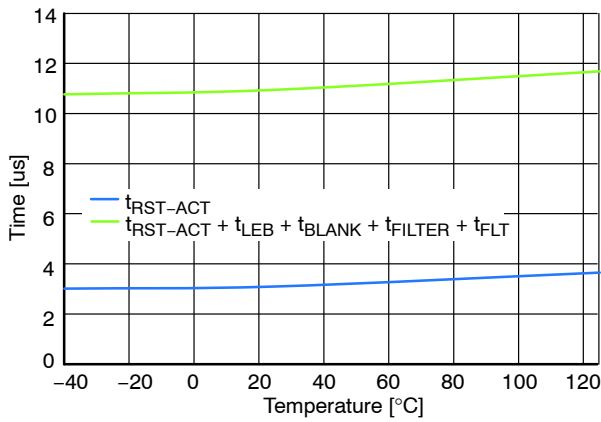


Figure 30. DESAT Check Activation (15 pulses 250 ns)

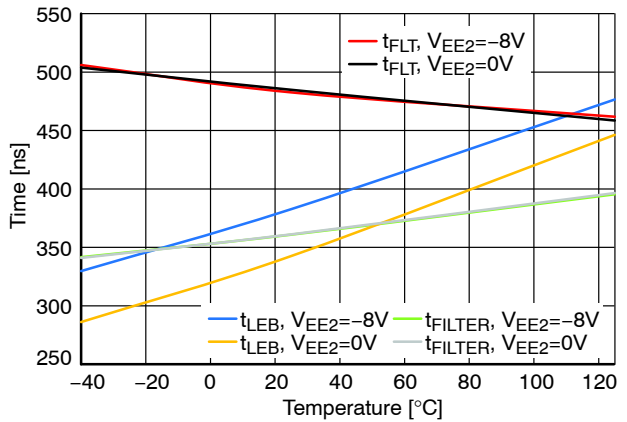


Figure 31. DESAT Time Parameters

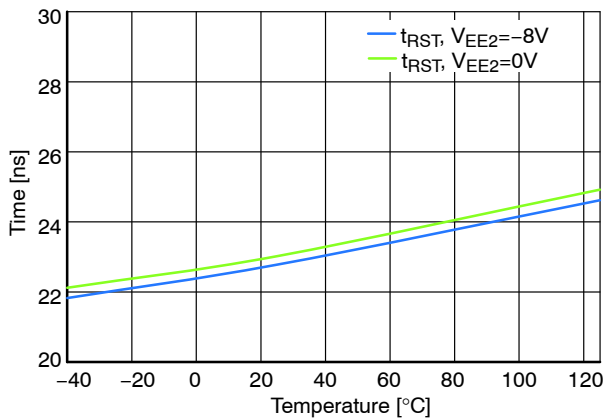


Figure 32. Reset to Fault Response Time

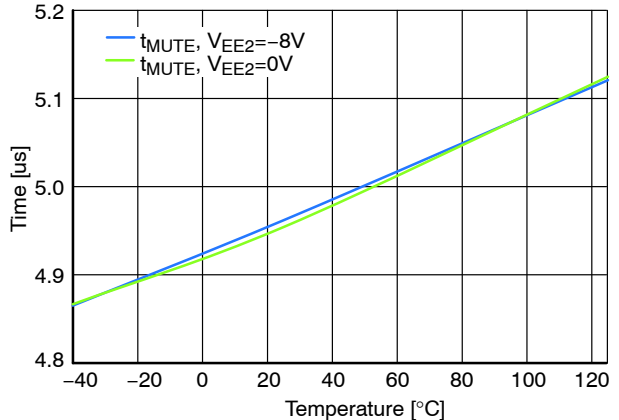


Figure 33. DESAT Mute Time

TYPICAL CHARACTERISTICS

(Conditions for the following figures are the same as stated for ELECTRICAL CHARACTERISTICS Table unless otherwise noted. Typical and/or average values are used.) (continued)

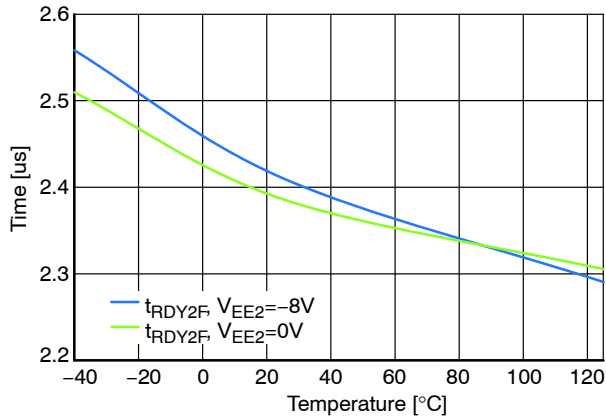


Figure 34. UVLO2 to RDY Delay

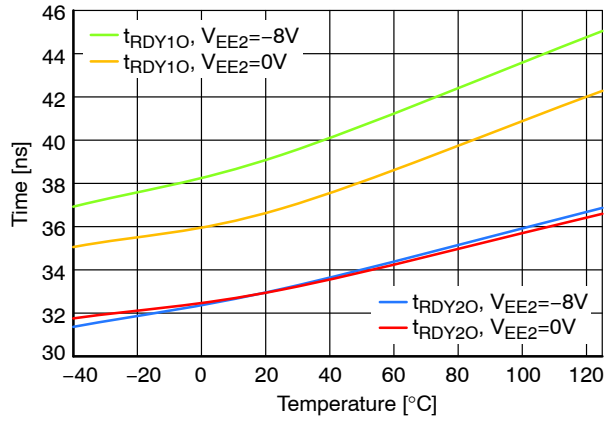


Figure 35. RDY to OUT Delay

FEATURE DESCRIPTIONS

**Under Voltage Lockout (UVLO)**

UVLO ensures correct switching of IGBT connected to the driver output.

- The IGBT is turned-off, if the supply  $V_{DD1}$  drops below  $V_{UVLO1-OUT-OFF}$  and the RDY pin output goes to low.
- The driver output does not start to react to the input signal on  $V_{IN}$  until the  $V_{DD1}$  rises above the  $V_{UVLO1-OUT-ON}$  again. If the supply  $V_{DD1}$  increase over  $V_{UVLO1-OUT-ON}$ , the RDY pin output goes to be open-drain and outputs continue to switch IGBT

- The IGBT is turned-off, if the supply  $V_{DD2}$  drops below  $V_{UVLO2-OUT-OFF}$  and the RDY pin output goes to low.
- The driver output does not start to react to the input signal on  $V_{IN}$  until the  $V_{DD2}$  rises above the  $V_{UVLO2-OUT-ON}$  again. If the supply  $V_{DD2}$  increases over  $V_{UVLO2-OUT-ON}$ , the RDY pin output goes to be open-drain and outputs continue to switch IGBT
- VEE2 is not monitored.

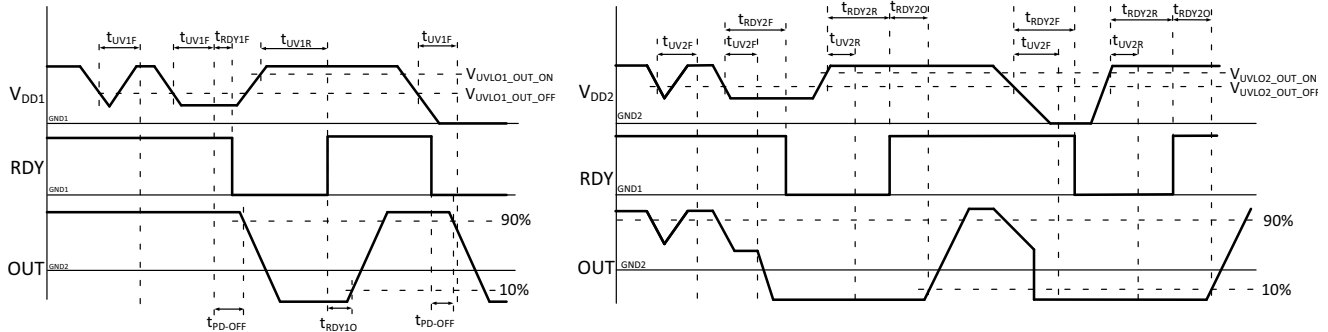


Figure 36. UVLO Diagram

**Active Miller Clamp Protection (CLAMP)**

NCx5710y supports both bipolar and unipolar power supply with active Miller clamp.

For operation with bipolar supplies, the IGBT is turned off with a negative voltage through OUTL/OUT with respect to its emitter. This prevents the IGBT from unintentionally turning on because of current induced from its collector to its gate due to Miller effect. In this condition it is not necessary to connect CLAMP output of the gate driver to the IGBT gate, but connecting CLAMP output to the IGBT gate is also not an issue. Typical values for bipolar operation are  $V_{DD2} = 15\text{ V}$  and  $V_{EE2} = -8\text{ V}$  with respect to  $GND_2$ .

For operation with unipolar supply, typically,  $V_{DD2} = 15\text{ V}$  with respect to  $GND_2$ , and  $V_{EE2} = GND_2$ . In this case, the IGBT can turn on due to additional charge from IGBT Miller capacitance caused by a high voltage slew rate transition on the IGBT collector. To prevent IGBT to turn on, the CLAMP pin is connected directly to IGBT gate and Miller current is sunk through a low impedance CLAMP transistor. When the IGBT is turned-off and the gate voltage transitions below  $V_{CLAMP-THR}$ , the CLAMP current output is activated.

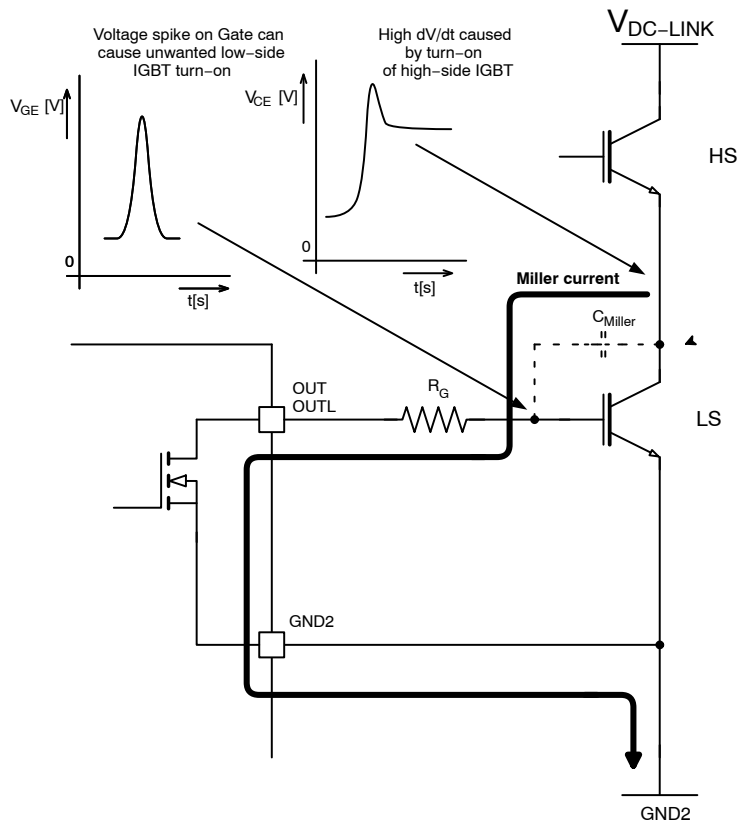


Figure 37. Current Path without Miller Clamp Protection

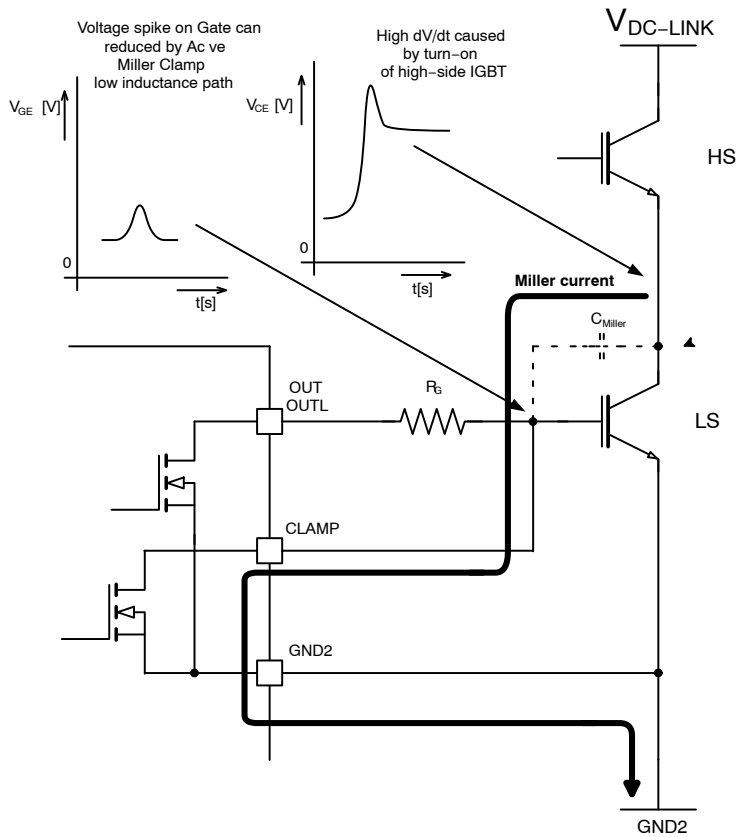


Figure 38. Current Path with Miller Clamp Protection

**Non-inverting and Inverting Input Pin (IN+, IN-)**

NCx5710y has two possible input modes to control IGBT. Both inputs have defined minimum input pulse width to filter occasional glitches.

- Non-inverting input IN+ controls the driver output while inverting input IN- is set to LOW
- Inverting input IN- controls the driver output while non-inverting input IN+ is set to HIGH

**Warning:** When the application uses an independent or separate power supply for the control unit and the input side of the driver, all inputs should be protected by a serial resistor (In case of a power failure of the driver, the driver may be damaged due to overloading of the input protection circuits)

**Desaturation Protection (DESAT)**

Desaturation protection ensures the protection of IGBT at short circuit. When the  $V_{CE-SAT}$  voltage goes up and reaches the set limit, the output is driven low by Soft Turn Off and /FLT output is activated. Blanking time can be set by internal current source and an external capacitor. To avoid false DESAT triggering and minimize blanking time, fast switching diodes with low internal capacitance are recommended. All DESAT protective diodes internal capacitances build voltage divider with the blanking capacitor.

**Warning:** Both external protective diodes are recommended for the protection against voltage spikes caused by IGBT transients passing through parasitic capacitances.

**DESAT Circuit Parameters Specification**

$$t_{BLANK} = C_{BLANK} \cdot \frac{V_{DESAT-THR}}{I_{DESAT-CHG}}$$

$$V_{DESAT-THR} > R_{S-DESAT} \cdot I_{DESAT-CHG} + V_{F\ HV\ diode} + V_{CESAT\_IGBT}$$

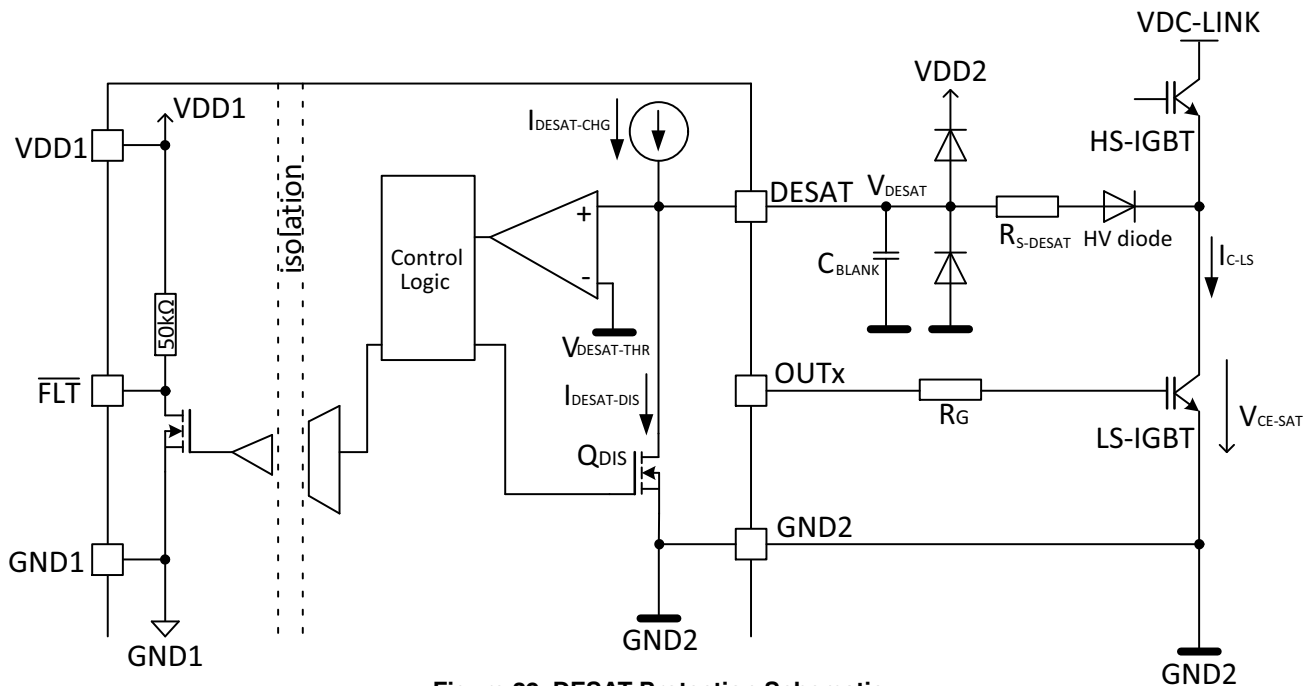


Figure 39. DESAT Protection Schematic

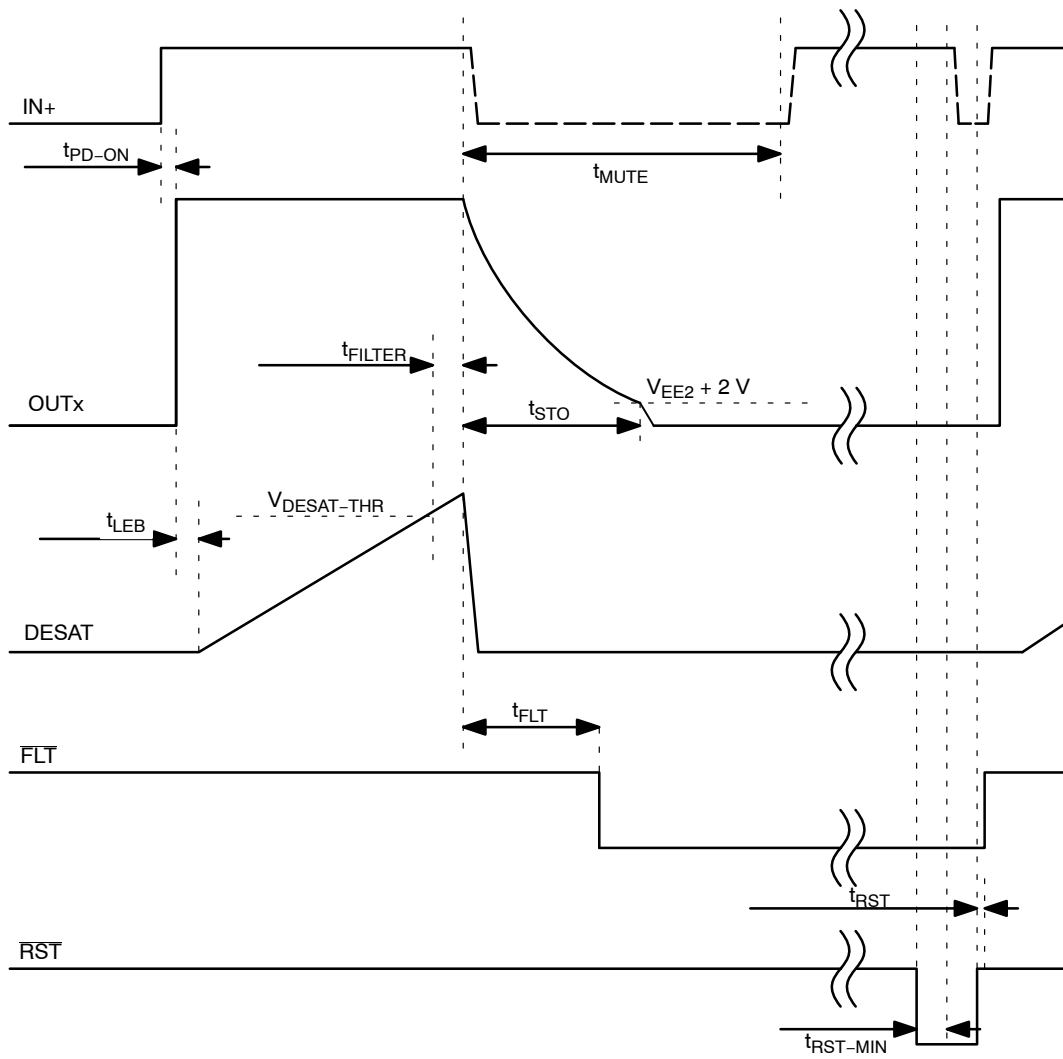


Figure 40. DESAT Switch Off Behavior

**Fault Output Pin ( $\overline{FLT}$ )**

$\overline{FLT}$  open-drain output provides feedback to the controller about driver DESAT protection conditions. The open-drain  $\overline{FLT}$  outputs of multiple NCx5710y devices can be wired together forming a single, common fault bus for interfacing directly to the microcontroller.  $\overline{FLT}$  output has 50 k $\Omega$  internal pull-up resistor to VDD1.

**Ready Output Pin (RDY)**

RDY open-drain output provides feedback to the controller about driver UVLO protections conditions.

- If either side of device has insufficient supply (VDD1 or VDD2), the RDY pin output goes low; otherwise, RDY pin output is open drain.

The open-drain RDY outputs of multiple NCx5710y devices can be “OR”ed together.

**Reset Input Pin (RST)**

Reset input pin is ACTIVE LOW and has internal pull-up resistor to VDD1. In normal condition the  $\overline{RST}$  pin is connected to HIGH. To reset FAULT conditions or disable output pulses connect  $\overline{RST}$  pin to LOW. To invoke DESAT Check (DSCHK) function apply pulse sequence (see Figure 9).

In applications that do not allow to control the reset,  $\overline{RST}$  pin should be connected to IN+, the driver will be reset by each input pulse. In this case  $t_{MIN2}$  need to be longer than  $t_{RST}$ .

**RESET Input has Three Functions:**

1. Set back the  $\overline{FLT}$  output
  2. It can be used as Disable/shutdown output (independent of the input logic)
  3. It can be used to test DESAT circuit functionality
- ♦ To set back  $\overline{FLT}$  output (if DESAT conditions are fulfilled and  $\overline{FLT}$  output is activated), negative pulse of minimum length  $t_{RST}$  needs to be applied to  $\overline{RST}$  pin. (see Figure 7.)

- ♦ To disable output, negative pulse of minimum length  $t_{RST-DIS}$  needs to be applied to  $\overline{RST}$  pin. (see Figure 8.)
- ♦ To activate DESAT check function apply 15 negative pulses of  $t_{RST-ACT1}$  width and  $t_{RST-ACT}$  pulse Length (see Figure 9.)

**Warning:** When the application uses an independent or separate power supply for the control unit and the input side of the driver, all inputs should be protected by a serial resistor (in case of a power failure of the driver, the driver may be damaged due to overloading of the input protection circuits)

**Power Supply (VDD1, VDD2, VEE2)**

NCx5710y is designed to support two different power supply configurations, bipolar or unipolar power supply. For reliable high output current delivery suitable external power capacitors are required. Parallel combination of 100 nF + 4.7  $\mu$ F ceramic capacitors is optimal for a wide range of applications using IGBT. For reliable driving of IGBT modules (containing several parallel IGBTs) a higher capacity is required (typically 100 nF + 10  $\mu$ F). Capacitors should be as close as possible to the driver’s power pins.

- In bipolar power supply the driver is typically supplied with a positive voltage of 15 V at VDD2 and negative voltage -5 V at VEE2 (Figure 41). Negative power supply prevents a dynamic turn on throughout the internal IGBT input capacitance.
- In Unipolar power supply the driver is typically supplied with a positive voltage of 15 V at VDD2 (Figure 42). Dynamic turn on throughout the internal IGBT input capacitance could be prevented by Active Miller Clamp function. CLAMP output should be directly connected to IGBT gate (Figure 38).

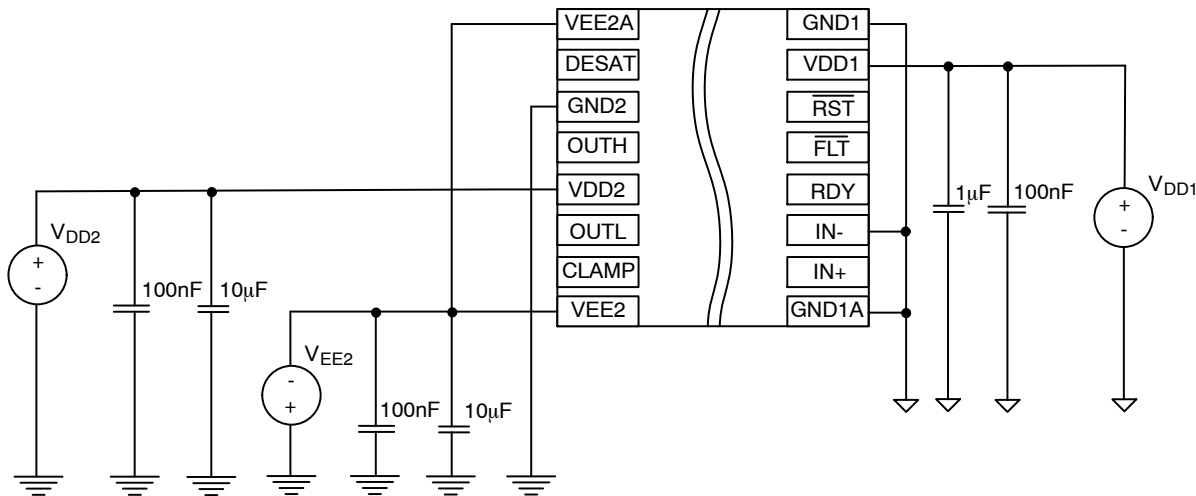


Figure 41. Bipolar Power Supply



NCD57100, NCD57101, NCV57100, NCV57101

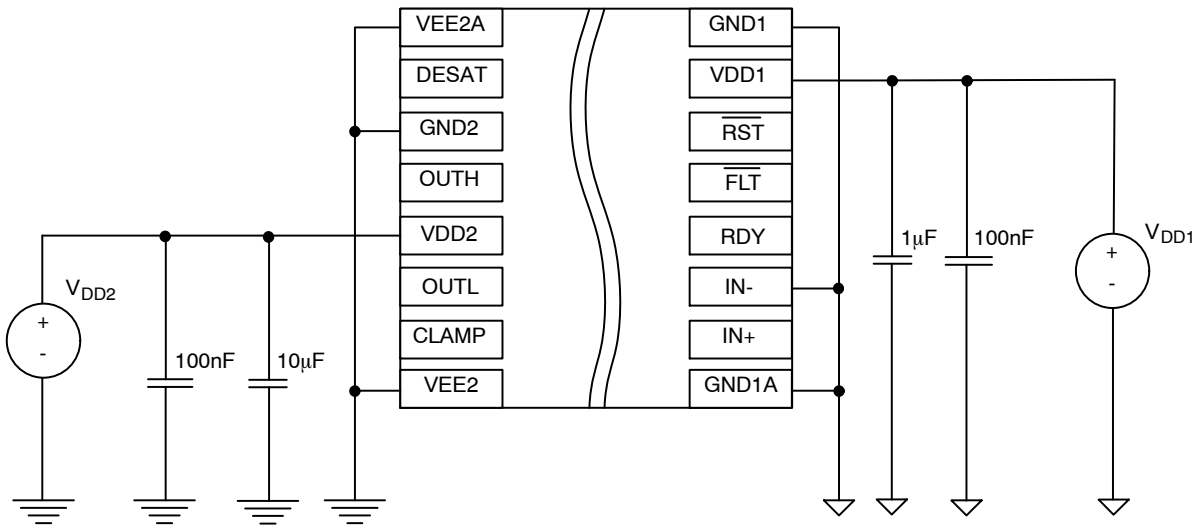


Figure 42. Unipolar Power Supply

Common Mode Transient Immunity (CMTI)

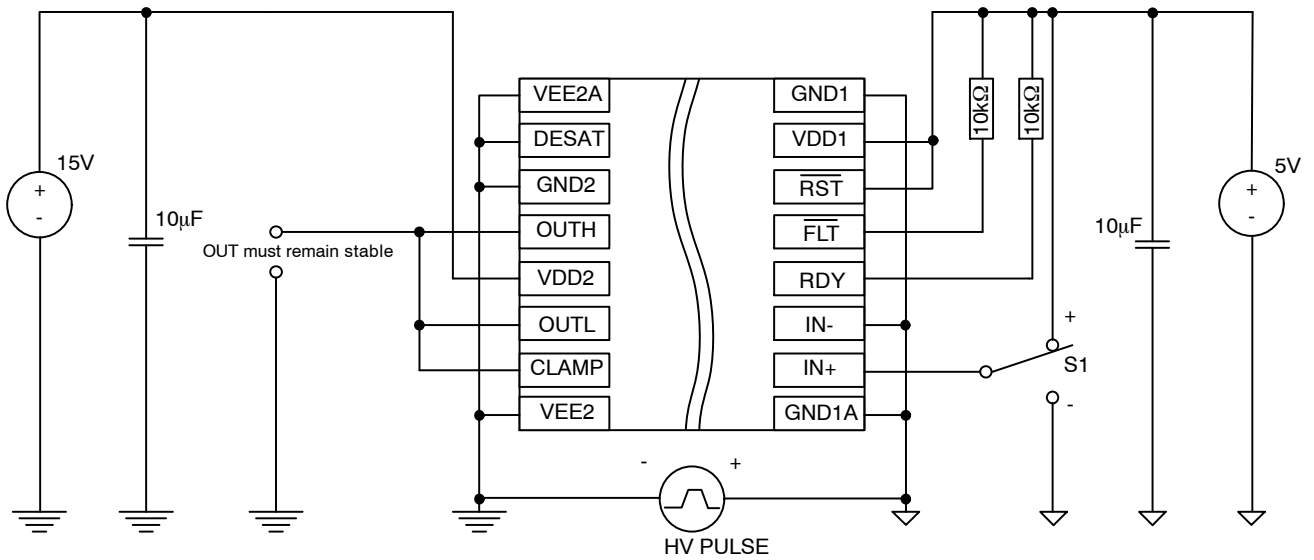


Figure 43. Common-Mode Transient Immunity Test Circuit

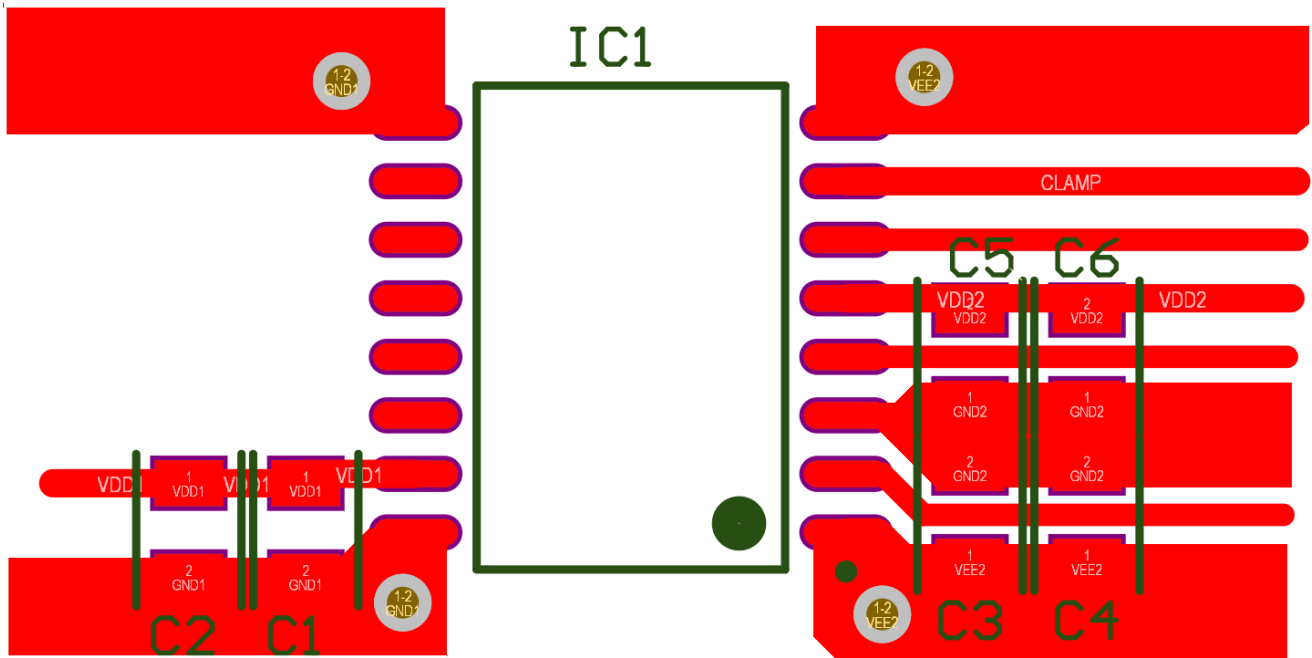
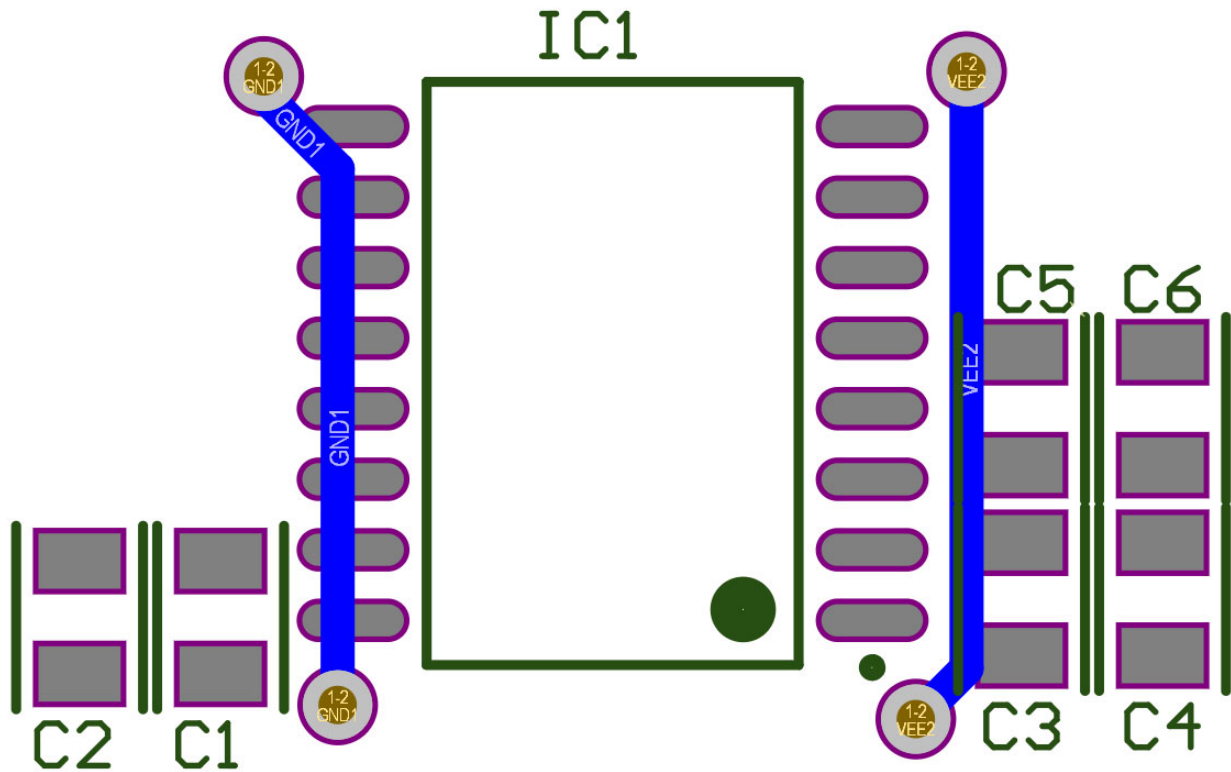


Figure 44. Recommended Basic Bipolar Power Supply PCB Design

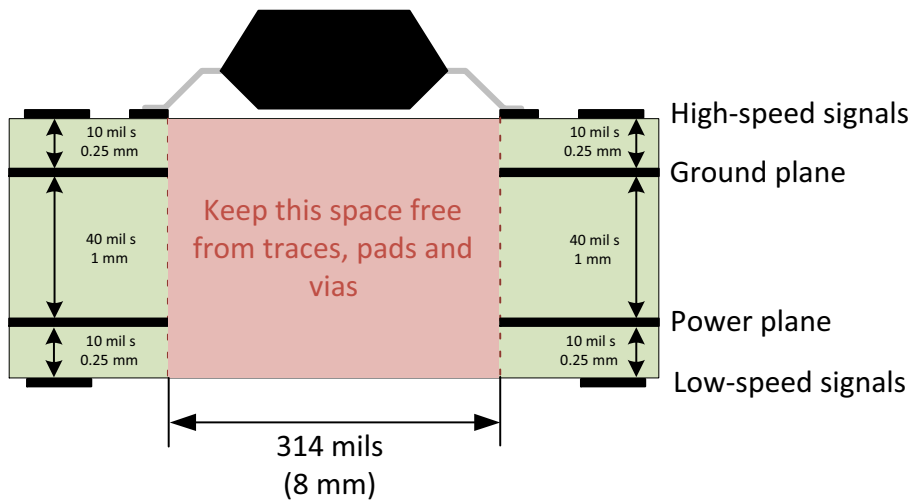
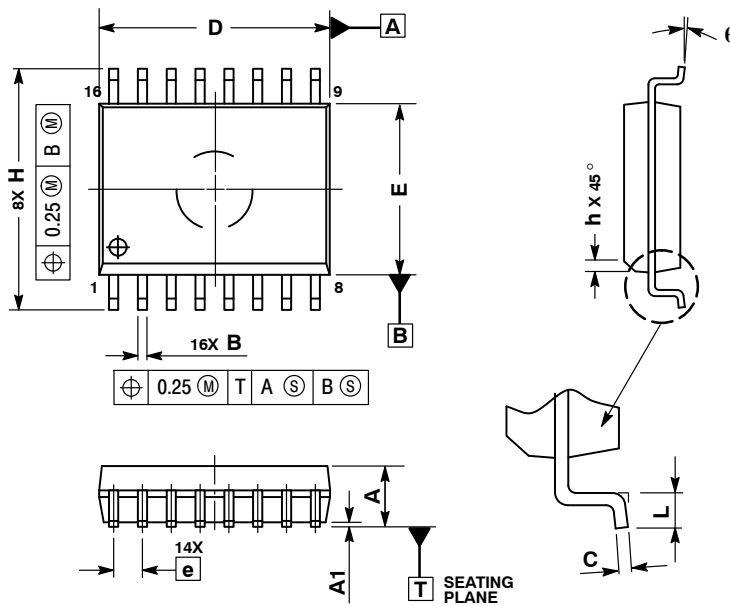


Figure 45. Recommended Layer Stack

# NCD57100, NCD57101, NCV57100, NCV57101

## PACKAGE DIMENSIONS

### SOIC-16 WB CASE 751G-03 ISSUE D

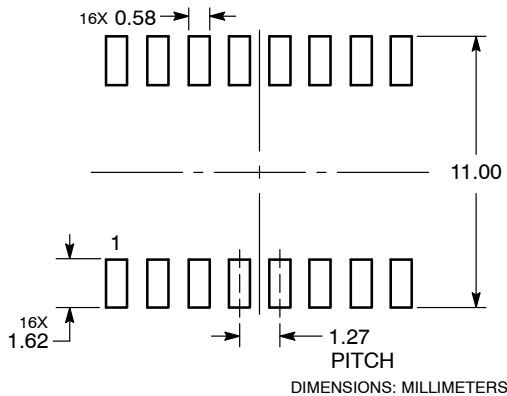


#### NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
q	0°	7°

#### SOLDERING FOOTPRINT



**onsemi, Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries. onsemi owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of onsemi's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marketing.pdf](http://www.onsemi.com/site/pdf/Patent-Marketing.pdf). onsemi reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and onsemi makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using onsemi products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by onsemi. "Typical" parameters which may be provided in onsemi data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. onsemi does not convey any license under any of its intellectual property rights nor the rights of others. onsemi products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use onsemi products for any such unintended or unauthorized application, Buyer shall indemnify and hold onsemi and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that onsemi was negligent regarding the design or manufacture of the part. onsemi is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

#### ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:  
 Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
 onsemi Website: [www.onsemi.com](http://www.onsemi.com)

ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)  
 For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)