1.2 V Dual Channel CMOS Buffer/Translator

NB3U23C

Description

The NB3U23C is a 2−input, 2−output buffer/voltage translator for UFS (Universal Flash Storage) in portable consumer applications such as mobile phones, tablets, cameras, etc. This dual channel CMOS buffer accepts 1.8 V CMOS input and translates it to 1.2 V CMOS output. The device is powered using single supply of 1.2 V ±5%.

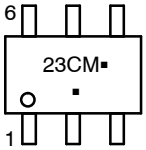
The NB3U23C is packaged in 2 ultra−small 6−pin packages: the 6 pin SC70 and a 6 pin thin UDFN package.

Features

- Operating Frequency: 52 MHz (Max)
- Propagation Delay: 5 ns (Max)
- Low Standby Current: < 10 μA at 1.2 V V_{DD}
- Low Phase Noise Floor: −150 dBc/Hz (Typ)
- Rise/Fall Times (tr/tf): 2 ns (Max)
- ESD Protection Exceeds JEDEC Standards
  - 2000 V Human−Body Model (JS−001−2012)
  - 200 V Machine Model (JESD22−A115C)
  - 1000 V Charged−Device Model (JESDC101E)
- Operating Supply Voltage Range (V_{DD}): 1.2 V ±5%
- Operating Temperature Range (Industrial): −40°C to 85°C
- These are Pb−Free Devices

MARKING DIAGRAMS

SC−70
SQ SUFFIX
CASE 419B



23C = Device Code
M = Date Code*
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

UDFN6
MN SUFFIX
CASE 517CW

C = Device Code
M = Date Code

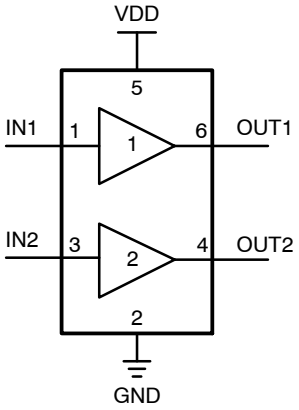


Figure 1. Simplified Logic Diagram

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 4.

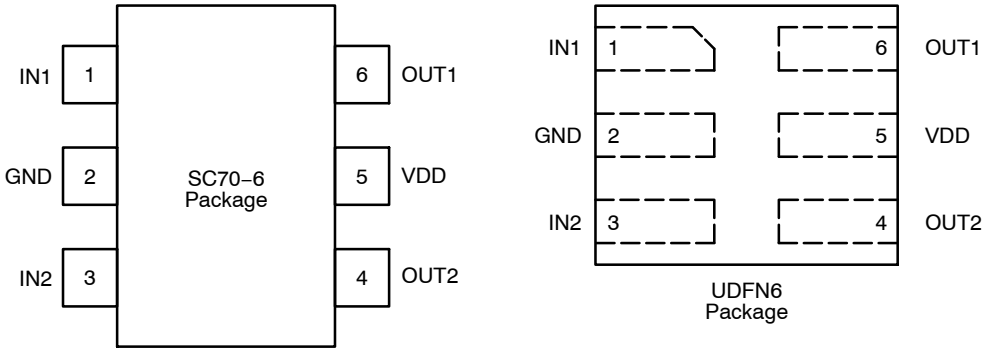


Figure 2. Pinout Diagram (Top Views)

Table 1. PIN DESCRIPTION

Number	Name	Description
1	IN1	Input Clock Signal − Channel 1
2	GND	Power Supply Ground (0 V)
3	IN2	Input Clock Signal − Channel 2
4	OUT2	Output − Channel 2
5	VDD	Power Supply Voltage
6	OUT1	Output − Channel 1

Table 2. ATTRIBUTES

Characteristic		Value
ESD Protection	Human Body Model Machine Model Charge Device Model	2 kV min 200 V min 1 kV min
Moisture Sensitivity (Note 1)		Level 1
Flammability Rating Oxygen Index: 28 to 34		UL 94 V−0 @ 0.125 in
Transistor Count		120
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test II		

1. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{DD}	Supply Voltage			3.6	V
V_{in}	Input Voltage			$-0.5 \le V_I \le 2.5$	V
I_D	Output Current			25	mA
T_A	Operating Temperature Range, Industrial			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm (Note 3) 0 lfpm 500 lfpm (Note 3)	SC70−6 UDFN−6	210 126 245 172	°C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 3)	SC70−6 UDFN−6	100 150	°C/W
T_{sol}	Wave Solder			260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.
3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power).

Table 4. ELECTRICAL CHARACTERISTICS (V_{DD} = 1.2 ±5% V, GND = 0 V, T_A = −40°C to +85°C)

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
DIDD	Power Supply Current (Single Channel Switching @ 52 MHz)	C_L = 20 pF C_L = 5 pF C_L = 1 pF		2.5 1.5 1		mA
	Power Supply Current (Both Channels Switching @ 52 MHz)	C_L = 20 pF C_L = 5 pF C_L = 1 pF		5 3 2		mA
I_{off}	Standby Current	Vi = V_{IH} Max or GND; V_{DD} = 1.2 V, No Output Load			10	μA
V_{IH}	Input High Voltage		0.65 * VDD		1.98	V
V_{IL}	Input Low Voltage		0		0.35 * VDD	V
V_{OH}	Output High Voltage	C_L = 20 pF R_L = 100 kΩ	0.75 * VDD		VDD	V
V_{OL}	Output Low Voltage	C_L = 20 pF R_L = 100 kΩ	0		0.25 * VDD	V
C_{in}	Input Capacitance				5	pF
F_{clk}	Operating Frequency Range		0		52	MHz
t_{PD}	Propagation Delay	INx to OUTx C_L = 20 pF, R_L = 100 kΩ			5	ns
	Phase Noise Floor Density (Notes 4 and 5)	C_L = 20 pF R_L = 100 kΩ		−150		dBc/Hz
	Additive RMS Phase Jitter (Notes 5 and 6)	C_L = 20 pF R_L = 100 kΩ Offset Frequency Range: 50 kHz to 10 MHz		0.15	0.25	ps
DC	Output Duty Cycle (Note 7)	Input Duty Cycle = 50%, Min Input Slew Rate = 1 V/ns	45		55	%
tr/tf	Output Rise/Fall Times	0.2 * V_{DD} to 0.8 * VDD C_L = 20 pF R_L = 100 kΩ			2	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. White noise floor.
5. This parameter refers to the random jitter only.
6. The output RMS phase jitter can be calculated using the following equation:
   $(\text{Output RMS Phase Jitter})^2 = (\text{Input RMS Phase Jitter})^2 + (\text{Additive RMS Phase Jitter})^2$
7. Measured with input voltage swing from 0 V to 1.8 V.

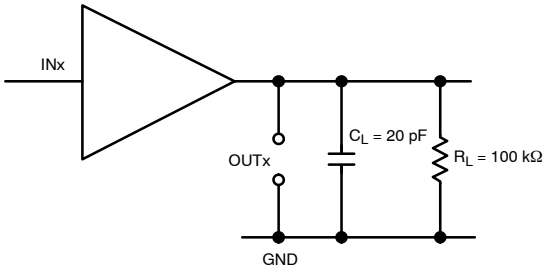


Figure 3. Typical Test Setup for Evaluation

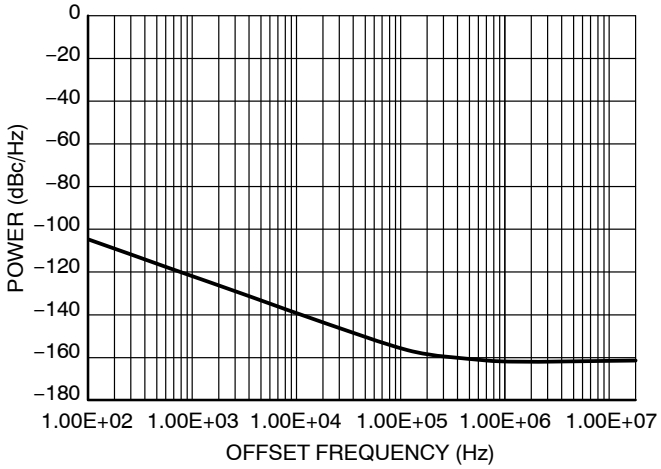


Figure 4. Typical Phase Noise Plot at 50 MHz Carrier Frequency

ORDERING INFORMATION

Device	Package	Shipping†
NB3U23CMNTAG	UDFN6 (Pb−Free)	3,000 / Tape & Reel

DISCONTINUED (Note 8)

NB3U23CSQTCG	SC−70−6 (Pb−Free)	3,000 / Tape & Reel

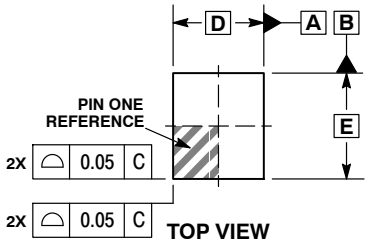
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

8. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

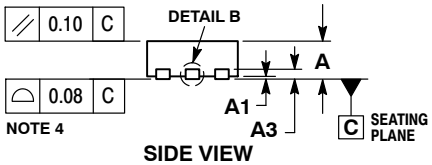
SCALE 4:1

UDFN6 1.2x1.4, 0.4P
CASE 517CW
ISSUE O

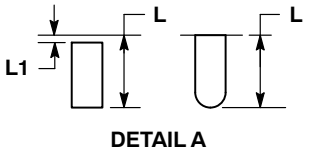
DATE 09 JAN 2014



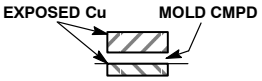
TOP VIEW



SIDE VIEW



DETAIL A
OPTIONAL TERMINAL CONSTRUCTIONS



DETAIL B
OPTIONAL CONSTRUCTION

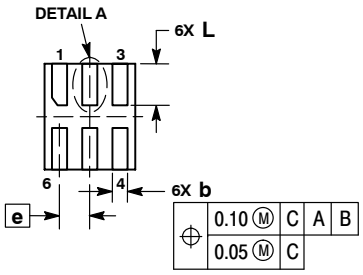
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	1.20 BSC	
E	1.40 BSC	
e	0.40 BSC	
L	0.50	0.60
L1	---	0.15

GENERIC MARKING DIAGRAM*

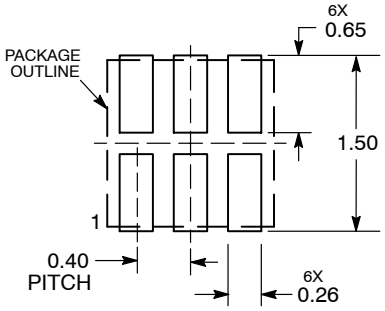
X = Specific Device Code
M = Month Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.



BOTTOM VIEW

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**UDFN6 1.2X1.4, 0.4P**		**PAGE 1 OF 1**

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