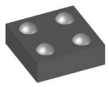
8 Kb I²C CMOS Serial EEPROM with 1.2 V I/Os

N24C008



WLCSP4, 0.75 x 0.75 x 0.3
CASE 567GG

Description

The N24C008 is an 8 Kb Serial CMOS EEPROM, internally organized as 1,024 words of 8 bits each. These devices feature a 16−byte page write buffer and support both the Standard (100 kHz), Fast (400 kHz) and Fast−Plus (1 MHz) I²C protocol.

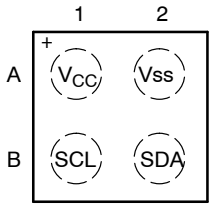
The devices also feature a 128−bit factory−set read−only Unique ID, a 16−byte Secure Data Page that can be permanently locked against future changes, and Software Write Protection of the entire array.

A Device Configuration Register enables the user to specify the last 1 bit of the Device Address, allowing up to two N24C008 devices to be addressed on the same bus.

Features

- Supports Standard, Fast and Fast−Plus I²C Protocol
- SCL and SDA are referred to 1.2 V
- 1.4 V (Min) to 2.2 V (Max) Supply Voltage Range
- 16 Byte Page Write Buffer
- Lockable Secure Data Page
- User Programmable Write Protection
- User Programmable Device Address
- Schmitt Triggers and Noise Suppression Filters on I²C Bus Inputs
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Industrial Temperature Range: −40°C to +85°C
- Ultra−thin 4−ball WLCSP Package
- This Device is Pb−Free, Halogen Free/BFR Free and RoHS Compliant*

PIN CONFIGURATION

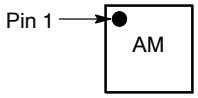


WLCSP4
(Top View)

PIN FUNCTION

Pin Name	Function
SDA	Serial Data Input/Output
SCL	Serial Clock Input
V_{CC}	Power Supply
V_{SS}	Ground

MARKING DIAGRAM



A = Specific Device Code
M = Month Code

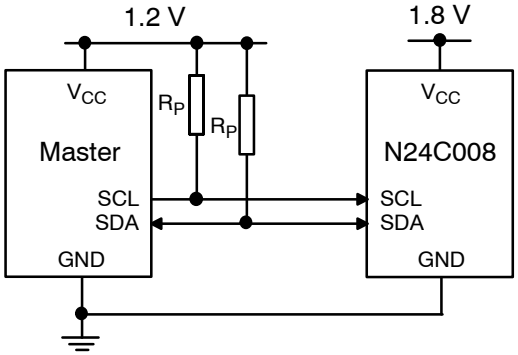


Figure 1. Typical Application

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Storage Temperature Range	−65 to +150	°C
Operational Temperature Range	−40 to +85	°C
Voltage on Any Pin with Respect to Ground (Note 1)	−0.5 to +3.6	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The DC input voltage on any pin should not be lower than −0.5 V or higher than V_{CC} + 1.0 V. During transitions, the voltage on any pin may undershoot to no less than −1.5 V or overshoot to no more than V_{CC} + 1.5 V, for periods of less than 20 ns.

Table 2. RELIABILITY CHARACTERISTICS (Note 2)

Symbol	Parameter	Min	Unit
N_{END} (Note 3)	Endurance	1,000,000	Program/Erase Cycles
T_{DR} (Note 4)	Data Retention	100	Years

2. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
3. Page Mode, V_{CC} = 1.4 V, 25°C
4. T_A = 25°C

Table 3. DC AND AC OPERATING CHARACTERISTICS

Supply Voltage / Temperature Range	Operation
V_{CC} = 1.4 V to 2.2 V, T_A = −40°C to +85°C	READ / WRITE

Table 4. D.C. OPERATING CHARACTERISTICS
(V_{CC} = 1.4 V to 2.2 V, T_A = −40°C to 85°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Max	Unit
I_{CCR}	Read Current	Read, f_{SCL} = 400 kHz/1 MHz		1	mA
I_{CCW}	Write Current			2.5	mA
I_{SB}	Standby Current	All I/O Pins at GND or V_{CC} T_A = −40 to 85°C		1	μA
I_L	I/O Pin Leakage	Pin at GND or V_{CC}		2	μA
V_{IL}	Input Low Voltage		−0.5	0.24	V
V_{IH}	Input High Voltage		0.96	2.2	V
V_{HYS}	Input Hysteresis		100		mV
V_{OL1}	Output Low Voltage	V_{CC} > 1.7 V, I_{OL} = 3.0 mA		0.4	V
V_{OL2}	Output Low Voltage	$V_{CC} \leq$ 1.7 V, I_{OL} = 1.0 mA		0.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 5. PIN IMPEDANCE CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN} (Note 5)	SDA I/O Pin Capacitance	V_{IN} = 0 V		8	pF
C_{IN} (Note 5)	Input Capacitance (other pins)	V_{IN} = 0 V		6	pF

5. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.

Table 6. A.C. CHARACTERISTICS (V_{CC} = 1.4 V to 2.2 V, T_A = −40°C to 85°C) (Note 6)

Symbol	Parameter	Standard		Fast		Fast−Plus		Unit
		Min	Max	Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400		1,000	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6		0.26		μs
t_{LOW}	Low Period of SCL Clock	4.7		1.3		0.50		μs
t_{HIGH}	High Period of SCL Clock	4		0.6		0.26		μs
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		0.26		μs
$t_{HD:DAT}$	Data In Hold Time	0		0		0		μs
$t_{SU:DAT}$	Data In Setup Time	250		100		50		ns
t_R (Note 7)	SDA and SCL Rise Time		1,000	20	300		100	ns
t_F (Note 7)	SDA and SCL Fall Time		300	20	300		100	ns
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		0.25		μs
t_{BUF}	Bus Free Time Between STOP and START	4.7		1.3		0.5		μs
t_{AA}	SCL Low to Data Out Valid		3.5		0.9		0.40	μs
t_{DH}	Data Out Hold Time	100		100		50		ns
T_i (Note 7)	Noise Pulse Filtered at SCL and SDA Inputs		50		50		50	ns
t_{WR}	Write Cycle Time		5		5		5	ms
t_{PU} (Notes 7, 8)	Power−up to Ready Mode		0.60		0.60		0.60	ms

6. Test conditions according to “A.C. Test Conditions” table.
7. Tested initially and after a design or process change that affects this parameter.
8. t_{PU} is the delay between the time V_{CC} is stable and the device is ready to accept commands.

Table 7. A.C. TEST CONDITIONS

Input Levels (V)	0.18 to 1.02
Input Rise and Fall Times	≤ 50 ns
Input Reference Levels (V)	0.24, 0.96
Output Reference Levels (V)	0.6
Output Load	Current Source: I_{OL} = 3 mA, C_L = 100 pF

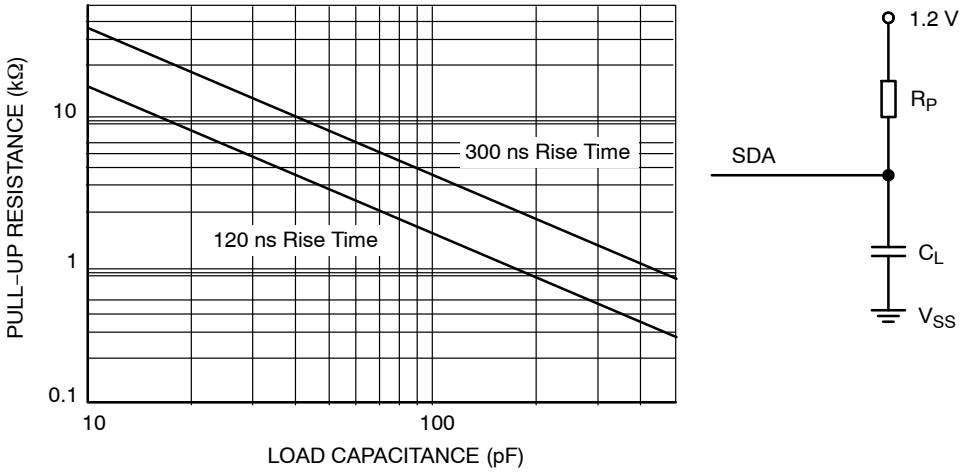


Figure 2. Maximum Pull−up Resistance vs. Load Capacitance at I/Os for Typical Applications

POWER−ON RESET (POR)

The N24C008 incorporates Power−On Reset (POR) circuitry which protects the device against powering up in the wrong state.

The N24C008 will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level. This bi−directional POR feature protects the device against "brown−out" failure following a temporary loss of power.

Pin Description

SCL: The Serial Clock input pin accepts the Serial Clock generated by the Master.

SDA: The Serial Data I/O pin receives input data and transmits data stored in EEPROM. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

Functional Description

The N24C008 supports the Inter-Integrated Circuit (I^2C) Bus data transmission protocol, which defines a device that sends data to the bus as a transmitter and a device receiving data as a receiver. Data flow is controlled by a Master device, which generates the serial clock and all START and STOP conditions. The N24C008 acts as a Slave device. Master and Slave alternate as either transmitter or receiver. Up to 2 devices may be connected to the bus as determined by the Device Address bit A2 in the Device Configuration Register.

I^2C Bus Protocol

The I^2C bus consists of two 'wires', SCL and SDA. The two wires are connected to the 1.2 V via pull−up resistors. Master and Slave devices connect to the 2−wire bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to 'transmit' a '0' and releases it to 'transmit' a '1'.

Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics).

During data transfer, the SDA line must remain stable while the SCL line is HIGH. An SDA transition while SCL is HIGH will be interpreted as a START or STOP condition (Figure 3). The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a 'wake−up' call to all receivers. Absent a START, a Slave will not respond to commands. The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH.

Device Addressing

The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8-bit serial Slave address. The first 4 bits of the Slave address are set to 1010, for normal Read/Write operations, and to 1011 for special Read/Write operations (Figure 4). The next bit must match the A2 bit in the Device Configuration Register. The next two bits are MSB's memory address. The last bit, R/W, specifies whether a Read (1) or Write (0) operation is to be performed.

The factory default for the A2 bit is 0.

Acknowledge

After processing the Slave address, the Slave responds with an acknowledge (ACK) by pulling down the SDA line during the 9^{th} clock cycle (Figure 5). The Slave will also acknowledge all address bytes and every data byte presented in Write mode if the addressed location is not write protected. In Read mode the Slave shifts out a data byte, and then releases the SDA line during the 9^{th} clock cycle. As long as the Master acknowledges the data, the Slave will continue transmitting. The Master terminates the session by not acknowledging the last data byte (NoACK) and by issuing a STOP condition. Bus timing is illustrated in Figure 6.

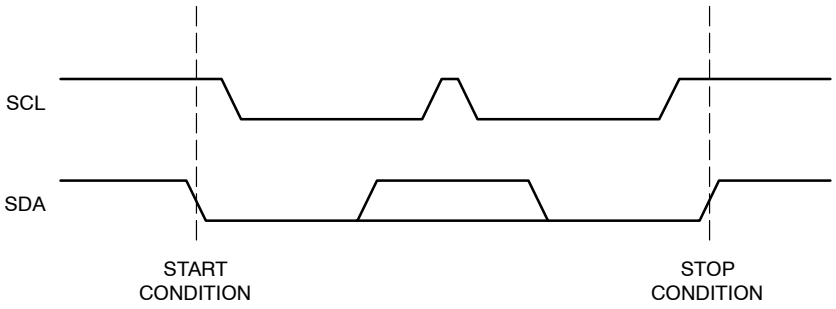


Figure 3. Start/Stop Conditions

	DEVICE ADDRESS							
Memory Array Access	1	0	1	0	A2	a9	a8	R/W
Secure Data Page, UID, Device Config.	1	0	1	1	A2	x	x	R/W

Figure 4. Slave Address Bits

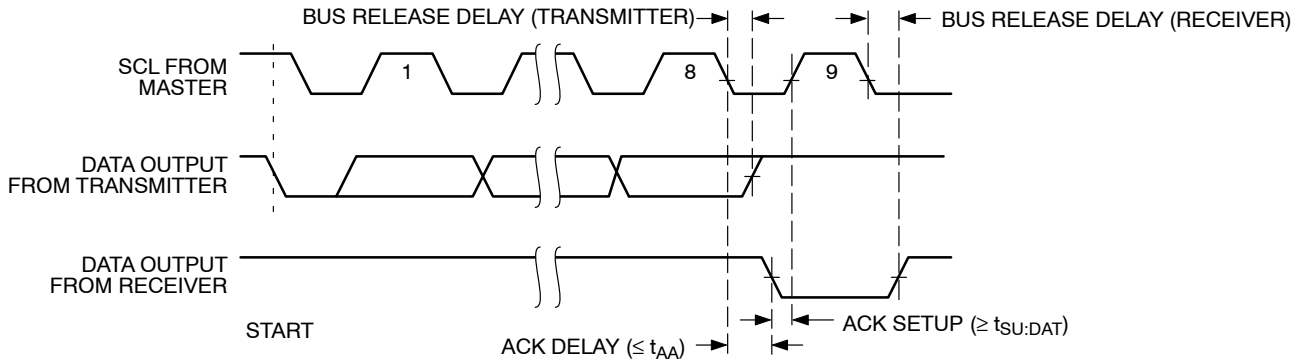


Figure 5. Acknowledge Timing

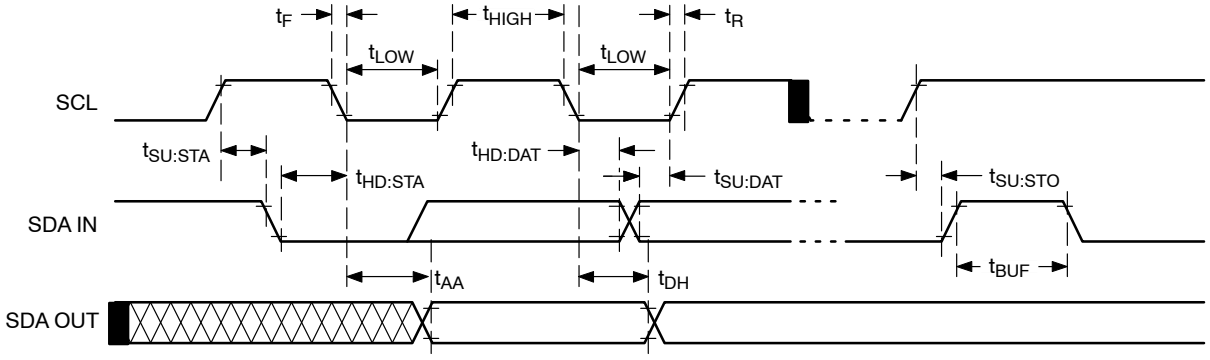


Figure 6. Bus Timing

WRITE OPERATIONS

Byte Write

In Byte Write mode the Master sends a START, followed by Slave address, one byte address (Table 8) and data to be written (Figure 7). The Slave, N24C008 acknowledges all 3 bytes, and the Master then follows up with a STOP, which in turn starts the internal Write operation (Figure 8). During the internal Write cycle (t_{WR}), the N24C008 will not acknowledge any Read or Write request from the Master.

Page Write

The N24C008 contains 1,024 bytes of data, arranged in 64 pages of 16 bytes each. A one byte address word (Table 8), following the Slave address, points to the first byte to be written into the memory array. The most significant 6 bits form the address active bits (a9 to a4) identify the page and the last 4 bits (a3 to a0) identify the byte within the page. Up to 16 bytes can be written in one Write cycle (Figure 9). The internal byte address counter is automatically incremented after each data byte is loaded. If the Master transmits more than 16 data bytes, then earlier bytes will be overwritten by later bytes in a 'wrap-around' fashion (within the selected page). The internal Write cycle starts immediately following the STOP.

Acknowledge Polling

The ready/busy status of the N24C008 can be ascertained by sending Read or Write requests immediately following the STOP condition that initiated the internal Write cycle. As long as internal Write is in progress, the N24C008 will not acknowledge the Slave address.

The Device Configuration Register Write instruction does not support acknowledge polling. Following this instruction, the master must wait t_{WR} = 5 ms before sending a new instruction.

Secure Data Page Write

The Secure Data Page Write instruction is similar to a Page Write instruction. To address the Secure Data Page, the user must address the device with the header 1011b followed by the A2 bit that match the bits in the Device Configuration register.

The second byte consists of 00xx a3a2a1a0, where x is don't care. The last 4 bits indicate the address within the Secure Data Page.

The remainder of the instruction is identical to a normal Page Write.

Secure Data Page Lock

The Secure Data Page Lock instruction is similar to a Byte Write instruction. To lock the Secure Data Page against future changes, the user must address the device with the header 1011b followed by the A2 bit that match the bits in the Device Configuration register. The second byte consists of 10xx xxxx, where x is don't care.

The data byte following the address bytes must be all 1s (FFh). After this instruction is sent, the user will be able to read, but not to write the content of the Secure Data Page. Any write instructions to the Secure Data Page will return No ACK from the device.

Device Configuration Register Write

The Device Configuration Register Write instruction is similar to a Byte Write instruction. The user must address the device with the header 1011b followed by the A2 bit that match the bit in the Device Configuration register. The second byte consists of 11xx xxxx, where x is don't care. The data byte following the address will be written into the Device Configuration Register (see Table 9 for the position of each bit.) The A2 bit determines the Device Address.

The SWP bit is the Software Write Protection bit. When SWP is set to 1, the memory array, the Secure Data Page and the Device Configuration Register are protected against write operations. The A2 bit cannot be overwritten during a Device Configuration Register write operation if SWP is set to 1. The SWP bit alone can be changed to 0.

The Device Configuration Register Write instruction does not support acknowledge polling.

Table 8. BYTE ADDRESS

	Header				Slave Adrr.	A9	A8	R/W	A7	A6	A5	A4	A3	A2	A1	A0
Memory Array	1	0	1	0	A2	a9	a8	1/0	a7	a6	a5	a4	a3	a2	a1	a0
Secure Data Page	1	0	1	1	A2	x	x	1/0	0	0	x	x	a3	a2	a1	a0
Secure Page Lock Bit	1	0	1	1	A2	x	x	1/0	1	0	x	x	x	x	x	x
Unique ID Number	1	0	1	1	A2	x	x	1/0	0	1	x	x	0	0	0	0
Device Configuration	1	0	1	1	A2	x	x	1/0	1	1	x	x	x	x	x	x

Table 9. DEVICE CONFIGURATION REGISTER

b7	b6	b5	b4	b3	b2	b1	b0
A2	x	x	x	x	x	SWP	x

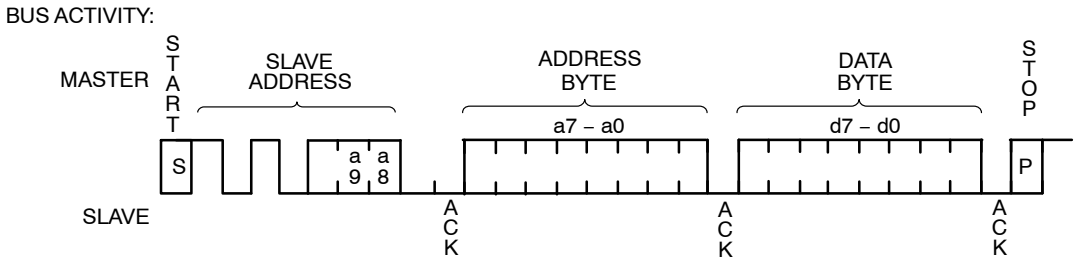


Figure 7. Byte Write Sequence

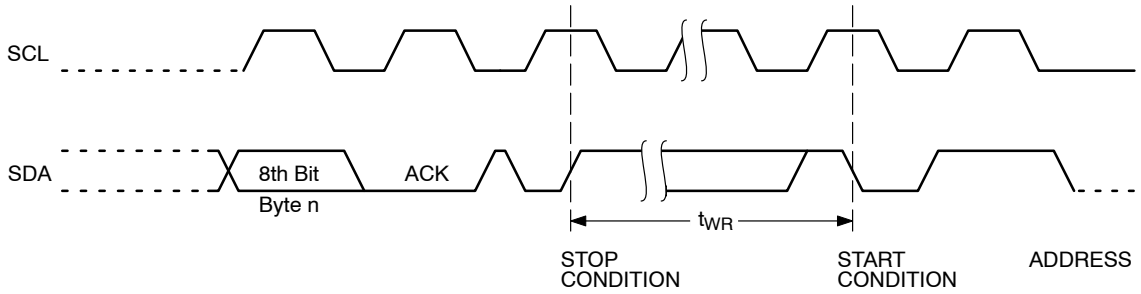


Figure 8. Write Cycle Timing

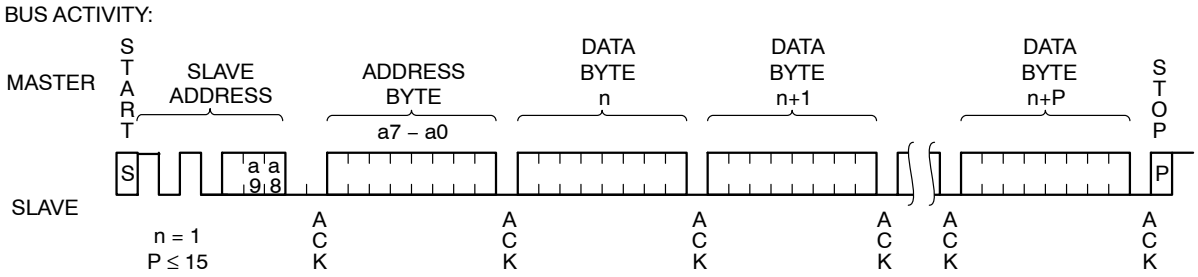


Figure 9. Page Write Sequence

READ OPERATIONS

Immediate Read

Upon receiving a Slave address with the R/W bit set to '1', the N24C008 will interpret this as a request for data residing at the current byte address in memory. The N24C008 will acknowledge the Slave address, will immediately shift out the data residing at the current address, and will then wait for the Master to respond. If the Master does not acknowledge the data (NoACK) and then follows up with a STOP condition (Figure 10), the N24C008 returns to Standby mode.

Selective Read

To read data residing at a specific location, the internal address counter must first be initialized as described under Byte Write. If rather than following up the address byte with data, the Master instead follows up with an Immediate Read sequence, then the N24C008 will use the 10 active address bits to initialize the internal address counter and will shift out data residing at the corresponding location. If the Master does not acknowledge the data (NoACK) and then follows up with a STOP condition (Figure 11), the N24C008 returns to Standby mode.

Sequential Read

If during a Read session the Master acknowledges the 1st data byte, then the N24C008 will continue transmitting data residing at subsequent locations until the Master responds with a NoACK, followed by a STOP (Figure 12). In contrast to Page Write, during Sequential Read the address count will automatically increment to and then wrap−around at end of memory (rather than end of page).

Secure Data Page Read

The Secure Data Page Read instruction is similar to a Sequential Read instruction. To read data from a specific location within the Secure Data Page, the address counter is initialized by sending the device header and the address byte as for a Secure Data Page Write instruction. This dummy write instruction is followed by an Immediate Read with the device header 1011b, and the device will shift back data from Secure Data Page. When the end of the Secure Data Page is reached, the address counter will wrap−around to zero, and the next byte returned will be the first byte in the page.

Device Configuration Register Read

The Device Configuration Register Read instruction is similar to a Selective Read instruction. The user must send the device header and the address byte as for a Device Configuration Register Write instruction. This dummy write instruction is followed by an Immediate Read with the device header 1011b, and the device will shift back the content of the Device Configuration Register. Don't care bits are read as 1s.

If the master acknowledges the data byte, requesting more data, the device will continue to return the content of the Device Configuration Register until the master responds with a NoACK.

Unique ID Number Read

The Unique ID Number Read instruction is similar to a Sequential Read instruction. The user must send the device header starting with 1011b followed by the A2 bit that match the bit in the Device Configuration register. As specified in Table 8, the second byte consists of 01xx 0000 where x is don't care. This dummy write instruction is followed by an Immediate Read with the device header 1011b, and the device will shift back the Unique ID byte by byte. The Unique ID is 16 bytes (128 bits) long. After the last byte of the Unique ID has been shifted, if the master acknowledges (requesting more data), the device will wrap−around and start returning the Unique ID from the beginning.

Secure Data Page Lock Status Read

There are two ways to check the lock status of the Security Sector. The first way is to initiate a Secure Data Page Write. The EEPROM will acknowledge if the Secure Data Page is unlocked, and it will not acknowledge if the Secure Data Page is locked. After the acknowledge bit, it is recommended to generate a Start condition followed by a Stop condition, to reset the interface.

The second way is to use a Lock Status Read instruction. This instruction is similar to a Selective Read instruction, but requires the use of the device address 1011b followed by the A2 bit. The master first sends a dummy write instruction followed by the address byte specified in Table 8 (10xx xxxx where x is don't care). This is followed by a read instruction using the same device address as above. The device will return a data byte where Bit 1 indicates the lock status. If the lock is active this bit is "1", otherwise it is "0".

Delivery State

The N24C008 is shipped erased, i.e., all memory array bytes are FFh, and the settable Device Configuration bits set to 0 (7Dh).

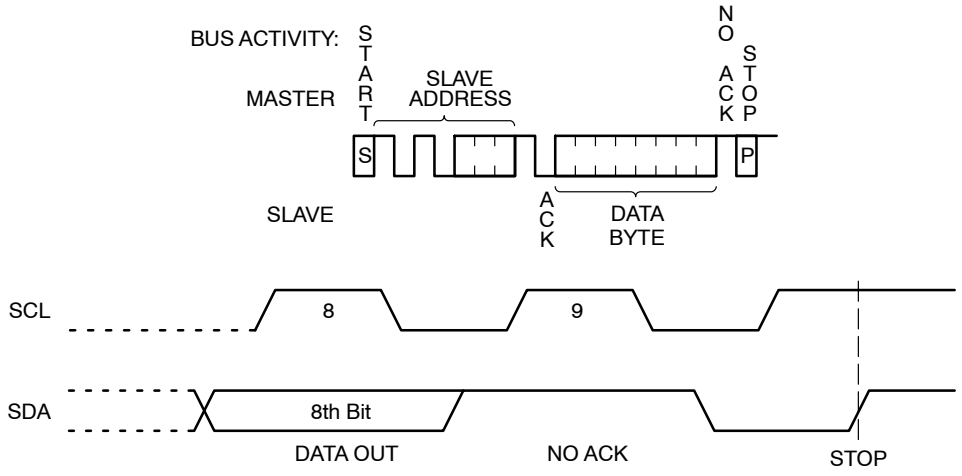


Figure 10. Immediate Read Sequence and Timing

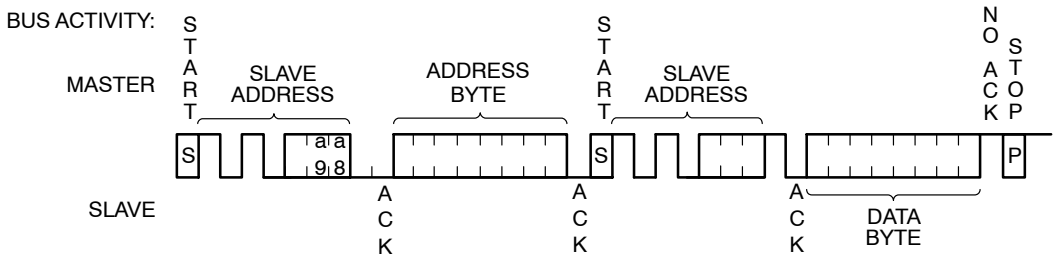


Figure 11. Selective Read Sequence

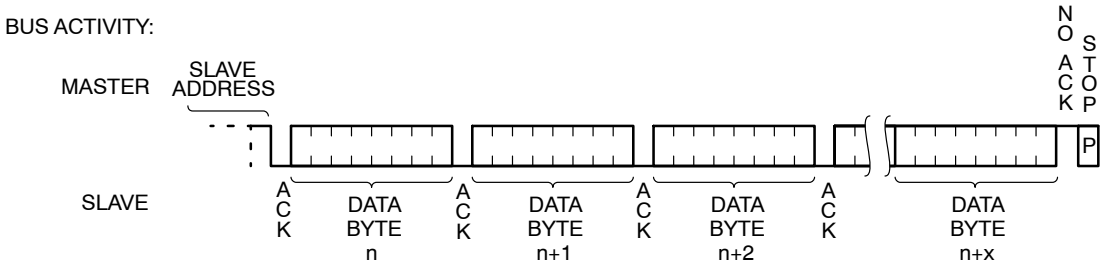


Figure 12. Sequential Read Sequence

ORDERING INFORMATION (Notes 9 thru 11)

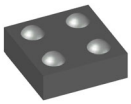
Device Order Number	Specific Device Marking	Package Type	Temperature Range	Shipping†
N24C008C4DTG	A	WLCSP 4−ball	Industrial (−40°C to +85°C)	Tape & Reel, 5,000 Units / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

9. All packages are RoHS−compliant (Lead−free, Halogen−free).
10. For detailed information and a breakdown of device nomenclature and numbering systems, please see the **onsemi** Device Nomenclature document, TND310/D, available at www.onsemi.com
11. **Caution: The EEPROM devices delivered in WLCSP must never be exposed to ultra violet light. When exposed to ultra violet light the EEPROM cells lose their stored data.**

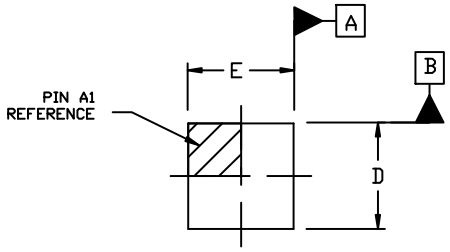
onsemi is licensed by Philips Corporation to carry the I^2C Bus Protocol.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

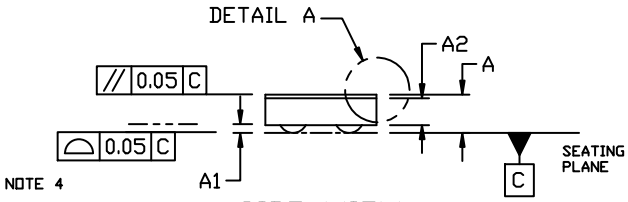


WLCSP4 0.75x0.75x0.3
CASE 567GG
ISSUE A

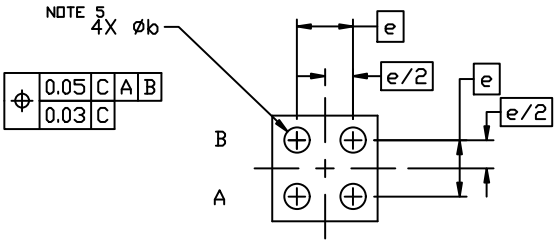
DATE 19 JAN 2023



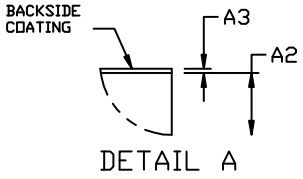
TOP VIEW



SIDE VIEW



BOTTOM VIEW



DETAIL A

NOTES:

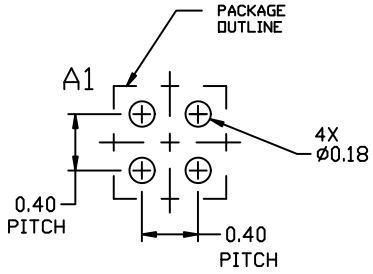
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM CONTACT BALL DIAMETER PARALLEL TO DATUM C.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	---	---	0.30
A1	0.04	0.06	0.08
A2		0.19 REF	
A3		0.025 REF	
b	0.16	0.18	0.20
D	0.73	0.75	0.78
E	0.73	0.75	0.78
e		0.40 BSC	

GENERIC MARKING DIAGRAM*

X = Specific Device Code
M = Month Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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