

Silicon Power Transistors

MJL21193 (PNP), **MJL21194 (NPN)**

The MJL21193 and MJL21194 utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

Features

- Total Harmonic Distortion Characterized
- High DC Current Gain
- Excellent Gain Linearity
- High SOA
- These Devices are Pb-Free and are RoHS Compliant*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	250	Vdc
Collector-Base Voltage	V_{CBO}	400	Vdc
Emitter-Base Voltage	V_{EBO}	5	Vdc
Collector-Emitter Voltage - 1.5 V	V_{CEX}	400	Vdc
Collector Current - Continuous	Ic	16	Adc
Collector Current - Peak (Note 1)	I _{CM}	30	Adc
Base Current - Continuous	Ι _Β	5	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	P _D	200 1.43	W W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤2%

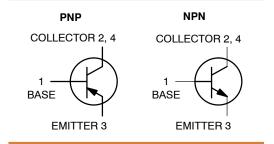
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.7	°C/W

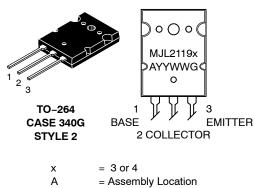
*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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16 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 250 VOLTS, 200 WATTS



MARKING DIAGRAM



= Year

WW = Work Week = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping [†]
MJL21193G	TO-264 (Pb-Free)	25 Units / Rail
MJL21194G	TO-264 (Pb-Free)	25 Units / Rail

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS	•				
Collector–Emitter Sustaining Voltage ($I_C = 100$ mAdc, $I_B = 0$)	V _{CEO(sus)}	250	-	-	Vdc
Collector Cutoff Current (V _{CE} = 200 Vdc, I _B = 0)	I _{CEO}	-	-	100	μAdc
Emitter Cutoff Current (V _{CE} = 5 Vdc, I _C = 0)	I _{EBO}	-	-	100	μAdc
Collector Cutoff Current (V _{CE} = 250 Vdc, V _{BE(off)} = 1.5 Vdc)	I _{CEX}	-	_	100	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased (V _{CE} = 50 Vdc, t = 1 s (non-repetitive) (V _{CE} = 80 Vdc, t = 1 s (non-repetitive)	I _{S/b}	4.0 2.25	<u>-</u> -	_ _	Adc
ON CHARACTERISTICS			I		
DC Current Gain ($I_C = 8$ Adc, $V_{CE} = 5$ Vdc) ($I_C = 16$ Adc, $I_B = 5$ Adc)	h _{FE}	25 8	_ _	75 -	
Base-Emitter On Voltage (I _C = 8 Adc, V _{CE} = 5 Vdc)	V _{BE(on)}	-	_	2.2	Vdc
Collector–Emitter Saturation Voltage ($I_C = 8$ Adc, $I_B = 0.8$ Adc) ($I_C = 16$ Adc, $I_B = 3.2$ Adc)	V _{CE(sat)}	- -	- -	1.4 4	Vdc
DYNAMIC CHARACTERISTICS					
Total Harmonic Distortion at the Output V _{RMS} = 28.3 V, f = 1 kHz, P _{LOAD} = 100 W _{RMS}	h _{FE}		0.8		%
(Matched pair h _{FE} = 50 @ 5 A/5 V)	h _{FE} tched	_	0.08	_	
Current Gain Bandwidth Product ($I_C = 1$ Adc, $V_{CE} = 10$ Vdc, $f_{test} = 1$ MHz)	f _T	4	-	-	MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f _{test} = 1 MHz)	C _{ob}	-	-	500	pF

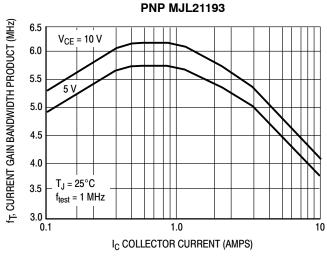


Figure 1. Typical Current Gain Bandwidth Product

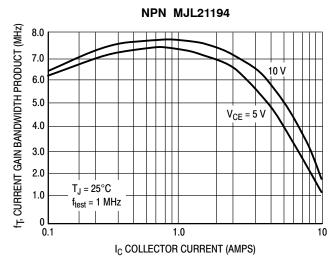


Figure 2. Typical Current Gain Bandwidth Product

TYPICAL CHARACTERISTICS

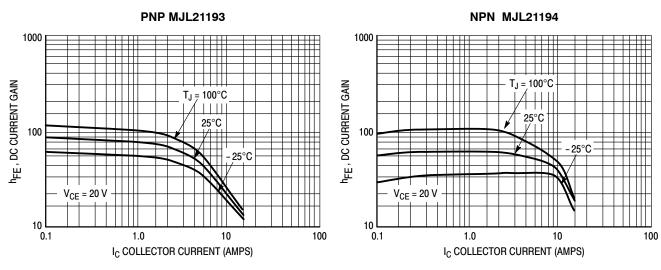


Figure 3. DC Current Gain, V_{CE} = 20 V

Figure 4. DC Current Gain, V_{CE} = 20 V

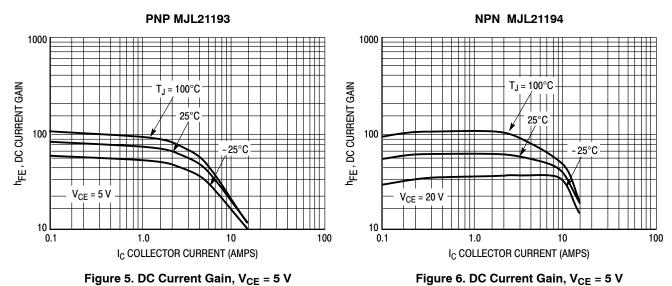


Figure 5. DC Current Gain, V_{CE} = 5 V

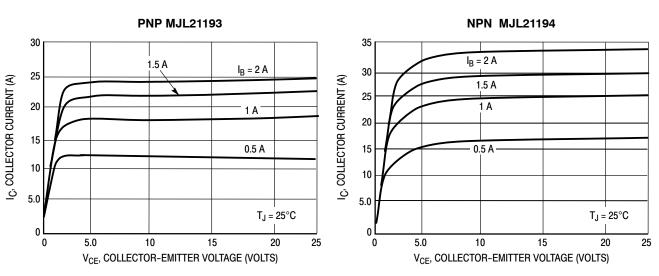


Figure 7. Typical Output Characteristics

Figure 8. Typical Output Characteristics

TYPICAL CHARACTERISTICS

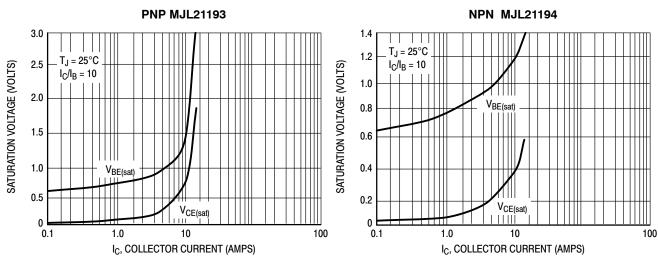


Figure 9. Typical Saturation Voltages

Figure 10. Typical Saturation Voltages

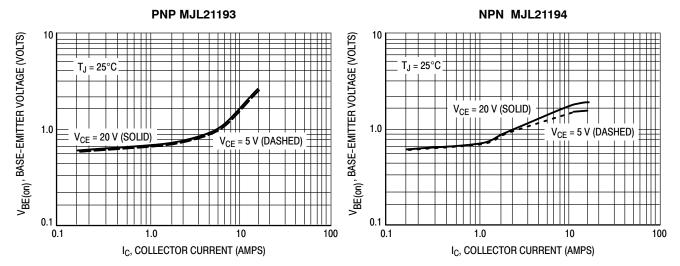


Figure 11. Typical Base-Emitter Voltage

Figure 12. Typical Base-Emitter Voltage

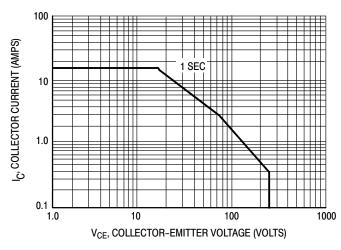


Figure 13. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_{J(pk)} = 150^{\circ} C$; T_{C} is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

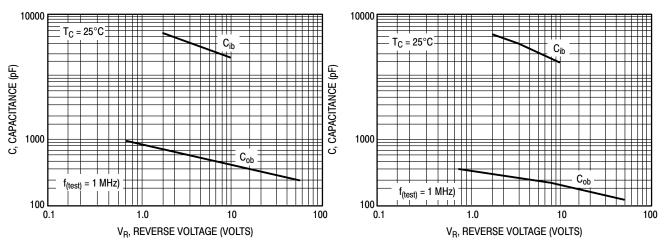


Figure 14. MJL21193 Typical Capacitance

Figure 15. MJL21194 Typical Capacitance

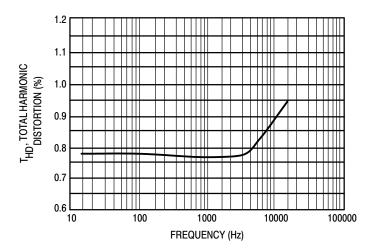


Figure 16. Typical Total Harmonic Distortion

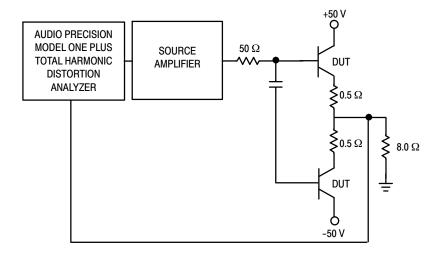
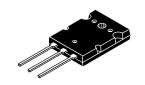


Figure 17. Total Harmonic Distortion Test Circuit

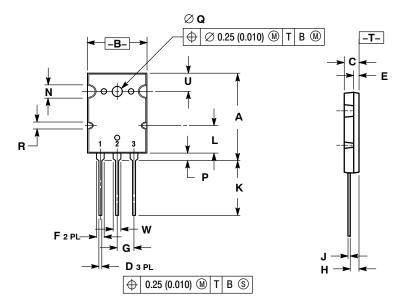




TO-3BPL (TO-264) CASE 340G-02 **ISSUE J**

DATE 17 DEC 2004

SCALE 1:2



NOTES:

- 1. DIMENSIONING AND TOLERANCING PER
- ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	28.0	29.0	1.102	1.142	
В	19.3	20.3	0.760	0.800	
С	4.7	5.3	0.185	0.209	
D	0.93	1.48	0.037	0.058	
E	1.9	2.1	0.075	0.083	
F	2.2	2.4	0.087	0.102	
G	5.45	5.45 BSC		0.215 BSC	
Н	2.6	3.0	0.102	0.118	
J	0.43	0.78	0.017	0.031	
K	17.6	18.8	0.693	0.740	
L	11.2 REF		0.411	REF	
N	4.35 REF		0.172	REF	
P	2.2	2.6	0.087	0.102	
Q	3.1	3.5	0.122	0.137	
R	2.25 REF		0.089	REF	
U	6.3 REF		0.248	REF	
W	2.8	3.2	0.110	0.125	

GENERIC MARKING DIAGRAM*

STYLE 1	:
PIN 1.	GATE
2.	DRAIN
3.	SOURCE

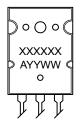
STYLE 2: PIN 1. BASE 2. COLLECTOR

EMITTER

STYLE 3: PIN 1. GATE 2. SOURCE DRAIN

STYLE 4: PIN 1. DRAIN 2. SOURCE GATE 3.

STYLE 5: PIN 1. GATE 2. COLLECTOR EMITTER



XXXXXX = Specific Device Code

Α = Location Code

YY = Year WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present.

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