

Octal D-Type Latch with 3-State Output

MC74VHC573, MC74VHCT573A

The MC74VHC573/MC74VHCT573A is an advanced high speed CMOS octal latch with 3-state output fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The 8-bit D-type latch is controlled by a latch enable input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

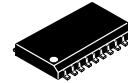
The MC74VHC573 inputs are compatible with standard CMOS levels while the MC74VHCT573A inputs are compatible with TTL levels. The MC74VHCT573A device can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5.0 V CMOS level output swings.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The MC74VHC573 and MC74VHCT573A inputs tolerate voltages up to 5.5 V, allowing the interface of 5 V systems to 3 V systems.

The MC74VHCT573A output structures provide protection when $V_{CC} = 0$ V. These output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

Features

- High Speed: $t_{PD} = 4.5$ ns (Typ) at $V_{CC} = 5.0$ V (VHC)
 $t_{PD} = 7.7$ ns (Typ) at $V_{CC} = 5.0$ V (VHCT)
- Low Power Dissipation: $I_{CC} = 4.0$ μ A (Max) at $T_A = 25^\circ$ C
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\%$
- Power Down Protection Provided
- Balanced Propagation Delays
- Designed for: 2.0 V to 5.5 V (VHC)
4.5 V to 5.5 V (VHCT)
- Low Noise: $V_{OLP} = 1.2$ V (Max) (VHC)
 $V_{OLP} = 1.6$ V (Max) (VHCT)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 100 mA
- ESD Performance: Human Body Model > 2000 V;
- Chip Complexity: 234 FETs or 58.5 Equivalent Gates
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

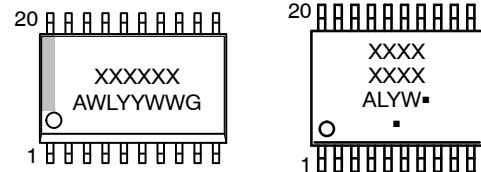


SOIC-20
DW SUFFIX
CASE 751D



TSSOP-20
DT SUFFIX
CASE 948E

MARKING DIAGRAMS



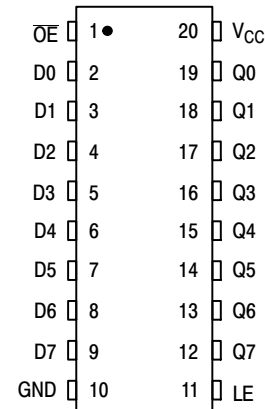
SOIC-20

TSSOP-20

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

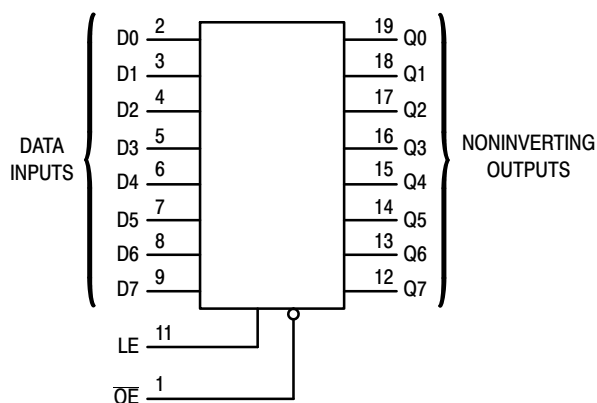
PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

MC74VHC573, MC74VHCT573A



FUNCTION TABLE

INPUTS			OUTPUT
OE	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

Figure 1. Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to +6.5	V
V_{IN}	DC Input Voltage	-0.5 to +6.5	V
V_{OUT}	DC Output Voltage (MC74VHC)	-0.5 to $V_{CC}+0.5$	V
	DC Output Voltage (MC74VHCT) Active Mode (High or Low State)	-0.5 to $V_{CC}+0.5$	
	Tristate Mode (Note 1)	-0.5 to +6.5	
	Power-Off Mode ($V_{CC} = 0$ V)	-0.5 to +6.5	
I_{IN}	DC Input Current, per Pin	± 20	mA
I_{OUT}	DC Output Current, Per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
I_{IK}	Input Clamp Current	-20	mA
I_{OK}	Output Clamp Current	MC74VHC ± 20	mA
		MC74VHCT -20	
T_{STG}	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
T_L	Lead Temperature, 1 mm from Case for 10 secs	260	$^{\circ}\text{C}$
T_J	Junction Temperature Under Bias	+150	$^{\circ}\text{C}$
θ_{JA}	Thermal Resistance (Note 2)	SOIC-20W 96	$^{\circ}\text{C}/\text{W}$
		TSSOP-20 150	
P_D	Power Dissipation in Still Air at 25 $^{\circ}\text{C}$	SOIC-20W 1302	mW
		TSSOP-20 833	
MSL	Moisture Sensitivity	SOIC-20W Level 3 All Other Packages Level 1	-
F_R	Flammability Rating	Oxygen Index: 28 to 34 UL 94 V-0 @ 0.573 in	-
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model 2000	V
		Charged Device Model N/A	
$I_{LATCHUP}$	Latchup Performance (Note 4)	± 100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.
4. Tested to EIA/JESD78 Class II.

MC74VHC573, MC74VHCT573A

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
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MC74VHC

V_{CC}	DC Supply Voltage	2.0	5.5	V
V_{IN}	DC Input Voltage (Note 5)	0	5.5	V
V_{OUT}	DC Output Voltage (Note 5)	0	V_{CC}	V
T_A	Operating Temperature	-55	+85	°C
t_r, t_f	Input Rise or Fall Rate	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ $V_{CC} = 4.5\text{ V to }5.5\text{ V}$	0 100 20	ns/V

MC74VHCT

V_{CC}	DC Supply Voltage	4.5	5.5	V
V_{IN}	DC Input Voltage (Note 5)	0	5.5	V
V_{OUT}	DC Output Voltage (Note 5)	Active Mode (High or Low State) Tristate Mode Power-Off Mode ($V_{CC} = 0\text{ V}$)	0 0 0	V_{CC} 5.5 5.5
T_A	Operating Temperature	-55	+85	°C
t_r, t_f	Input Rise or Fall Rate	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	0	20

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

MC74VHC573, MC74VHCT573A

DC ELECTRICAL CHARACTERISTICS (MC74VHC573)

Symbol	Parameter	Test Conditions	V _{CC} V	T _A = 25°C			T _A = - 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	Minimum High-Level Input Voltage		2.0 3.0 to 5.5	1.50 V _{CC} × 0.7			1.50 V _{CC} × 0.7		V
V _{IL}	Maximum Low-Level Input Voltage		2.0 3.0 to 5.5			0.50 V _{CC} × 0.3		0.50 V _{CC} × 0.3	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{OH} = - 50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V _{in} = V _{IH} or V _{IL} I _{OH} = - 4 mA I _{OH} = - 8 mA	3.0 4.5	2.58 3.94			2.48 3.80		
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{OL} = 50 μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V _{in} = V _{IH} or V _{IL} I _{OL} = 4mA I _{OL} = 8 mA	3.0 4.5			0.36 0.36		0.44 0.44	
I _{in}	Maximum Input Leakage Current	V _{in} = 5.5 V or GND	0 to 5.5			±0.1		±1.0	μA
I _{oz}	Maximum Three-State Leakage Current	V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	5.5			±0.25		±2.5	μA
I _{CC}	Maximum Quiescent Supply Current	V _{in} = V _{CC} or GND	5.5			4.0		40.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

MC74VHC573, MC74VHCT573A

AC ELECTRICAL CHARACTERISTICS (MC74VHC573)

Symbol	Parameter	Test Conditions	T _A = 25°C			T _A = - 40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, LE to Q	V _{CC} = 3.3 ± 0.3 V C _L = 15 pF C _L = 50 pF		7.6 10.1	11.9 15.4	1.0 1.0	14.0 17.5	ns
		V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF		5.0 6.5	7.7 9.7	1.0 1.0	9.0 11.0	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, D to Q	V _{CC} = 3.3 ± 0.3 V C _L = 15 pF C _L = 50 pF		7.0 9.5	11.0 14.5	1.0 1.0	13.0 16.5	ns
		V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF		4.5 6.0	6.8 8.8	1.0 1.0	8.0 10.0	
t _{PZL} , t _{PZH}	Output Enable Time, OE to Q	V _{CC} = 3.3 ± 0.3 V C _L = 15 pF C _L = 50 pF		7.3 9.8	11.5 15.0	1.0 1.0	13.5 17.0	ns
		V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF		5.2 6.7	7.7 9.7	1.0 1.0	9.0 11.0	
t _{PLZ} , t _{PHZ}	Output Disable Time, OE to Q	V _{CC} = 3.3 ± 0.3 V C _L = 50 pF		10.7	14.5	1.0	16.5	ns
		V _{CC} = 5.0 ± 0.5 V C _L = 50 pF		6.7	9.7	1.0	11.0	
t _{OSLH} , t _{OSHL}	Output to Output Skew	V _{CC} = 3.3 ± 0.3 V C _L = 50 pF (Note 6)			1.5		1.5	ns
		V _{CC} = 5.5 ± 0.5 V C _L = 50 pF (Note 6)			1.0		1.0	ns
C _{in}	Maximum Input Capacitance			4	10		10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Im- pedance State)			6				pF

C _{PD}	Power Dissipation Capacitance (Note 7)	Typical @ 25°C, V _{CC} = 5.0 V	pF
		29	

6. Parameter guaranteed by design. t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSHL} = |t_{PHLm} - t_{PHLn}|.
7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/8 (per latch). C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

NOISE CHARACTERISTICS (MC74VHC573) (C_L = 50 pF, V_{CC} = 5.0 V)

Symbol	Parameter	T _A = 25°C		Unit
		Typ	Max	
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	0.9	1.2	V
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	-0.9	-1.2	V
V _{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V _{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

TIMING REQUIREMENTS (MC74VHC573)

Symbol	Parameter	Test Conditions	T _A = 25°C		T _A = - 40 to 85°C	Unit
			Typ	Limit	Limit	
t _{w(h)}	Minimum Pulse Width, LE	V _{CC} = 3.3 ± 0.3 V V _{CC} = 5.0 ± 0.5 V		5.0 5.0	5.0 5.0	ns
t _{su}	Minimum Setup Time, D to LE	V _{CC} = 3.3 ± 0.3 V V _{CC} = 5.0 ± 0.5 V		3.5 3.5	3.5 3.5	ns
t _h	Minimum Hold Time, D to LE	V _{CC} = 3.3 ± 0.3 V V _{CC} = 5.0 ± 0.5 V		1.5 1.5	1.5 1.5	ns

MC74VHC573, MC74VHCT573A

DC ELECTRICAL CHARACTERISTICS (MC74VHCT573A)

Symbol	Parameter	Test Conditions	V _{CC} V	T _A = 25°C			T _A = - 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	Minimum High-Level Input Voltage		4.5 to 5.5	2.0			2.0		V
V _{IL}	Maximum Low-Level Input Voltage		4.5 to 5.5			0.8		0.8	V
V _{OH}	Minimum High-Level Output Voltage V _{in} = V _{IH} or V _{IL}	I _{OH} = - 50 µA	4.5	4.4	4.5		4.4		V
		I _{OH} = - 8 mA	4.5	3.94			3.80		
V _{OL}	Maximum Low-Level Output Voltage V _{in} = V _{IH} or V _{IL}	I _{OL} = 50 µA	4.5		0.0	0.1		0.1	V
		I _{OL} = 8 mA	4.5			0.36		0.44	
I _{in}	Maximum Input Leakage Current	V _{in} = 5.5 V or GND	0 to 5.5			± 0.1		±1.0	µA
I _{OZ}	Maximum 3-State Leakage Current	V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	5.5			± 0.25		±2.5	µA
I _{CC}	Maximum Quiescent Supply Current	V _{in} = V _{CC} or GND	5.5			4.0		40.0	µA
I _{CCT}	Quiescent Supply Current	Per Input: V _{IN} = 3.4 V Other Input: V _{CC} or GND	5.5			1.35		1.50	mA
I _{OPD}	Output Leakage Current	V _{OUT} = 5.5 V	0			0.5		5.0	µA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (MC74VHCT573A)

Symbol	Parameter	Test Conditions	T _A = 25°C			T _A = - 40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, LE to Q	V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF		7.7 8.5	12.3 13.3	1.0 1.0	13.5 14.5	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, D to Q	V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF		5.1 5.9	8.5 9.5	1.0 1.0	9.5 10.5	ns
t _{PZL} , t _{PZH}	Output Enable Time, OE to Q	V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF		6.3 7.1	10.9 11.9	1.0 1.0	12.5 13.5	ns
t _{PLZ} , t _{PHZ}	Output Disable Time, OE to Q	V _{CC} = 5.0 ± 0.5 V C _L = 50 pF		8.8	11.2	1.0	12.0	ns
t _{OSLH} , t _{OSHL}	Output to Output Skew	V _{CC} = 5.5 ± 0.5 V C _L = 50 pF (Note 8)			1.0		1.0	ns
C _{in}	Maximum Input Capacitance			4	10		10	pF
C _{out}	Maximum 3-State Output Capacitance (Output in High-Impedance State)			6				pF

C _{PD}	Power Dissipation Capacitance (Note 9)	Typical @ 25°C, V _{CC} = 5.0 V	pF
		25	

8. Parameter guaranteed by design. t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSHL} = |t_{PHLm} - t_{PHLn}|.
9. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/8 (per latch). C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

MC74VHC573, MC74VHCT573A

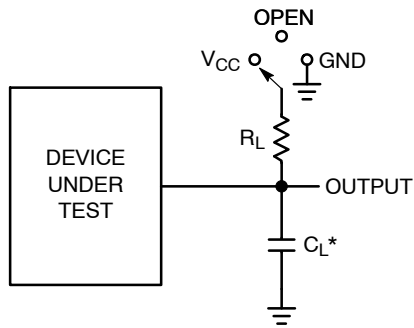
NOISE CHARACTERISTICS (MC74VHCT573A) ($C_L = 50 \text{ pF}$, $V_{CC} = 5.0 \text{ V}$)

Symbol	Parameter	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	1.2	1.6	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	-1.2	-1.6	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

TIMING REQUIREMENTS (MC74VHCT573A)

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$		$T_A = -40 \text{ to } 85^\circ\text{C}$	Unit
			Typ	Limit	Limit	
$t_{w(h)}$	Minimum Pulse Width, LE	$V_{CC} = 5.0 \pm 0.5\text{V}$		6.5	8.5	ns
t_{su}	Minimum Setup Time, D to LE	$V_{CC} = 5.0 \pm 0.5\text{V}$		1.5	1.5	ns
t_h	Minimum Hold Time, D to LE	$V_{CC} = 5.0 \pm 0.5\text{V}$		3.5	3.5	ns

MC74VHC573, MC74VHCT573A



* C_L Includes probe and jig capacitance
Input signal $t_R = t_F = 3$ ns

Test	Switch Position	C_L	R_L
t_{PLH} / t_{PHL}	Open	See AC Characteristics Table	1 k Ω
t_{PLZ} / t_{PZL}	V_{CC}		
t_{PHZ} / t_{PZH}	GND		

Figure 2. Test Circuits

SWITCHING WAVEFORMS

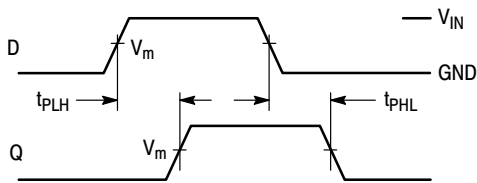


Figure 1.

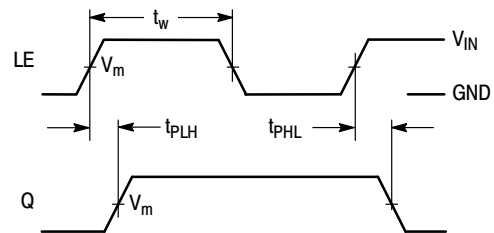


Figure 2.

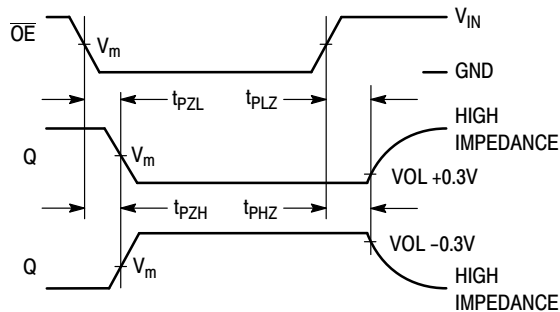


Figure 3.

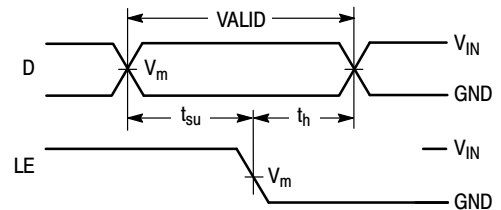


Figure 4.

Device	V_{IN} , V	V_m , V
MC74VHC573	V_{CC}	$50\% \times V_{CC}$
MC74VHCT573A	3 V	1.5 V

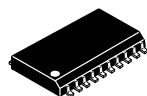
The diagram illustrates a 10-bit shift register implemented with ten D flip-flops. Each flip-flop has a data input (D), a clock input (Q), and a load enable input (LE). The inputs are as follows:

- Data Inputs (D):** D0 through D7 are connected to inverters with inputs 2 through 9. D8 and D9 are connected to inverters with inputs 11 and 1 respectively.
- Load Enable (LE):** A common LE input (11) is connected to the LE pin of every flip-flop.
- Output Enable (OE):** A common OE input (1) is connected to the OE pin of every flip-flop.
- Outputs (Q):** The Q outputs of the flip-flops are labeled 19 through 12, corresponding to Q0 through Q7. The outputs 11 and 1 are also labeled.

The circuit diagram shows a 4-bit parallel adder. It consists of two 74147 BCD-to-7-segment decoders and one 7447 BCD-to-7-segment decoder. The 74147 decoders are configured to take a 4-bit input (A, B, C, D) and produce a 7-bit output (S, C, and three other bits). The 7447 decoder is configured to take a 4-bit input (A, B, C, D) and produce a 7-bit output (S, C, and three other bits). The outputs of the 74147 decoders are connected to the inputs of the 7447 decoder. The 7447 decoder's outputs are connected to a 7-segment display. The 74147 decoders are also connected to a 7-segment display. The 7447 decoder is connected to a 7-segment display. The 74147 decoders are connected to a 7-segment display. The 7447 decoder is connected to a 7-segment display.

Device	Marking	Package	Shipping [†]
MC74VHC573DWR2G	VHC573G	SOIC–20 WB	1000 Units / Tape & Reel
MC74VHC573DTR2G	VHC 573	TSSOP–20	2500 Units / Tape & Reel
MC74VHCT573ADWR2G	VHCT573AG	SOIC–20 WB	1000 Units / Tape & Reel
MC74VHCT573ADTG	VHCT 573A	TSSOP–20	75 Units / Rail
MC74VHCT573ADTR2G	VHCT 573A	TSSOP–20	2500 Units / Tape & Reel

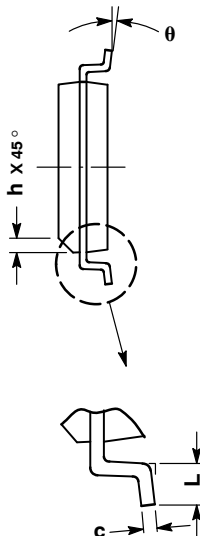
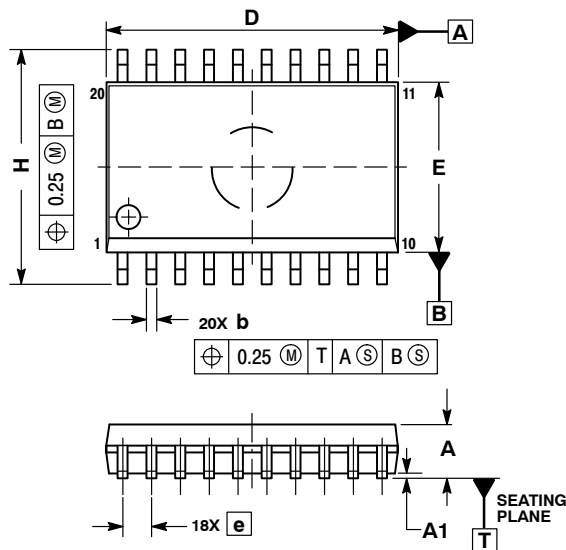
*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable



SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015

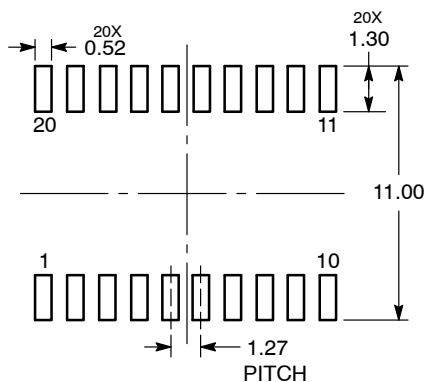


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

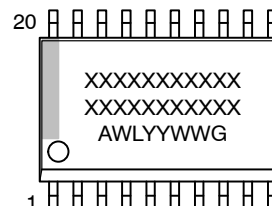
RECOMMENDED
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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