

Hex Inverter

MC74VHC04, MC74VHCT04A

The MC74VHC04 and MC74VHCT04A are high speed CMOS quad Inverters fabricated with silicon gate CMOS technology. These achieve high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHC04 inputs are compatible with standard CMOS levels while the MC74VHCT04A inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5.0 V CMOS level output swings.

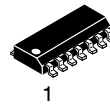
The MC74VHC04 and MC74VHCT04A internal circuits are composed of three stages, including a buffer output which provides high noise immunity and stable output. The input structures tolerate voltages up to 5.5 V, allowing the interface of 5 V systems to 3 V systems.

The MC74VHCT04A output structures provide protection when $V_{CC} = 0$ V. These output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

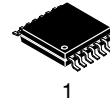
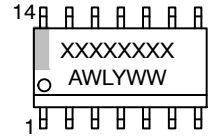
Features

- High Speed: $t_{PD} = 3.8$ ns (Typ) at $V_{CC} = 5$ V
- Low Power Dissipation: $I_{CC} = 2$ μ A (Max) at $T_A = 25^\circ$ C
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\%$ V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2 V to 5.5 V Operating Range
- Low Noise: $V_{OLP} = 0.8$ V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 100 mA
- ESD Performance: HBM > 2000 V
- Chip Complexity: 48 FETs or 12 Equivalent Gates
- –Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
- These Devices are Pb–Free and are RoHS Compliant

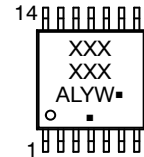
MARKING DIAGRAMS



SOIC–14
D SUFFIX
CASE 751A



TSSOP–14
DT SUFFIX
CASE 948G



XXXXXX = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or \blacksquare = Pb–Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

Inputs	Outputs
A	\bar{Y}
L	H
H	L

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

MC74VHC04, MC74VHCT04A

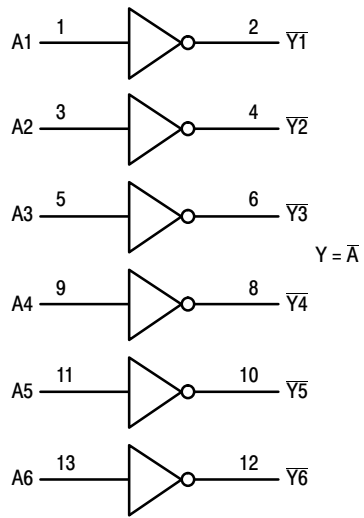


Figure 1. Logic Diagram

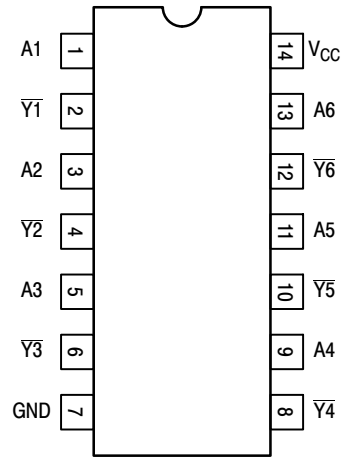


Figure 2. Pinout:
14-Lead Packages
(Top View)

MC74VHC04, MC74VHCT04A

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit	
V _{CC}	DC Supply Voltage	-0.5 to +6.5	V	
V _{in}	DC Input Voltage	-0.5 to +6.5	V	
V _{out}	DC Output Voltage (MC74VHC)	-0.5 to V _{CC} + 0.5	V	
	DC Output Voltage (MC74VHCT)	Active Mode (High or Low State)		-0.5 to V _{CC} + 0.5
		Tristate Mode (Note 1)		-0.5 to +6.5
	Power-Off Mode (V _{CC} = 0 V)	-0.5 to +6.5		
I _{IN}	DC Input Current, per Pin	±20	mA	
I _{OUT}	DC Output Current, Per Pin	±25	mA	
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA	
I _{IK}	Input Clamp Current	-20	mA	
I _{OK}	Output Clamp Current	MC74VHC	±20	mA
		MC74VHCT	-20	
T _{STG}	Storage Temperature Range	-65 to +150	°C	
T _L	Lead Temperature, 1 mm from Case for 10 secs	260	°C	
T _J	Junction Temperature Under Bias	+150	°C	
θ _{JA}	Thermal Resistance (Note 2)	SOIC-14	116	°C/W
		QFN14	130	
		TSSOP-14	150	
P _D	Power Dissipation in Still Air at 25°C	SOIC-14	1077	mW
		QFN14	962	
		TSSOP-20	833	
MSL	Moisture Sensitivity	Level 1	-	
F _R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	-
V _{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model	> 2000	V
		Charged Device Model	N/A	
I _{LATCHUP}	Latchup Performance (Note 4)	±100	mA	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.

2. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.

3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

4. Tested to EIA/JESD78 Class II.

MC74VHC04, MC74VHCT04A

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
MC74VHC				
V_{CC}	DC Supply Voltage	2.0	5.5	V
V_{in}	DC Input Voltage (Note 5)	0	5.5	V
V_{out}	DC Output Voltage (Note 5)	0	V_{CC}	V
T_A	Operating Temperature	-55	+125	°C
t_r, t_f	Input Rise or Fall Rate	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ $V_{CC} = 4.5\text{ V to }5.5\text{ V}$	100 20	ns/V

MC74VHCT

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	5.5	V
V_{IN}	DC Input Voltage (Note 5)	0	5.5	V
V_{OUT}	DC Output Voltage (Note 5)	Active Mode (High or Low State) Tristate Mode Power-Off Mode ($V_{CC} = 0\text{ V}$)	V_{CC} 5.5 5.5	V
T_A	Operating Temperature	-55	+125	°C
t_r, t_f	Input Rise or Fall Rate	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (MC74VHC04)

Symbol	Parameter	Test Conditions	V_{CC} V	$T_A = 25^\circ\text{C}$			$T_A = -40\text{ to }85^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High-Level Input Voltage		2.0 3.0 to 5.5	1.50 $V_{CC} \times 0.7$			1.50 $V_{CC} \times 0.7$		V
V_{IL}	Maximum Low-Level Input Voltage		2.0 3.0 to 5.5			0.50 $V_{CC} \times 0.3$	0.50 $V_{CC} \times 0.3$		V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $I_{OH} = -50\ \mu\text{A}$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		$V_{in} = V_{IH}$ or V_{IL} $I_{OH} = -4\text{ mA}$ $I_{OH} = -8\text{ mA}$	3.0 4.5	2.58 3.94		2.48 3.80			
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $I_{OL} = 50\ \mu\text{A}$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $I_{OL} = 4\text{ mA}$ $I_{OL} = 8\text{ mA}$	3.0 4.5			0.36 0.36	0.44 0.44		
I_{in}	Maximum Input Leakage Current	$V_{in} = 5.5$ or GND	0 to 5.5			± 0.1		± 0.1	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{in} = V_{CC}$ or GND	5.5			2.0		20.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

MC74VHC04, MC74VHCT04A

AC ELECTRICAL CHARACTERISTICS (MC74VHC04)

Symbol	Parameter	Test Conditions	T _A = 25°C			T _A = -40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, A to \bar{Y}	V _{CC} = 3.3 ± 0.3V C _L = 15 pF		5.0	7.1	1.0	8.5	ns
		C _L = 50 pF		7.5	10.6	1.0	12.0	
		V _{CC} = 5.0 ± 0.5V C _L = 15 pF		3.8	5.5	1.0	6.5	
		C _L = 50 pF		5.3	7.5	1.0	8.5	
C _{in}	Maximum Input Capacitance			4	10		10	pF

C _{PD}	Power Dissipation Capacitance (Per Inverter) (Note 6)	Typical @ 25°C, V _{CC} = 5.0 V		pF
		18		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/6 (per buffer). C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

NOISE CHARACTERISTICS (MC74VHC04, C_L = 50 pF, V_{CC} = 5.0 V)

Symbol	Characteristic	T _A = 25°C		Unit
		Typ	Max	
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	0.4	0.8	V
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	-0.4	-0.8	V
V _{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V _{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

MC74VHC04, MC74VHCT04A

DC ELECTRICAL CHARACTERISTICS (MC74VHCT04A)

Symbol	Parameter	Test Conditions	V _{CC} V	T _A = 25°C			T _A = - 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	Minimum High-Level Input Voltage		4.5 to 5.5	2.0			2.0		V
V _{IL}	Maximum Low-Level Input Voltage		4.5 to 5.5			0.8		0.8	V
V _{OH}	Minimum High-Level Output Voltage V _{in} = V _{IH} or V _{IL}	I _{OH} = - 50 μA	4.5	4.4	4.5		4.4		V
		I _{OH} = - 8 mA	4.5	3.94			3.80		
V _{OL}	Maximum Low-Level Output Voltage V _{in} = V _{IH} or V _{IL}	I _{OL} = 50 μA	4.5		0.0	0.1		0.1	V
		I _{OL} = 8 mA	4.5			0.36		0.44	
I _{in}	Maximum Input Leakage Current	V _{in} = 5.5 V or GND	0 to 5.5			±0.1		±1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{in} = V _{CC} or GND	5.5			2.0		20.0	μA
I _{CC} T	Quiescent Supply Current	Per Input: V _{IN} = 3.4 V Other Input: V _{CC} or GND	5.5			1.35		1.50	mA
I _{OPD}	Output Leakage Current	V _{OUT} = 5.5 V	0			0.5		5.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (MC74VHCT04A)

Symbol	Parameter	Test Conditions	T _A = 25°C			T _A = - 40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, A to Y	V _{CC} = 5.0 ± 0.5V C _L = 15 pF C _L = 50 pF		4.7 5.5	6.7 7.7	1.0 1.0	7.5 8.5	ns
C _{in}	Maximum Input Capacitance			4	10		10	pF

C _{PD}	Power Dissipation Capacitance (Note 7)	Typical @ 25°C, V _{CC} = 5.0 V		Unit
		11		
				pF

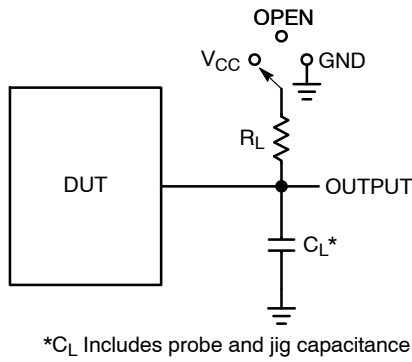
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/6 (per buffer). C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

NOISE CHARACTERISTICS (MC74VHCT04A, C_L = 50 pF, V_{CC} = 5.0 V)

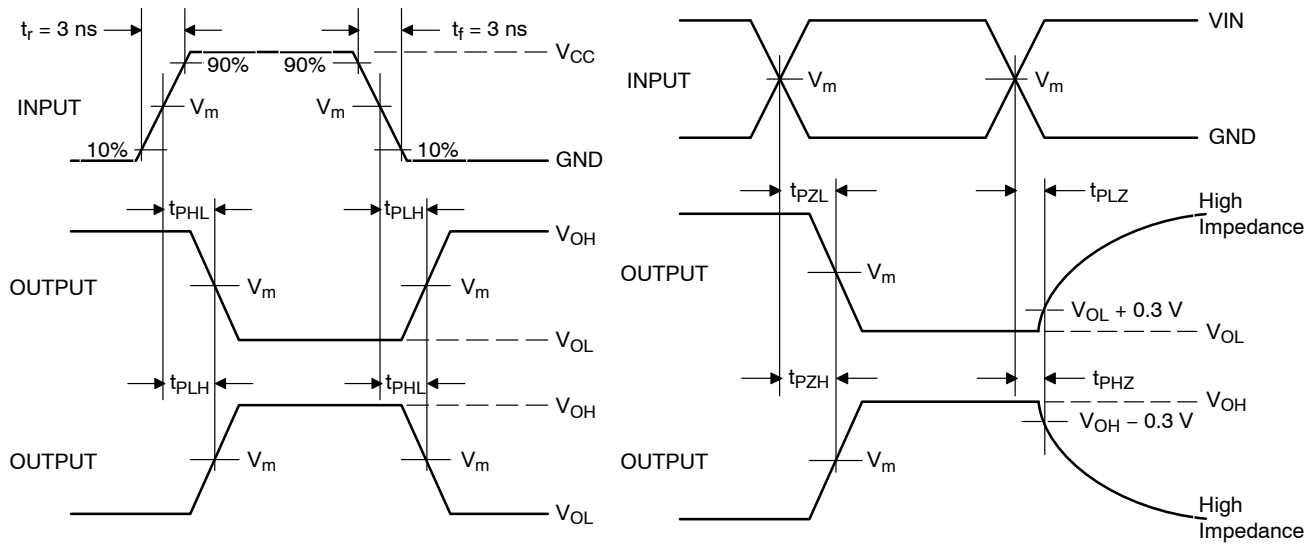
Symbol	Characteristic	T _A = 25°C		Unit
		Typ	Max	
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	0.8	1.0	V
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	-0.8	-1.0	V
V _{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V _{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

MC74VHC04, MC74VHCT04A



Test	Switch Position	C _L	R _L
t _{PLH} / t _{PHL}	Open	See AC Characteristics Table	1 kΩ
t _{PLZ} / t _{PZL}	V _{CC}		
t _{PHZ} / t _{PZH}	GND		

Figure 3. Test Circuit



Device	V _{IN} , V	V _m , V
MC74VHC04	V _{CC}	50% x V _{CC}
MC74VHCT04A	3 V	1.5 V

Figure 4. Switching Waveforms

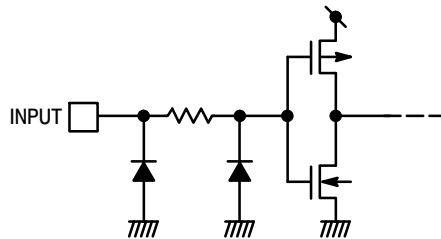


Figure 5. Input Equivalent Circuit

MC74VHC04, MC74VHCT04A

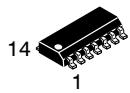
ORDERING INFORMATION

Device	Package	Marking	Shipping†
MC74VHC04DR2G	SOIC-14	VHC04G	2500 / Tape & Reel
MC74VHC04DTR2G	TSSOP-14	VHC 04	2500 / Tape & Reel
MC74VHC04DTR2G-Q*	TSSOP-14	VHC 04	2500 / Tape & Reel
MC74VHCT04ADR2G	SOIC-14	VHCT04AG	2500 / Tape & Reel
MC74VHCT04ADTR2G	TSSOP-14	VHCT 04A	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

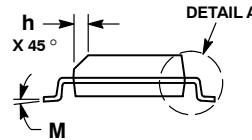
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-14 NB
CASE 751A-03
ISSUE L

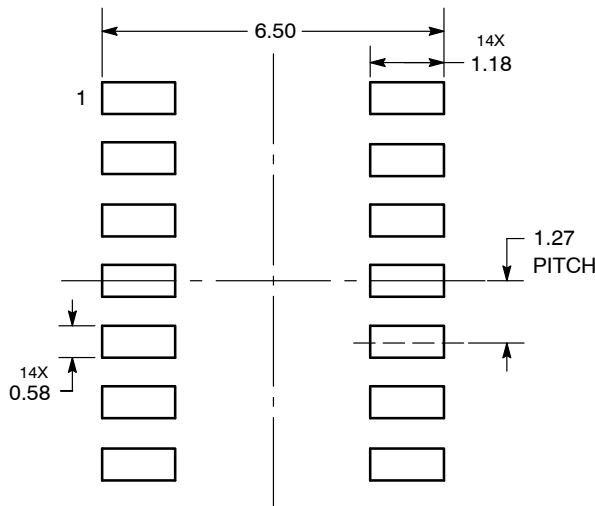
DATE 03 FEB 2016



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
 5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

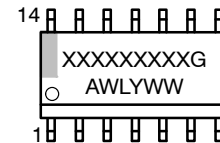
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42565B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-14 NB	PAGE 1 OF 2

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

SOIC-14
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. NO CONNECTION
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 2:
 CANCELLED

STYLE 3:
 PIN 1. NO CONNECTION
 2. ANODE
 3. ANODE
 4. NO CONNECTION
 5. ANODE
 6. NO CONNECTION
 7. ANODE
 8. ANODE
 9. ANODE
 10. NO CONNECTION
 11. ANODE
 12. ANODE
 13. NO CONNECTION
 14. COMMON CATHODE

STYLE 4:
 PIN 1. NO CONNECTION
 2. CATHODE
 3. CATHODE
 4. NO CONNECTION
 5. CATHODE
 6. NO CONNECTION
 7. CATHODE
 8. CATHODE
 9. CATHODE
 10. NO CONNECTION
 11. CATHODE
 12. CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 5:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. COMMON ANODE
 8. COMMON CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 6:
 PIN 1. CATHODE
 2. CATHODE
 3. CATHODE
 4. CATHODE
 5. CATHODE
 6. CATHODE
 7. CATHODE
 8. ANODE
 9. ANODE
 10. ANODE
 11. ANODE
 12. ANODE
 13. ANODE
 14. ANODE

STYLE 7:
 PIN 1. ANODE/CATHODE
 2. COMMON ANODE
 3. COMMON CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. COMMON CATHODE
 12. COMMON ANODE
 13. ANODE/CATHODE
 14. ANODE/CATHODE

STYLE 8:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. COMMON ANODE
 8. COMMON ANODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. NO CONNECTION
 12. ANODE/CATHODE
 13. ANODE/CATHODE
 14. COMMON CATHODE

DOCUMENT NUMBER:	98ASB42565B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-14 NB	PAGE 2 OF 2

onsemi and **ONSEMI** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



TSSOP-14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016

SCALE 2:1

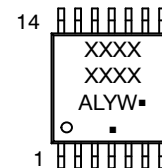


NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

GENERIC MARKING DIAGRAM*

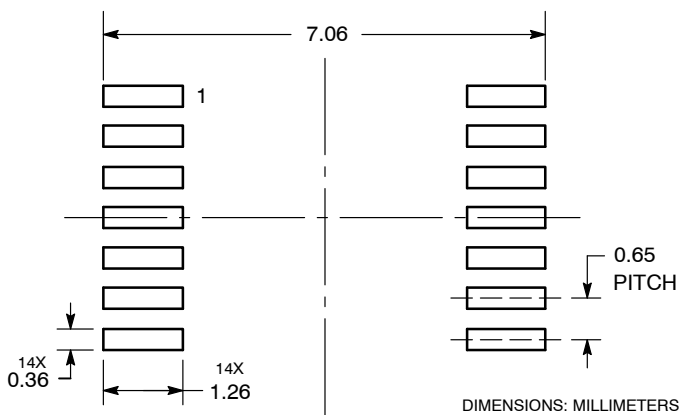


- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

SOLDERING FOOTPRINT



DOCUMENT NUMBER:	98ASH70246A	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TSSOP-14 WB	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales