

Octal D-Type Flip-Flop with 3-State Outputs

MC74LVX574

The MC74LVX574 is an advanced high speed CMOS octal flip-flop with 3-state outputs. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

This 8-bit D-type flip-flop is controlled by a clock pulse input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

Features

- High Speed: $t_{PD} = 8.5$ ns (Typ) at $V_{CC} = 3.3$ V
- Low Power Dissipation: $I_{CC} = 4$ μ A (Max) at $T_A = 25^\circ$ C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: $V_{OLP} = 0.8$ V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
 - Human Body Model > 2000 V;
 - Machine Model > 200 V
- These Devices are Pb-Free and are RoHS Compliant

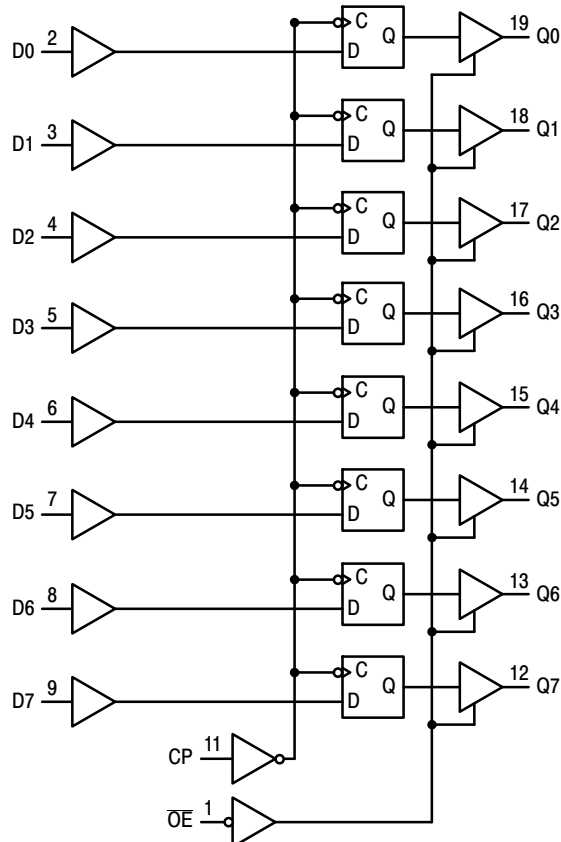
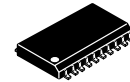


Figure 1. Logic Diagram

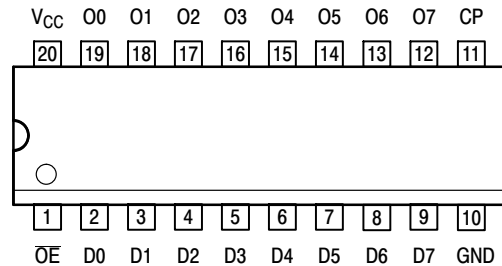


SOIC-20
DW SUFFIX
CASE 751D



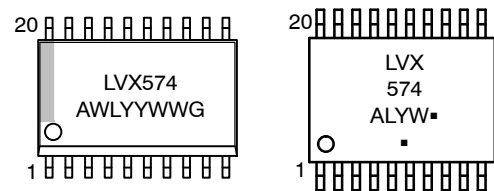
TSSOP-20
DT SUFFIX
CASE 948E

PIN ASSIGNMENT



20-Lead (Top View)

MARKING DIAGRAMS



SOIC-20

TSSOP-20

LVX574 = Specific Device Code
 A = Assembly Location
 WL, L = Wafer Lot
 Y = Year
 WW, W = Work Week
 G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.




NOTE: Some of the device on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5

MC74LVX574

PIN NAMES

| Pins | Function |
|-----------------|-----------------------|
| \overline{OE} | Output Enable Input |
| CP | Clock Pulse Input |
| D0–D7 | Data Inputs |
| O0–O7 | 3-State Latch Outputs |

FUNCTION TABLE

| INPUTS | | | OUTPUT |
|-----------------|---|---|-----------|
| \overline{OE} | CP | D | Q |
| L |  | H | H |
| L |  | L | L |
| L | L, H,  | X | No Change |
| H | X | X | Z |

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-----------|--|-----------------------|------|
| V_{CC} | DC Supply Voltage | –0.5 to +7.0 | V |
| V_{in} | DC Input Voltage | –0.5 to +7.0 | V |
| V_{out} | DC Output Voltage | –0.5 to V_{CC} +0.5 | V |
| I_{IK} | Input Diode Current | –20 | mA |
| I_{OK} | Output Diode Current | ±20 | mA |
| I_{out} | DC Output Current, per Pin | ±25 | mA |
| I_{CC} | DC Supply Current, V_{CC} and GND Pins | ±75 | mA |
| P_D | Power Dissipation | 180 | mW |
| T_{stg} | Storage Temperature | –65 to +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---------------------|--|-----|----------|------|
| V_{CC} | DC Supply Voltage | 2.0 | 3.6 | V |
| V_{in} | DC Input Voltage | 0 | 5.5 | V |
| V_{out} | DC Output Voltage | 0 | V_{CC} | V |
| T_A | Operating Temperature, All Package Types | –40 | +85 | °C |
| $\Delta t/\Delta V$ | Input Rise and Fall Time | 0 | 100 | ns/V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | V _{CC} V | T _A = 25°C | | | T _A = -40 to 85°C | | Unit |
|-----------------|--|---|----------------------|-----------------------|------------|--------------------|------------------------------|--------------------|------|
| | | | | Min | Typ | Max | Min | Max | |
| V _{IH} | High-Level Input Voltage | | 2.0 3.0 3.6 | 1.5 2.0 2.4 | | | 1.5 2.0 2.4 | | V |
| V _{IL} | Low-Level Input Voltage | | 2.0 3.0 3.6 | | | 0.5 0.8 0.8 | | 0.5 0.8 0.8 | V |
| V _{OH} | High-Level Output Voltage (V _{in} = V _{IH} or V _{IL}) | I _{OH} = -50 µA I _{OH} = -50 µA I _{OH} = -4 mA | 2.0 3.0 3.0 | 1.9 2.9 2.58 | 2.0 3.0 | | 1.9 2.9 2.48 | | V |
| V _{OL} | Low-Level Output Voltage (V _{in} = V _{IH} or V _{IL}) | I _{OL} = 50 µA I _{OL} = 50 µA I _{OL} = 4 mA | 2.0 3.0 3.0 | | 0.0 0.0 | 0.1 0.1 0.36 | | 0.1 0.1 0.44 | V |
| I _{in} | Input Leakage Current | V _{in} = 5.5 V or GND | 3.6 | | | ±0.1 | | ±1.0 | µA |
| I _{OZ} | Maximum 3-State Leakage Current | V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND | 3.6 | | | ±0.2 5 | | ±2.5 | µA |
| I _{CC} | Quiescent Supply Current | V _{in} = V _{CC} or GND | 3.6 | | | 4.0 | | 40.0 | µA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0ns)

| Symbol | Parameter | Test Conditions | | T _A = 25°C | | | T _A = -40 to 85°C | | Unit |
|--|---|--|--|-----------------------|-------------|--------------|------------------------------|--------------|------|
| | | | | Min | Typ | Max | Min | Max | |
| f _{max} | Maximum Clock Frequency (50% Duty Cycle) | V _{CC} = 2.7 V | C _L = 15 pF C _L = 50 pF | 60 45 | 115 60 | | 50 40 | | ns |
| | | V _{CC} = 3.3 ± 0.3 V | C _L = 15 pF C _L = 50 pF | 80 50 | 125 75 | | 65 45 | | |
| t _{PLH} , t _{PHL} | Propagation Delay CP to O | V _{CC} = 2.7 V | C _L = 15 pF C _L = 50 pF | | 9.2 11.5 | 14.5 18.0 | 1.0 1.0 | 17.5 21.0 | ns |
| | | V _{CC} = 3.3 ± 0.3 V | C _L = 15 pF C _L = 50 pF | | 8.5 11.0 | 13.2 16.7 | 1.0 1.0 | 15.5 19.0 | |
| t _{PZL} , t _{PZH} | Output Enable Time OE to O | V _{CC} = 2.7 V | C _L = 15 pF R _L = 1 kΩ | | 9.8 11.4 | 15.0 18.5 | 1.0 1.0 | 18.5 22.0 | ns |
| | | V _{CC} = 3.3 ± 0.3 V | C _L = 15 pF R _L = 1 kΩ | | 8.2 10.7 | 12.8 16.3 | 1.0 1.0 | 15.0 18.5 | |
| t _{PLZ} , t _{PHZ} | Output Disable Time OE to O | V _{CC} = 2.7 V | C _L = 50 pF R _L = 1 kΩ | | 12.1 | 19.1 | 1.0 | 22.0 | ns |
| | | V _{CC} = 3.3 ± 0.3 V | C _L = 50 pF R _L = 1 kΩ | | 11.0 | 15.0 | 1.0 | 17.0 | |
| t _{OSSL} , t _{OSLH} | Output-to-Output Skew (Note 1) | V _{CC} = 2.7 V V _{CC} = 3.3 ± 0.3 V | C _L = 50 pF C _L = 50 pF | | | 1.5 1.5 | | 1.5 1.5 | ns |

- Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSSL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

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CAPACITIVE CHARACTERISTICS

| Symbol | Parameter | T _A = 25°C | | | T _A = -40 to 85°C | | Unit |
|------------------|--|-----------------------|-----|-----|------------------------------|-----|------|
| | | Min | Typ | Max | Min | Max | |
| C _{in} | Input Capacitance | | 4 | 10 | | 10 | pF |
| C _{out} | Maximum Three-State Output Capacitance | | 6 | | | | pF |
| C _{PD} | Power Dissipation Capacitance (Note 2) | | 28 | | | | pF |

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/8$ (per latch). C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

NOISE CHARACTERISTICS (Input t_r = t_f = 3.0ns, C_L = 50pF, V_{CC} = 3.3V, Measured in SOIC Package)

| Symbol | Characteristic | T _A = 25°C | | Unit |
|------------------|--|-----------------------|------|------|
| | | Typ | Max | |
| V _{OLP} | Quiet Output Maximum Dynamic V _{OL} | 0.5 | 0.8 | V |
| V _{OLV} | Quiet Output Minimum Dynamic V _{OL} | -0.5 | -0.8 | V |
| V _{IHD} | Minimum High Level Dynamic Input Voltage | | 2.0 | V |
| V _{ILD} | Maximum Low Level Dynamic Input Voltage | | 0.8 | V |

TIMING REQUIREMENTS (Input t_r = t_f = 3.0ns)

| Symbol | Parameter | Test Conditions | T _A = 25°C | | T _A = -40 to 85°C | Unit |
|-------------------|-----------------------------|---|-----------------------|------------|------------------------------|------|
| | | | Typ | Limit | Limit | |
| t _{w(h)} | Minimum Pulse Width, CP | V _{CC} = 2.7 V V _{CC} = 3.3 ±0.3 V | | 6.5 5.0 | 7.5 5.0 | ns |
| t _{su} | Minimum Setup Time, D to CP | V _{CC} = 2.7 V V _{CC} = 3.3 ±0.3 V | | 5.0 3.5 | 5.0 3.5 | ns |
| t _h | Minimum Hold Time, D to CP | V _{CC} = 2.7 V V _{CC} = 3.3 ±0.3 V | | 1.5 1.5 | 1.5 1.5 | ns |

SWITCHING WAVEFORMS

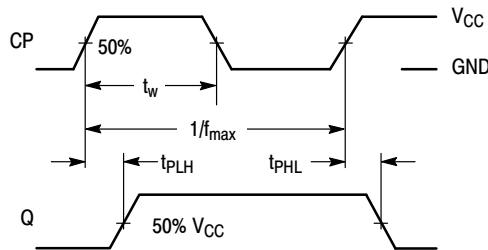


Figure 2.

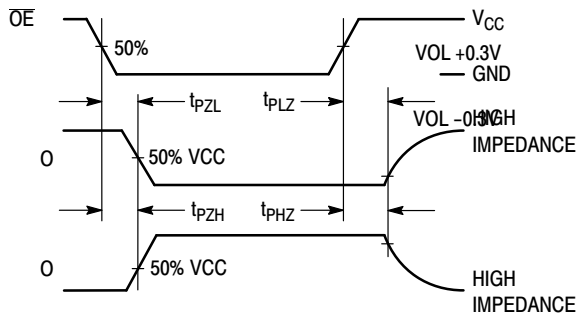


Figure 3.

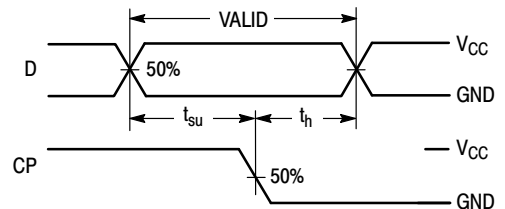
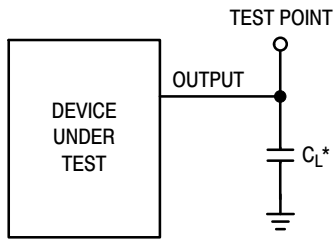


Figure 4.

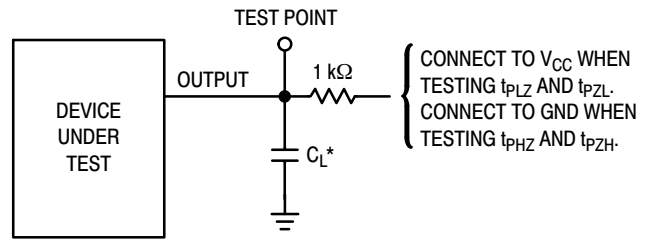
MC74LVX574

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 5. Propagation Delay Test Circuit



*Includes all probe and jig capacitance

Figure 6. Three-State Test Circuit

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|-----------------|-----------------------|-----------------------|
| MC74LVX574DWR2G | SOIC-20 (Pb-Free) | 1000 Tape & Reel |
| MC74LVX574DTG | TSSOP-20 (Pb-Free) | 75 Units / Rail |

DISCONTINUED (Note 3)

| Device | Package | Shipping [†] |
|-----------------|-----------------------|-----------------------|
| MC74LVX574DTR2G | TSSOP-20 (Pb-Free) | 2500 Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

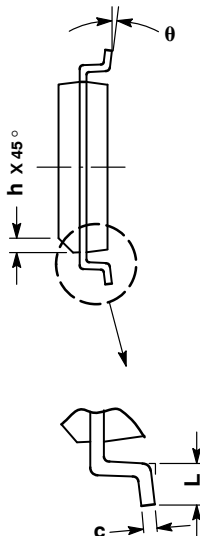
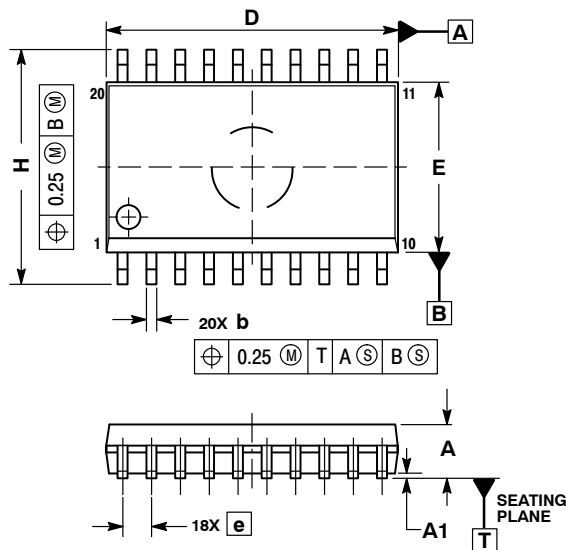
3. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.



SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015

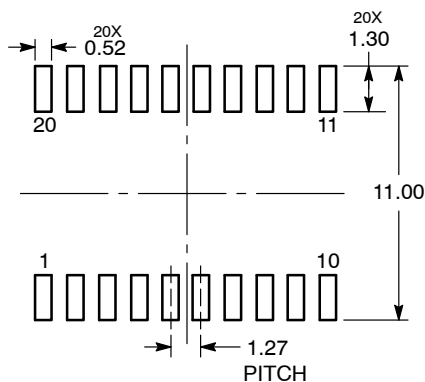


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | |
|-----|-------------|-------|
| | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| b | 0.35 | 0.49 |
| c | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

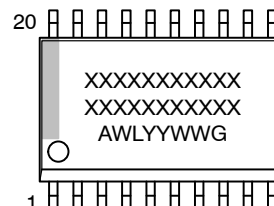
RECOMMENDED
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*

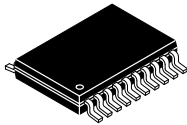


XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

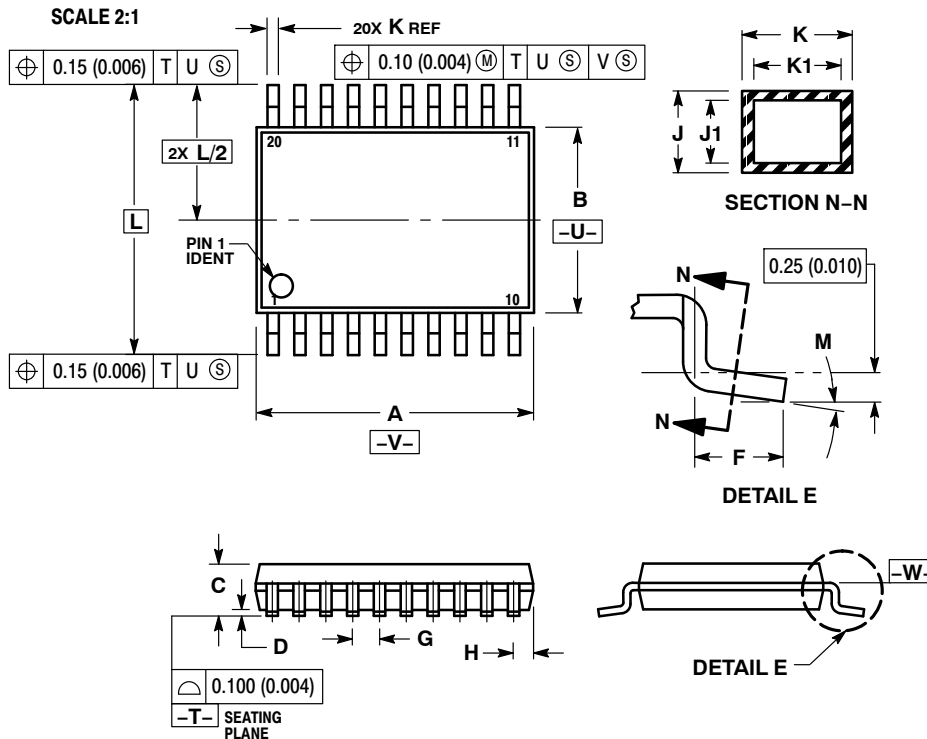
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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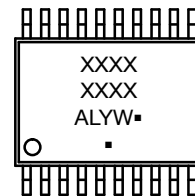

TSSOP-20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

GENERIC MARKING DIAGRAM*


A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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