

Low-Voltage CMOS Octal Transparent Latch Flow Through Pinout

With 5 V-Tolerant Inputs and Outputs
(3-State, Non-Inverting)

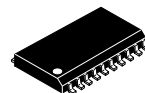
MC74LCX573

The MC74LCX573 is a high performance, non-inverting octal transparent latch operating from a 1.65 to 5.5 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5 V allows MC74LCX573 inputs to be safely driven from 5.0 V devices.

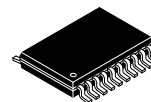
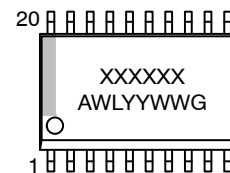
The MC74LCX573 contains 8 D-type latches with 3-state standard outputs. When the Latch Enable (LE) input is HIGH, data on the Dn inputs enters the latches. In this condition, the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state standard outputs are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the standard outputs are enabled. When \overline{OE} is HIGH, the standard outputs are in the high impedance state, but this does not interfere with new data entering into the latches. The LCX573 flow through design facilitates easy PC board layout.

Features

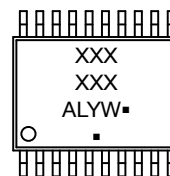
- Designed for 1.65 to 5.5 V V_{CC} Operation
- 5.0 V Tolerant – Interface Capability With 5.0 V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When $V_{CC} = 0$ V
- LVTTTL Compatible
- LVC MOS Compatible
- 24 mA Balanced Output Sink and Source Capability at 3 V
- Near Zero Static Supply Current in All Three Logic States (10 μ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 100 mA
- ESD Performance:
 - ♦ Human Body Model >2000 V
- -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



SOIC-20 WB
DW SUFFIX
CASE 751D



TSSOP-20
DT SUFFIX
CASE 948E



A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 8.

MC74LCX573

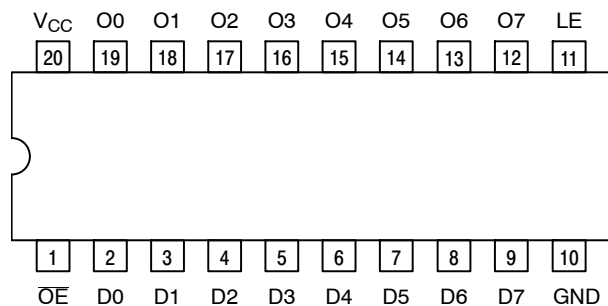


Figure 1. Pinout (Top View)

PIN NAMES

| Pins | Function |
|-------|-----------------------|
| OE | Output Enable Input |
| LE | Latch Enable Input |
| D0-D7 | Data Inputs |
| O0-O7 | 3-State Latch Outputs |

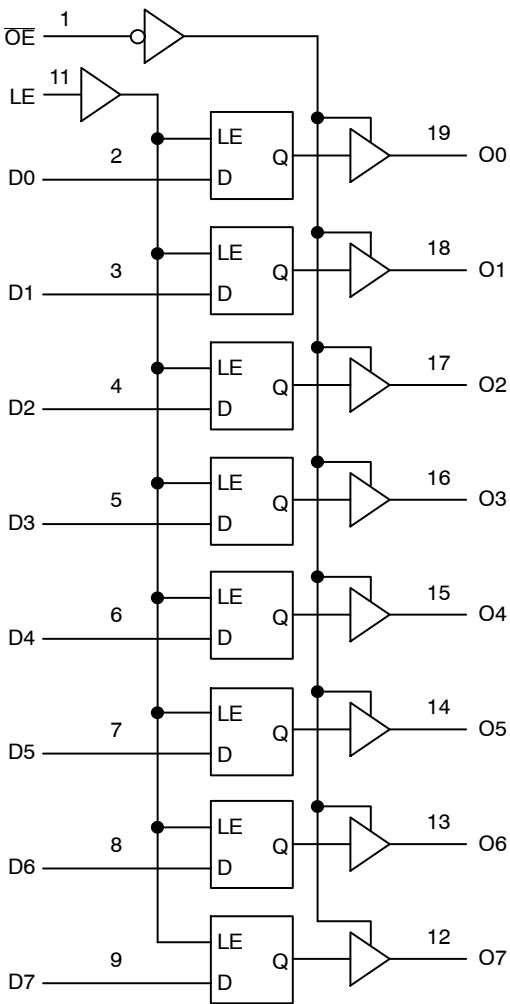


Figure 2. Logic Diagram

TRUTH TABLE

| Inputs | | | Outputs | Operating Mode |
|--------|----|----|---------|--|
| OE | LE | Dn | On | |
| L | H | H | H | Transparent (Latch Disabled); Read Latch |
| L | H | L | L | |
| L | L | h | H | Latched (Latch Enabled) Read Latch |
| L | L | l | L | |
| L | L | X | NC | Hold; Read Latch |
| H | L | X | Z | Hold; Disabled Outputs |
| H | H | H | Z | Transparent (Latch Disabled); Disabled Outputs |
| H | H | L | Z | |
| H | L | h | Z | Latched (Latch Enabled); Disabled Outputs |
| H | L | l | Z | |

H = High Voltage Level;
h = High Voltage Level One Setup Time Prior to the Latch Enable High-to-Low Transition
L = Low Voltage Level
l = Low Voltage Level One Setup Time Prior to the Latch Enable High-to-Low Transition
NC = No Change, State Prior to the Latch Enable High-to-Low Transition
X = High or Low Voltage Level or Transitions are Acceptable
Z = High Impedance State
For I_{CC} Reasons DO NOT FLOAT Inputs

MC74LCX573

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-----------------------|--|------------------------|------|
| V_{CC} | DC Supply Voltage | –0.5 to +6.5 | V |
| V_I | DC Input Voltage (Note 1) | –0.5 to +6.5 | V |
| V_O | DC Output Voltage (Note 1) Active-Mode (High or Low State) | –0.5 to $V_{CC} + 0.5$ | V |
| | Tri-State Mode | –0.5 to +6.5 | |
| | Power-Down Mode ($V_{CC} = 0$ V) | –0.5 to +6.5 | |
| I_{IK} | DC Input Diode Current $V_{IN} < GND$ | –50 | mA |
| I_{OK} | DC Output Diode Current $V_{OUT} < GND$ | –50 | mA |
| I_O | DC Output Source/Sink Current | ±50 | mA |
| I_{CC} or I_{GND} | DC Supply Current per Supply Pin or Ground Pin | ±100 | mA |
| T_{STG} | Storage Temperature Range | –65 to +150 | °C |
| T_L | Lead Temperature, 1 mm from Case for 10 secs | 260 | °C |
| T_J | Junction Temperature Under Bias | +150 | °C |
| θ_{JA} | Thermal Resistance (Note 2) SOIC-20W | 96 | °C/W |
| | WQFN20 | 99 | |
| | QFN20 | 111 | |
| | TSSOP-20 | 150 | |
| P_D | Power Dissipation in Still Air SOIC-20W | 1302 | mW |
| | WQFN20 | 1256 | |
| | QFN20 | 1127 | |
| | TSSOP-20 | 833 | |
| MSL | Moisture Sensitivity SOIC-20W All Other Packages | Level 3 Level 1 | – |
| F_R | Flammability Rating Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in | – |
| V_{ESD} | ESD Withstand Voltage (Note 3) Human Body Model | > 2000 | V |
| | Charged Device Model | N/A | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

MC74LCX573

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Typ | Max | Unit | |
|---------------------------------|--------------------------------|---|------|------|-----------------|------|
| V _{CC} | Supply Voltage | Operating | 1.65 | 3.3 | 5.5 | V |
| | | Data Retention Only | 1.5 | 3.3 | 5.5 | |
| V _I | Digital Input Voltage | 0 | – | 5.5 | V | |
| V _O | Output Voltage | Active Mode (High or Low State) | 0 | – | V _{CC} | V |
| | | Tri-State Mode | 0 | – | 5.5 | |
| | | Power Down Mode (V _{CC} = 0 V) | 0 | – | 5.5 | |
| T _A | Operating Free-Air Temperature | –55 | – | +125 | °C | |
| t _r , t _f | Input Rise or Fall Rate | V _{CC} = 1.65 V to 1.95 V | 0 | – | 20 | nS/V |
| | | V _{CC} = 2.3 V to 2.7 V | 0 | – | 20 | |
| | | V _I from 0.8 V to 2.0 V, V _{CC} = 3.0 V | 0 | – | 10 | |
| | | V _{CC} = 4.5 V to 5.5 V | 0 | – | 5 | |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | V_{CC} (V) | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ | | $T_A = -55^\circ\text{C to } +125^\circ\text{C}$ | | Unit |
|----------|---------------------------|-----------------------------|--------------|---|----------------------|--|----------------------|---------------|
| | | | | Min | Max | Min | Max | |
| V_{IH} | High-Level Input Voltage | | 1.65 to 1.95 | $0.65 \times V_{CC}$ | | $0.65 \times V_{CC}$ | | V |
| | | | 2.3 to 2.7 | 1.7 | | 1.7 | | |
| | | | 2.7 to 3.6 | 2.0 | | 2.0 | | |
| | | | 4.5 to 5.5 | $0.7 \times V_{CC}$ | | $0.7 \times V_{CC}$ | | |
| V_{IL} | Low-Level Input Voltage | | 1.65 to 1.95 | | $0.35 \times V_{CC}$ | | $0.35 \times V_{CC}$ | V |
| | | | 2.3 to 2.7 | | 0.7 | | 0.7 | |
| | | | 2.7 to 3.6 | | 0.8 | | 0.8 | |
| | | | 4.5 to 5.5 | | $0.3 \times V_{CC}$ | | $0.3 \times V_{CC}$ | |
| V_{OH} | High-Level Output Voltage | $V_I = V_{IH}$ or V_{IL} | | | | | | V |
| | | $I_{OH} = -100 \mu\text{A}$ | 1.65 to 5.5 | $V_{CC} - 0.1$ | – | $V_{CC} - 0.1$ | – | |
| | | $I_{OH} = -4 \text{ mA}$ | 1.65 | 1.2 | – | 1.2 | – | |
| | | $I_{OH} = -8 \text{ mA}$ | 2.3 | 1.8 | – | 1.8 | – | |
| | | $I_{OH} = -12 \text{ mA}$ | 2.7 | 2.2 | – | 2.2 | – | |
| | | $I_{OH} = -16 \text{ mA}$ | 3.0 | 2.4 | – | 2.4 | – | |
| | | $I_{OH} = -24 \text{ mA}$ | 3.0 | 2.2 | – | 2.2 | – | |
| | | $I_{OH} = -32 \text{ mA}$ | 4.5 | 3.8 | | 3.8 | | |
| V_{OL} | Low-Level Output Voltage | $V_I = V_{IH}$ or V_{IL} | | | | | | V |
| | | $I_{OL} = 100 \mu\text{A}$ | 1.65 to 5.5 | – | 0.1 | – | 0.1 | |
| | | $I_{OL} = 4 \text{ mA}$ | 1.65 | – | 0.45 | – | 0.45 | |
| | | $I_{OL} = 8 \text{ mA}$ | 2.3 | – | 0.6 | – | 0.6 | |
| | | $I_{OL} = 12 \text{ mA}$ | 2.7 | – | 0.4 | – | 0.4 | |
| | | $I_{OL} = 16 \text{ mA}$ | 3.0 | – | 0.4 | – | 0.4 | |
| | | $I_{OL} = 24 \text{ mA}$ | 3.0 | – | 0.55 | – | 0.55 | |
| | | $I_{OL} = 32 \text{ mA}$ | 4.5 | | 0.6 | | 0.6 | |
| I_I | Input Leakage Current | $V_I = 0$ to 5.5 V | 3.6 | – | ± 5.0 | – | ± 5.0 | μA |

MC74LCX573

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | V _{CC} (V) | T _A = -40 °C to +85 °C | | T _A = -55 °C to +125 °C | | Unit |
|------------------|---------------------------------------|--|---------------------|-----------------------------------|------|------------------------------------|------|------|
| | | | | Min | Max | Min | Max | |
| I _{OZ} | 3-State Output Leakage Current | V _I = V _{IH} or V _{IL} , V _O = 0 V to 5.5 V | 3.6 | – | ±5.0 | – | ±5.0 | μA |
| I _{OFF} | Power Off Leakage Current | V _I = 5.5 V or V _O = 5.5 V | 0 | – | 10 | – | 10 | μA |
| I _{CC} | Quiescent Supply Current | V _I = 5.5 V or GND | 3.6 | – | 10 | – | 10 | μA |
| ΔI _{CC} | Increase in I _{CC} per Input | V _{IH} = V _{CC} – 0.6 V | 2.3 to 3.6 | – | 500 | – | 500 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. These values of V_I are used to test DC electrical characteristics only.

AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Condition | V _{CC} (V) | T _A = -40 °C to +85 °C | | T _A = -55 °C to +125 °C | | Unit |
|--|-------------------------------------|----------------|---------------------|-----------------------------------|------|------------------------------------|------|------|
| | | | | Min | Max | Min | Max | |
| t _{PLH} , t _{PHL} | Propagation Delay, Dn to On | Waveform 1 | 1.65 to 1.95 | – | 14.0 | – | 14.0 | ns |
| | | | 2.3 to 2.7 | – | 9.6 | – | 9.6 | |
| | | | 2.7 | – | 9.0 | – | 9.0 | |
| | | | 3.0 to 3.6 | – | 8.0 | – | 8.0 | |
| | | | 4.5 to 5.5 | – | 5.5 | – | 5.5 | |
| t _{PLH} , t _{PHL} | Propagation Delay, LE to On | Waveform 3 | 1.65 to 1.95 | – | 15.0 | – | 15.0 | ns |
| | | | 2.3 to 2.7 | – | 10.5 | – | 10.5 | |
| | | | 2.7 | – | 9.5 | – | 9.5 | |
| | | | 3.0 to 3.6 | – | 8.5 | – | 8.5 | |
| | | | 4.5 to 5.5 | – | 6.0 | – | 6.0 | |
| t _{PZH} , t _{PZL} | Output Enable Time, to On | Waveform 2 | 1.65 to 1.95 | – | 15.0 | – | 15.0 | ns |
| | | | 2.3 to 2.7 | – | 10.5 | – | 10.5 | |
| | | | 2.7 | – | 9.5 | – | 9.5 | |
| | | | 3.0 to 3.6 | – | 8.5 | – | 8.5 | |
| | | | 4.5 to 5.5 | – | 6.0 | – | 6.0 | |
| t _{PHZ} , t _{PLZ} | Output Enable Time, to On | Waveform 2 | 1.65 to 1.95 | – | 10.0 | – | 10.0 | ns |
| | | | 2.3 to 2.7 | – | 7.8 | – | 7.8 | |
| | | | 2.7 | – | 7.0 | – | 7.0 | |
| | | | 3.0 to 3.6 | – | 6.5 | – | 6.5 | |
| | | | 4.5 to 5.5 | – | 4.5 | – | 4.5 | |
| t _s | Setup Time, HIGH or LOW Dn to LE | Waveform 3 | 1.65 to 1.95 | 4.0 | – | 4.0 | – | ns |
| | | | 2.3 to 2.7 | 4.0 | – | 4.0 | – | |
| | | | 2.7 | 2.5 | – | 2.5 | – | |
| | | | 3.0 to 3.6 | 2.5 | – | 2.5 | – | |
| | | | 4.5 to 5.5 | 2.5 | – | 2.5 | – | |

MC74LCX573

AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Condition | V _{CC} (V) | T _A = -40 °C to +85 °C | | T _A = -55 °C to +125 °C | | Unit |
|--|---------------------------------|----------------|---------------------|-----------------------------------|-----|------------------------------------|-----|------|
| | | | | Min | Max | Min | Max | |
| t _h | Hold Time, HIGH or LOW Dn to LE | Waveform 3 | 1.65 to 1.95 | 2.0 | – | 2.0 | – | ns |
| | | | 2.3 to 2.7 | 2.0 | – | 2.0 | – | |
| | | | 2.7 | 1.5 | – | 1.5 | – | |
| | | | 3.0 to 3.6 | 1.5 | – | 1.5 | – | |
| | | | 4.5 to 5.5 | 1.5 | – | 1.5 | – | |
| t _w | Pulse Width, LE HIGH | Waveform 3 | 1.65 to 1.95 | 4.0 | – | 4.0 | – | ns |
| | | | 2.3 to 2.7 | 4.0 | – | 4.0 | – | |
| | | | 2.7 | 3.3 | – | 3.3 | – | |
| | | | 3.0 to 3.6 | 3.3 | – | 3.3 | – | |
| | | | 4.5 to 5.5 | 3.3 | – | 3.3 | – | |
| t _{OSHL} , t _{OSLH} | Output to Output Skew | | 1.65 to 1.95 | – | – | – | – | ns |
| | | | 2.3 to 2.7 | – | – | – | – | |
| | | | 2.7 | – | – | – | – | |
| | | | 3.0 to 3.6 | – | 1.0 | – | 1.0 | |
| | | | 4.5 to 5.5 | – | – | – | – | |

DYNAMIC SWITCHING CHARACTERISTICS

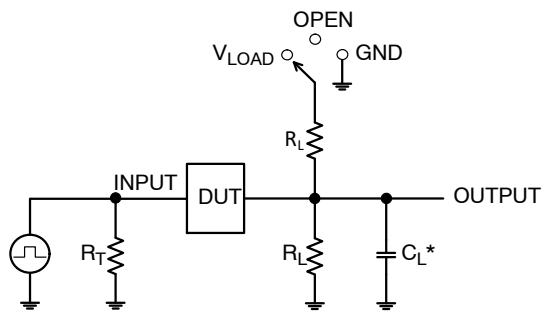
| Symbol | Characteristic | Condition | T _A = +25 °C | | | Unit |
|------------------|-------------------------------------|--|-------------------------|--------------|-----|--------|
| | | | Min | Typ | Max | |
| V _{OLP} | Dynamic LOW Peak Voltage (Note 6) | V _{CC} = 3.3 V, C _L = 50 pF, V _{IH} = 3.3 V, V _{IL} = 0 V V _{CC} = 2.5 V, C _L = 30 pF, V _{IH} = 2.5 V, V _{IL} = 0 V | | 0.8 0.6 | | V V |
| V _{OLV} | Dynamic LOW Valley Voltage (Note 6) | V _{CC} = 3.3 V, C _L = 50 pF, V _{IH} = 3.3 V, V _{IL} = 0 V V _{CC} = 2.5 V, C _L = 30 pF, V _{IH} = 2.5 V, V _{IL} = 0 V | | –0.8 –0.6 | | V V |

6. Number of outputs defined as “n”. Measured with “n-1” outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

| Symbol | Parameter | Condition | Typ | Unit |
|------------------|-------------------------------|--|-----|------|
| C _{IN} | Input Capacitance | V _{CC} = 3.3 V, V _I = 0 V or V _{CC} | 7 | pF |
| C _{I/O} | Input/Output Capacitance | V _{CC} = 3.3 V, V _I = 0 V or V _{CC} | 8 | pF |
| C _{PD} | Power Dissipation Capacitance | 10 MHz, V _{CC} = 3.3 V, V _I = 0 V or V _{CC} | 25 | pF |

MC74LCX573



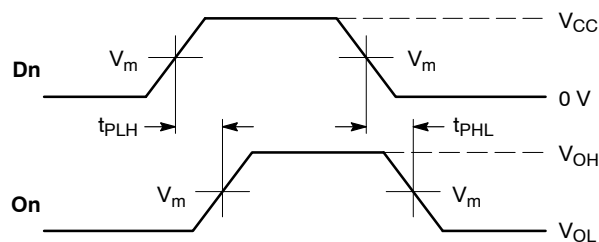
C_L includes probe and jig capacitance
 R_T is Z_{OUT} of pulse generator (typically 50 Ω)
 $f = 1$ MHz

| Test | Switch Position |
|---------------------|-----------------|
| t_{PLH} / t_{PHL} | Open |
| t_{PLZ} / t_{PZL} | V_{LOAD} |
| t_{PHZ} / t_{PZH} | GND |

Figure 3. Test Circuit

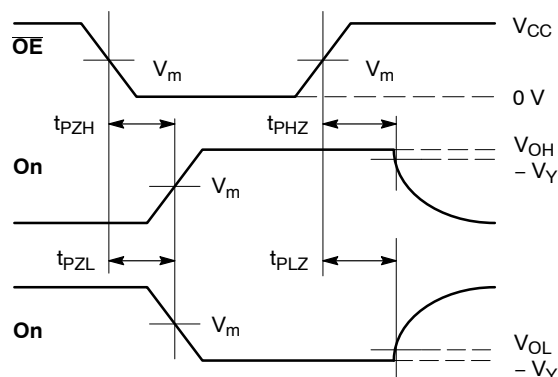
| V_{CC}, V | R_L, Ω | C_L, pF | V_{LOAD} | V_m, V | V_Y, V |
|--------------|---------------|-----------|-------------------|------------|----------|
| 1.65 to 1.95 | 500 | 30 | $2 \times V_{CC}$ | $V_{CC}/2$ | 0.15 |
| 2.3 to 2.7 | 500 | 30 | $2 \times V_{CC}$ | $V_{CC}/2$ | 0.15 |
| 2.7 | 500 | 50 | 6 V | 1.5 | 0.3 |
| 3.0 to 3.6 | 500 | 50 | 6 V | 1.5 | 0.3 |
| 4.5 to 4.5 | 500 | 50 | $2 \times V_{CC}$ | $V_{CC}/2$ | 0.3 |

MC74LCX573



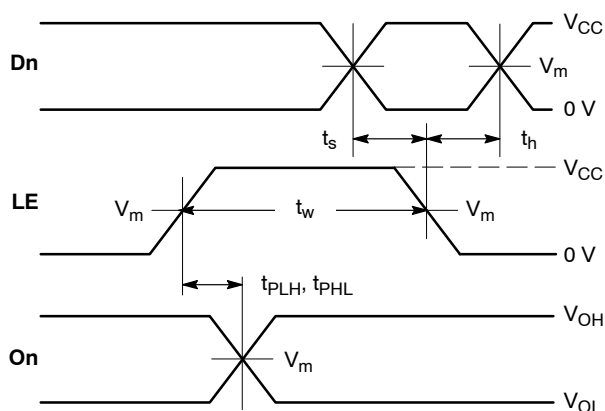
WAVEFORM 1 – PROPAGATION DELAYS

$t_R = t_F = 2.5 \text{ ns}$, 10% to 90%; $f = 1 \text{ MHz}$; $t_W = 500 \text{ ns}$



WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES

$t_R = t_F = 2.5 \text{ ns}$, 10% to 90%; $f = 1 \text{ MHz}$; $t_W = 500 \text{ ns}$



WAVEFORM 3 – LE to On PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn to LE SETUP AND HOLD TIMES

$t_R = t_F = 2.5 \text{ ns}$, 10% to 90%; $f = 1 \text{ MHz}$; $t_W = 500 \text{ ns}$ except when noted

Figure 4. AC Waveforms

ORDERING INFORMATION

| Device | Marking | Package | Shipping† |
|--------------------|---------|--------------------|------------------|
| MC74LCX573DWG | LCX573 | SOIC-20 (Pb-Free) | 38 Units / Rail |
| MC74LCX573DWR2G | LCX573 | SOIC-20 (Pb-Free) | 1000 Tape & Reel |
| MC74LCX573DTG | LCX 573 | TSSOP-20 (Pb-Free) | 75 Units / Rail |
| MC74LCX573DTR2G | LCX573 | TSSOP-20 (Pb-Free) | 2500 Tape & Reel |
| MC74LCX573DTR2G-Q* | LCX573 | TSSOP-20 (Pb-Free) | 2500 Tape & Reel |

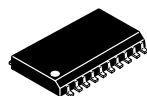
DISCONTINUED (Note 7)

| | | | |
|-------------------|--|--------------------|------------------|
| NLV74LCX573DTR2G* | | TSSOP-20 (Pb-Free) | 2500 Tape & Reel |
|-------------------|--|--------------------|------------------|

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

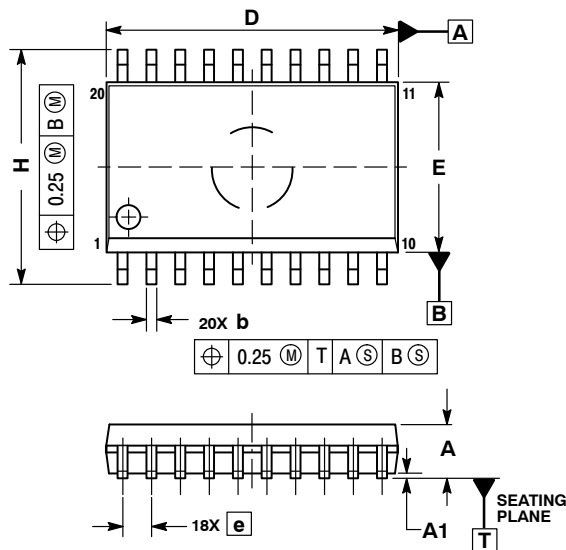
7. **DISCONTINUED:** This device is not recommended for new design. Please contact your onsemi representative for information. The most current information on this device may be available on www.onsemi.com.



SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015

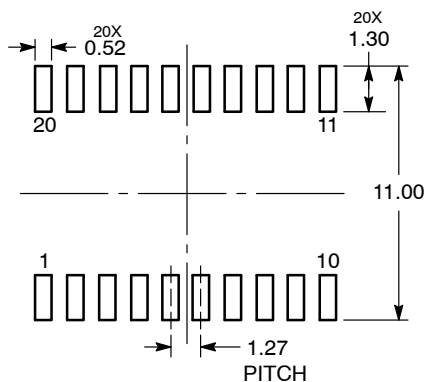


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | |
|-----|-------------|-------|
| | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| b | 0.35 | 0.49 |
| c | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

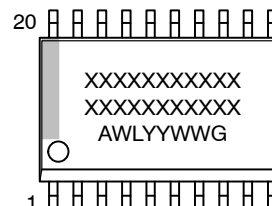
RECOMMENDED
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*

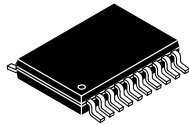


XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

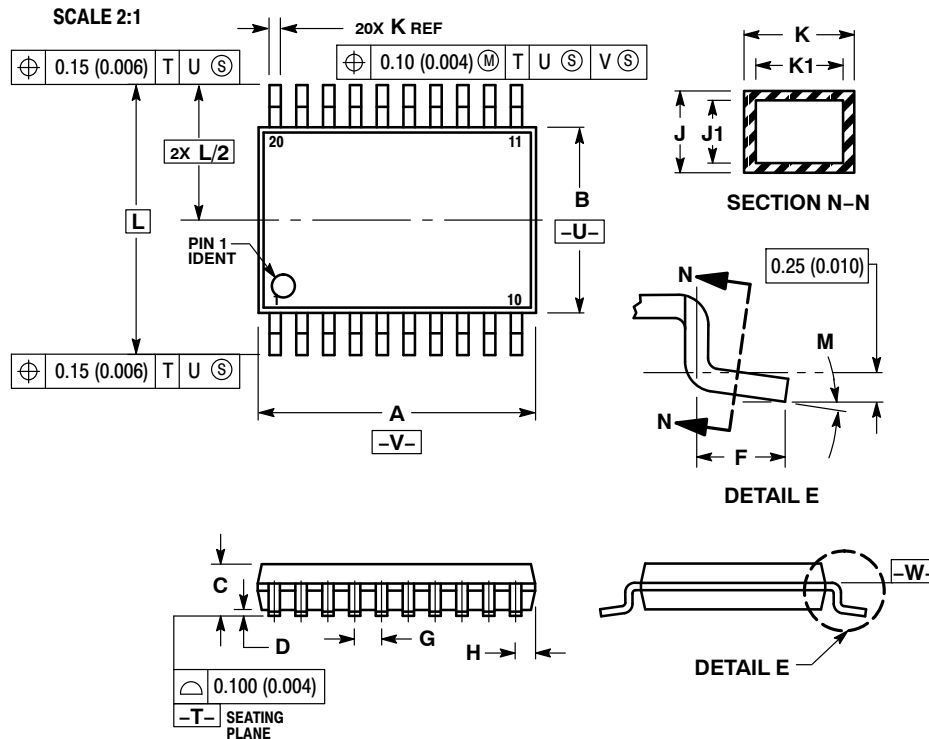
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|------------------|-------------|---|
| DOCUMENT NUMBER: | 98ASB42343B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | SOIC-20 WB | PAGE 1 OF 1 |

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

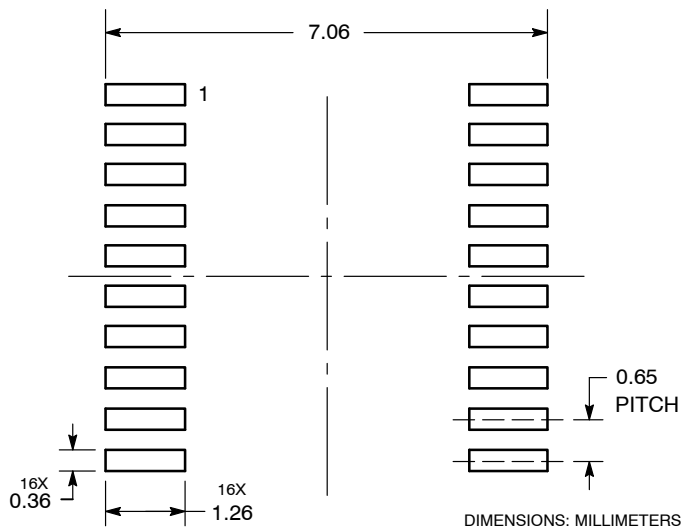

TSSOP-20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016

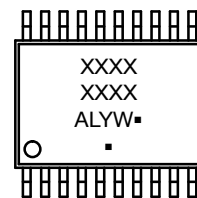

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

**RECOMMENDED
SOLDERING FOOTPRINT***


*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC
MARKING DIAGRAM***


A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|-------------------------|--------------------|---|
| DOCUMENT NUMBER: | 98ASH70169A | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | TSSOP-20 WB | PAGE 1 OF 1 |

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales