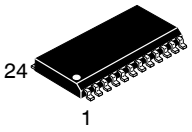
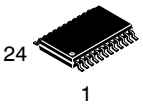
Quad Analog Switch/ Multiplexer/Demultiplexer

MC74HC4067A

High-Performance Silicon-Gate CMOS



SOIC-24
DW SUFFIX
CASE 751E



TSSOP-24
DT SUFFIX
CASE 948H

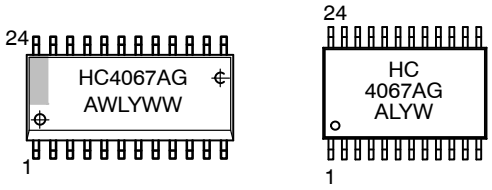
The MC74HC4067A utilizes silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF-channel leakage current. This bilateral switch/ multiplexer/demultiplexer controls analog and digital voltages that may vary across the full power-supply range (from V_{CC} to GND).

The ON/OFF control inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. For analog switches with voltage-level translators, see the HC4316A.

Features

- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Wide Power-Supply Voltage Range (V_{CC} − GND) = 2.0 to 6.0 V
- Analog Input Voltage Range (V_{CC} − GND) = 0 to 6.0 V
- Improved Linearity and Lower ON Resistance over Input Voltage
- Low Noise
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These are Pb-Free Devices

MARKING DIAGRAM



A	= Assembly Location
L, WL	= Wafer Lot
Y, YY	= Year
W, WW	= Work Week
G	= Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 10.

© Semiconductor Components Industries, LLC, 2015

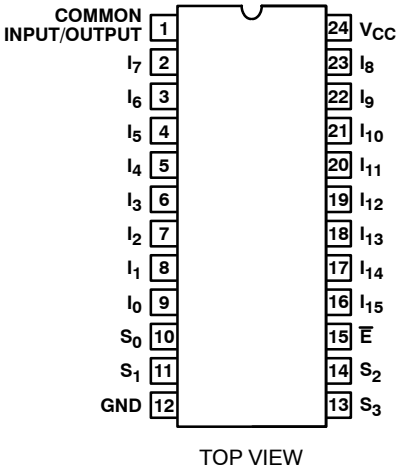


Figure 1. Pin Assignment

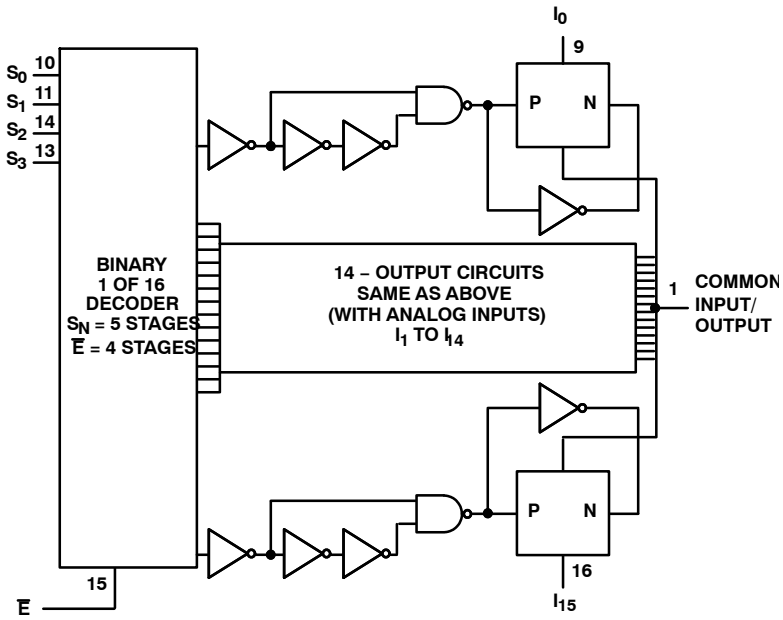


Figure 2. Function Diagram

TRUTH TABLE

S0	S1	S2	S3	$\overline{E}$	SELECTED CHANNEL
X	X	X	X	1	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

H= High Level
L= Low Level
X= Don't Care

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +7.0	V
V_{IS}	Analog Input Voltage		−0.5 to V_{CC} + 0.5	V
V_{IN}	Digital Input Voltage		−0.5 to V_{CC} + 0.5	V
I_{IK}	Input Clamping Current	V_{IN} < −0.5 V or V_{IN} > V_{CC} + 0.5 V	±20	mA
I_{SK}	Switch Input Clamping Current	V_{IS} < −0.5 V or V_{IS} > V_{CC} + 0.5 V	±20	mA
I_{IS}	DC Switch Current		±25	mA
I_O	DC Output Source / Sink Current		±25	mA
I_{CC}	DC Supply Current per Supply Pin		±100	mA
I_{GND}	DC Ground Current per Ground Pin		±100	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature under Bias		+150	°C
θ_{JA}	Thermal Resistance	SOIC TSSOP	97 148	°C/W
P_D	Power Dissipation in Still Air at 85 °C	SOIC TSSOP	500 450	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 30% − 35%	UL−94−VO (0.125 in)	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2)	>3000 >200	V
$I_{Latchup}$	Latchup Performance	Above V_{CC} and Below GND at 85 °C (Note 3)	±100	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Tested to EIA/JESD22-A114-A.
2. Tested to EIA/JESD22-A115-A.
3. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{IS}	Analog Input Voltage (Referenced to GND)		GND	V_{CC}	V
V_{in}	Digital Input Voltage (Referenced to GND)		GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch		−	1.2	V
T_A	Operating Temperature, All Package Types		−55	+125	°C
t_r, t_f	Input Rise and Fall Rate (Digital Inputs)	V_{CC} = 2.0 V V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0 0	1000 600 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

* For voltage drops across the switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC ELECTRICAL CHARACTERISTIC Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Conditions	V_{CC} (V)	Guaranteed Limit							Unit
				25 °C			−40 to 85 °C		−55 to 125 °C		
				Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	Minimum High-Level Input Voltage, Channel-Select or Enable Inputs		2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2			1.5 2.1 3.15 4.2			1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage, Channe-Select or Enable Inputs		2.0 3.0 4.5 6.0			0.5 0.9 1.35 1.8		0.5 0.9 1.35 1.8		0.5 0.9 1.35 1.8	V
I_{IN}	Input Leakage Current, Control Inputs	V_{IN} = V_{CC} or GND	6.0			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Supply Current per Package	V_{IN} = V_{CC} or GND, I_O=0 V_{IS} = GND or V_{CC}, V_{OS} = V_{CC} or GND	6.0			4.0		40		80	μA
R_{ON}	ON Resistance	I_O = 1 mA V_{IN} = V_{CC} or GND, V_{IS} = V_{CC} or GND	4.5 6.0		70 60	160 140		200 175		240 210	Ω
$R_{ON(peak)}$	ON Resistance (peak)	I_O = 1 mA V_{IN} = V_{CC} to GND, V_{IS} = V_{CC} to GND	4.5 6.0		90 80	180 160		225 200		270 240	Ω
ΔR_{on}	ON Resistance Mismatch Between Any 2 Switches		4.5 6.0		10 8.5						Ω
I_{OFF}	OFF-State Leakage Current, All Channels	SW OFF, V_{IS} = V_{CC} or GND	6.0			±0.8		±8		±8	μA
I_{ON}	ON-State Leakage Current	SW OFF, V_{IS} = V_{CC} or GND	6.0			±0.8		±8		±8	μA

AC CHARACTERISTICS (INPUT t_r, t_f = 6 ns)

Symbol	Parameter	Conditions	V_{CC} (V)	Guaranteed Limits							Unit
				25 °C			–40 to 85 °C		–55 to 125 °C		
				Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay Switch In to Out	C_L = 50 pF	2.0 4.5 6.0			75 15 13		95 19 16		110 22 19	ns
		C_L = 15 pF	5.0		6.0						
t_{ON}	Switch Turn-ON Time										ns
	$\overline{E}$ to Out	C_L = 50 pF	2.0 4.5 6.0			275 55 47		345 69 59		415 83 71	
		C_L = 15 pF	5.0		23						
	SN to Out	C_L = 50 pF	2.0 4.5 6.0			300 60 51		375 75 64		450 90 76	
		C_L = 15 pF	5.0		25						
t_{OFF}	Switch Turn-OFF Time										ns
	$\overline{E}$ to Out	C_L = 50 pF	2.0 4.5 6.0			275 55 47		345 69 59		415 83 71	
		C_L = 15 pF	5.0		23						
	SN to Out	C_L = 50 pF	2.0 4.5 6.0			290 58 49		365 73 62		435 87 74	
		C_L = 15 pF	5.0		21						
C_{in}	Input Capacitance, Control Pins				3.5	10		10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 4)	C_L = 15 pF	5.0			29					pF

4. C_{PD} is used to determine the dynamic power consumption, per multivibrator.

ANALOG SWITCH CHANNEL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	Limit* 25 °C	Unit
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response	f_{in} = 1 MHz Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{OS} Increase f_{in} Frequency Until dB Meter Reads-3 dB R_L = 50 Ω, C_L = 10 pF	4.5	90	MHz
–	Off-Channel Feedthrough Isolation	f_{in} ≡ Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	 4.5 4.5	 –65 –75	dB
–	Feedthrough Noise $\overline{E}$, Sn to Switch	V_{in} ≤ 1 MHz Square Wave (t_r = t_f = 6 ns) Adjust R_L at Setup so that I_S = 0 A R_L = 600 Ω, C_L = 50 pF R_L = 10 kΩ, C_L = 10 pF	 4.5 4.5	 60 30	mV_{PP}
–	Crosstalk Between Any Two Switches	f_{in} ≡ Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	 4.5 4.5	 –70 –80	dB
THD	Total Harmonic Distortion	f_{in} = 1 kHz, R_L = 10 kΩ, C_L = 50 pF $THD = THD_{Measured} - THD_{Source}$ V_{IS} = 4.0 V_{PP} sine wave	 4.5	 0.04	%
C_S	Switch Input Capacitance			5	pF
C_{COM}	Switch Common Capacitance			45	pF

* Limits not tested. Determined by design and verified by qualification.

TYPICAL CHARACTERISTICS

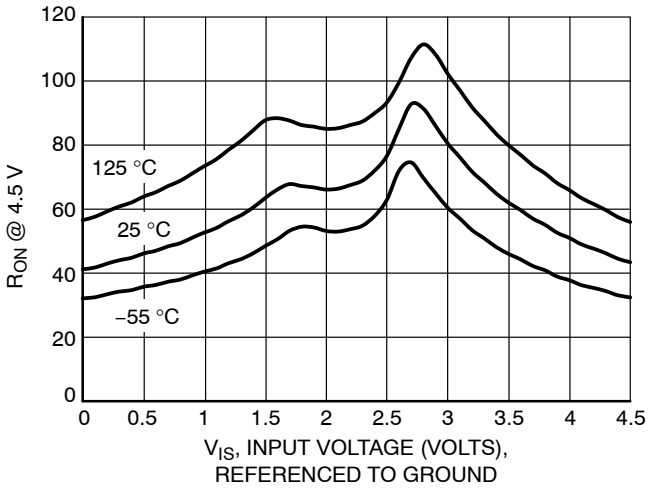


Figure 3. Typical On Resistance, V_{CC} = 4.5 V

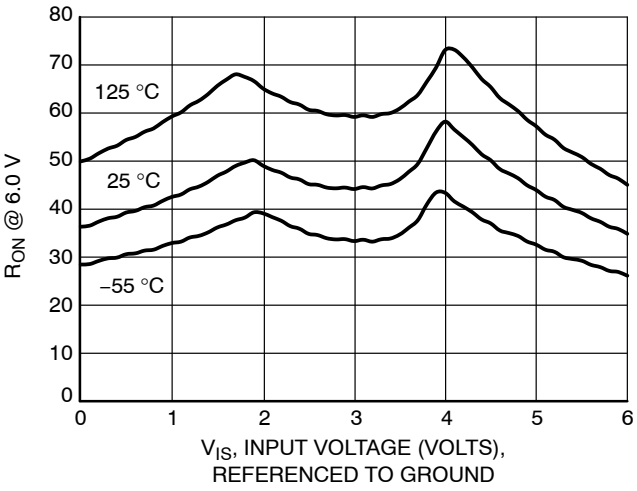


Figure 4. Typical On Resistance, V_{CC} = 6.0 V

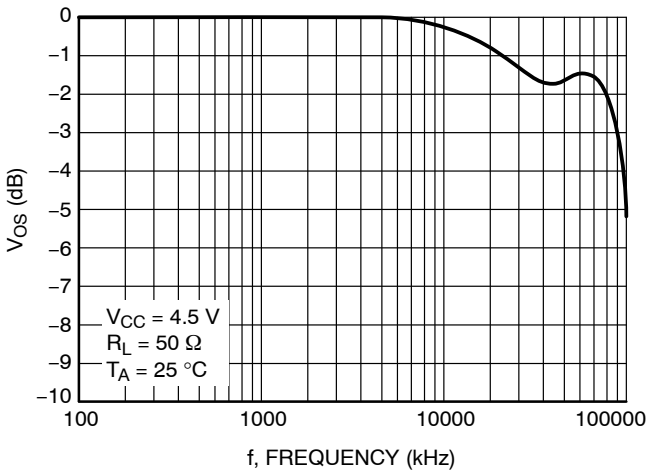


Figure 5. Typical Switch Frequency Response

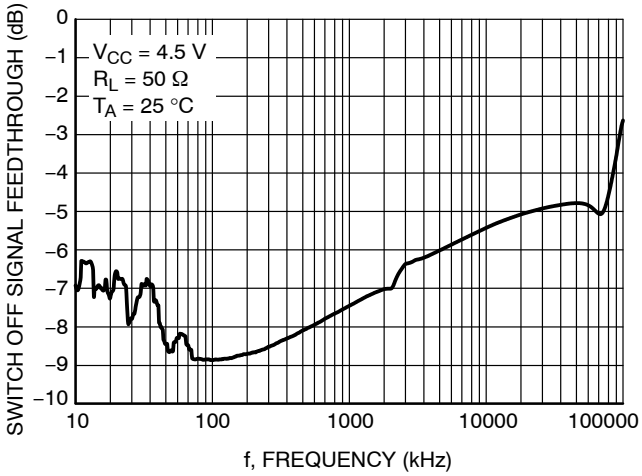


Figure 6. Typical Switch OFF Signal Feedthrough vs Frequency

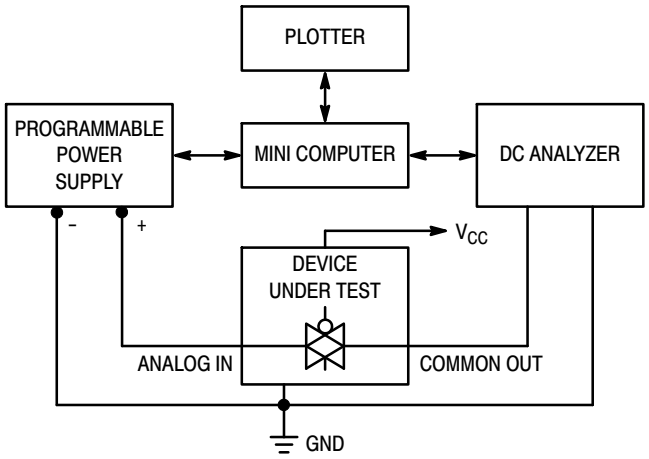


Figure 7. On Resistance Test Setup

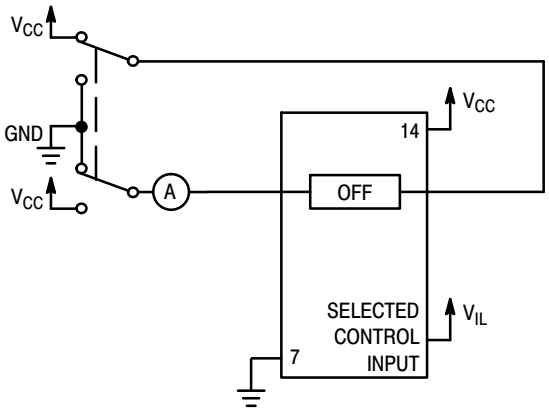


Figure 8. OFF Channel Leakage Current Test Setup, Any One Channel

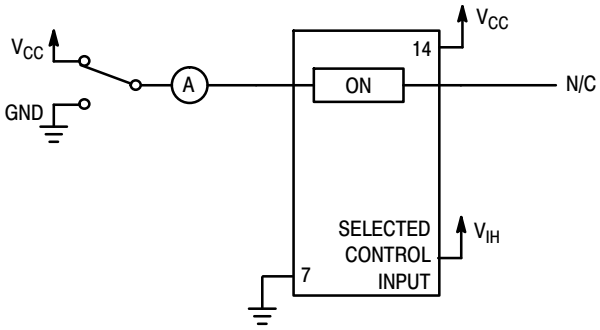


Figure 9. ON Channel Leakage Current Test Setup

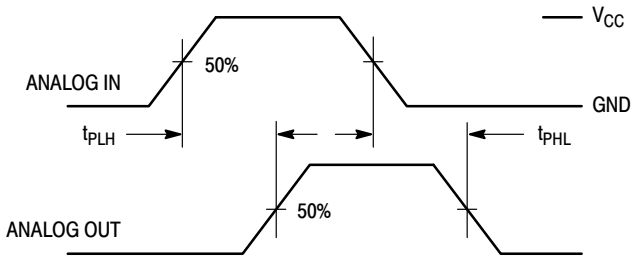
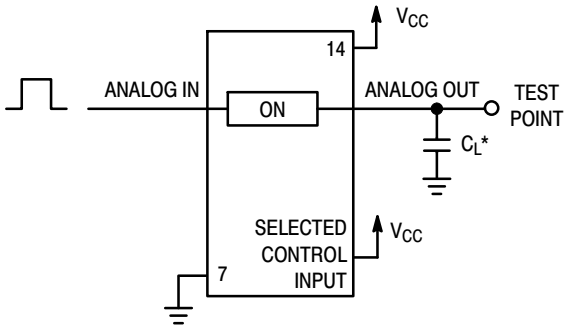


Figure 10. Propagation Delay, Analog In to Analog Out



*Includes all probe and jig capacitance.

Figure 11. Propagation Delay Test Setup

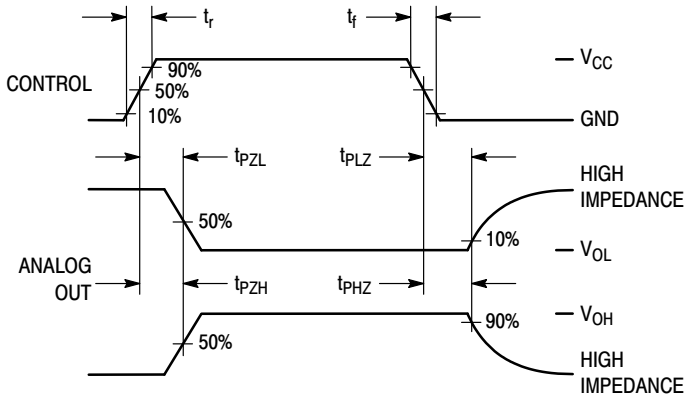
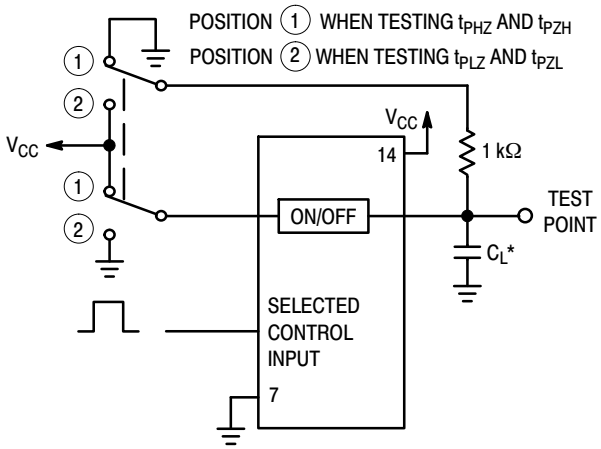


Figure 12. Turn-ON / Turn-OFF Times



*Includes all probe and jig capacitance.

Figure 13. Turn-ON / Turn-OFF Time Test Setup

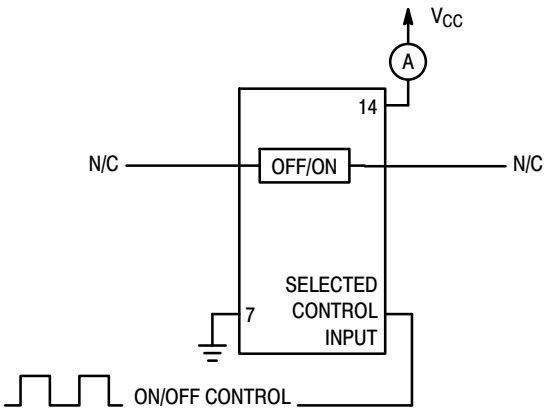
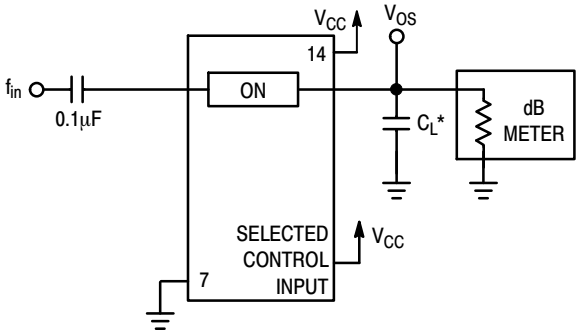
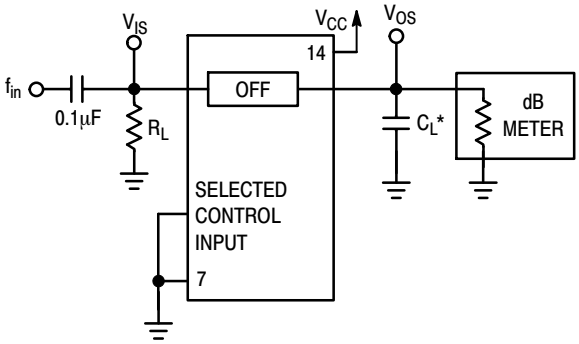


Figure 14. Power Dissipation Capacitance Test Setup



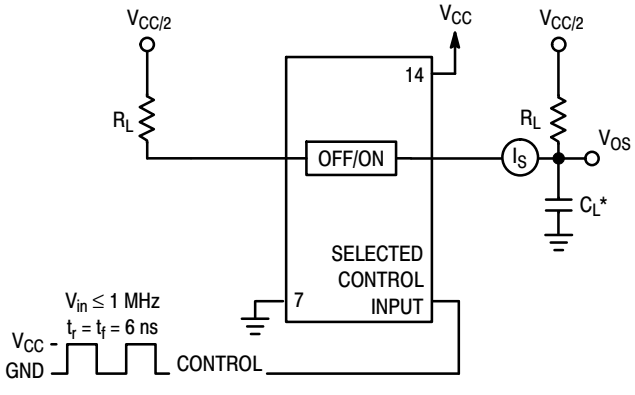
*Includes all probe and jig capacitance.

Figure 15. ON Channel Bandwidth Test Setup



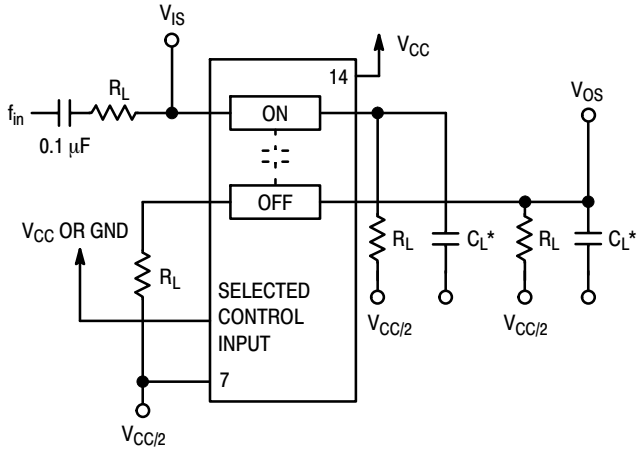
*Includes all probe and jig capacitance.

Figure 16. OFF Channel Feedthrough Isolation Test Setup



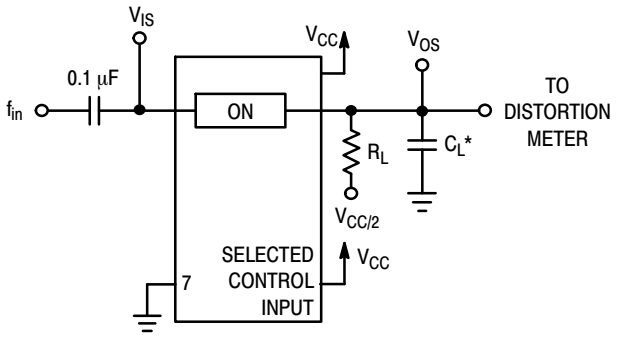
*Includes all probe and jig capacitance.

Figure 17. Feedthrough Noise Test Setup



*Includes all probe and jig capacitance.

Figure 18. Crosstalk Between Any Two Switches Test Setup



*Includes all probe and jig capacitance.

Figure 19. Total Harmonic Distortion Test Setup

ORDERING INFORMATION

Device	Package	Shipping†
NLV74HC4067ADTR2G*	TSSOP-24 (Pb-Free)	2500 / Tape & Reel

DISCONTINUED (Note 5)

Device	Package	Shipping†
MC74HC4067ADTG	TSSOP-24 (Pb-Free)	62 Units / Tube
MC74HC4067ADTR2G	TSSOP-24 (Pb-Free)	2500 / Tape & Reel
MC74HC4067ADWG	SOIC-24 (Pb-Free)	30 Units / Tube
MC74HC4067ADWR2G	SOIC-24 (Pb-Free)	1000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

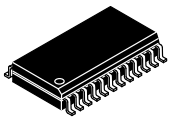
* NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

5. **DISCONTINUED:** These devices are not available. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

REVISION HISTORY

Revision	Description of Changes	Date
4	MC74HC4067ADTR2G and MC74HC4067ADWR2G OPNs Marked as Discontinued.	7/16/2026

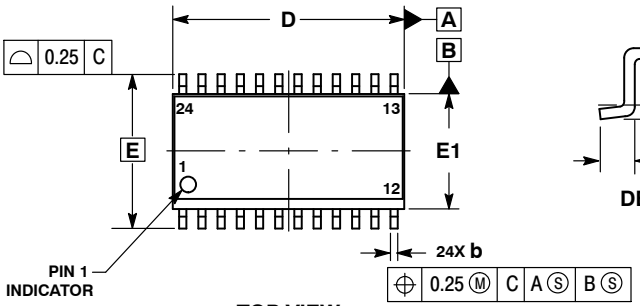
* Please note that this document has been previously updated prior to the inclusion of this revision history table and that the changes tracked only reflect what has occurred on the noted approval dates.

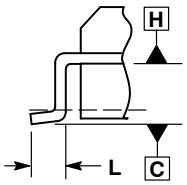


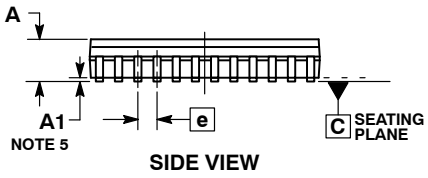
SCALE 1:1

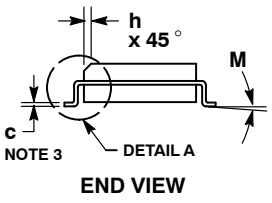
SOIC−24 WB
CASE 751E−04
ISSUE F

DATE 03 JUL 2012





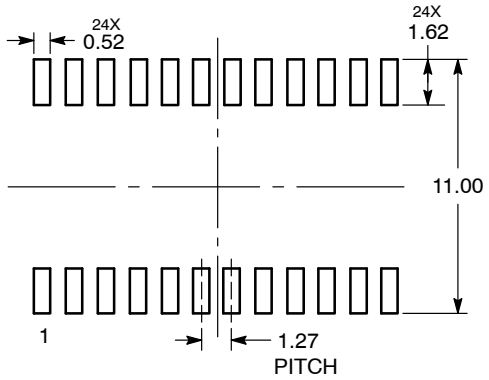




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD AND ARE MEASURED BETWEEN 0.10 AND 0.25 FROM THE LEAD TIP.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.13	0.29
b	0.35	0.49
c	0.23	0.32
D	15.25	15.54
E	10.30 BSC	
E1	7.40	7.60
e	1.27 BSC	
h	0.25	0.75
L	0.41	0.90
M	0 °	8 °

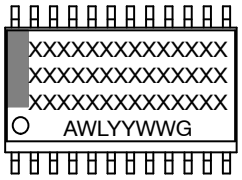
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



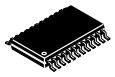
XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98ASB42344B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SOIC−24 WB**	**PAGE 1 OF 1**

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

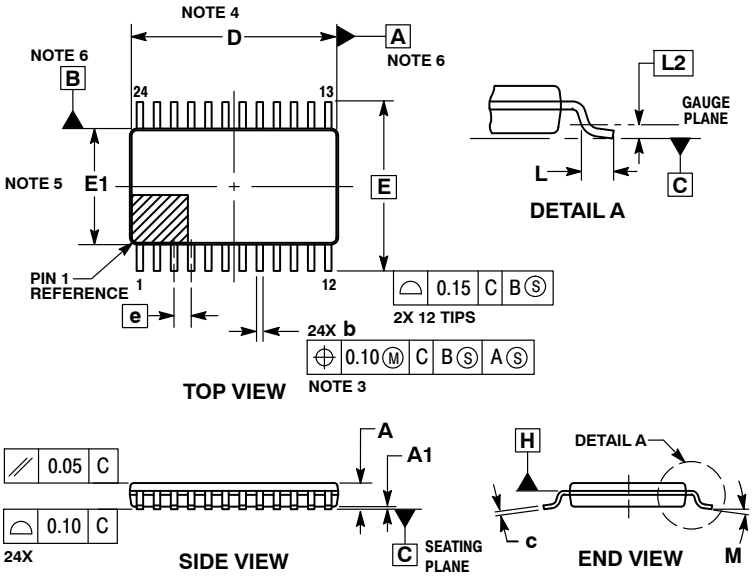
© Semiconductor Components Industries, LLC, 2019



SCALE 1:1

TSSOP24 7.8x4.4, 0.65P
CASE 948H
ISSUE B

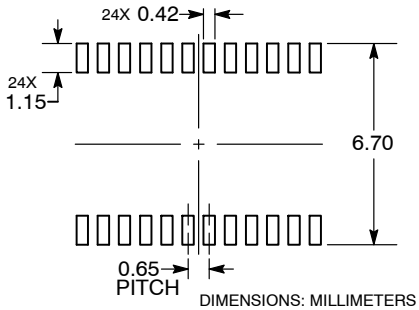
DATE 21 JUN 2012



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.08 MAX AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D IS DETERMINED AT DATUM PLANE H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM PLANE H.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.20
A1	0.05	0.15
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BSC	
E1	4.30	4.50
e	0.65 BSC	
L	0.50	0.75
L2	0.25 BSC	
M	0°	8°

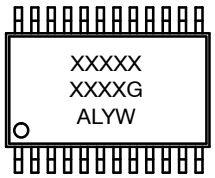
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98ASH70248A**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**TSSOP24 7.8X4.4, 0.65P**		**PAGE 1 OF 1**

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, ONSEMI , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales