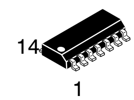
Single Supply Quad Operational Amplifiers

MC3403, MC3303

The MC3403 is a low cost, quad operational amplifier with true differential inputs. The device has electrical characteristics similar to the popular MC1741C. However, the MC3403 has several distinct advantages over standard operational amplifier types in single supply applications. The quad amplifier can operate at supply voltages as low as 3.0 V or as high as 36 V with quiescent currents about one third of those associated with the MC1741C (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

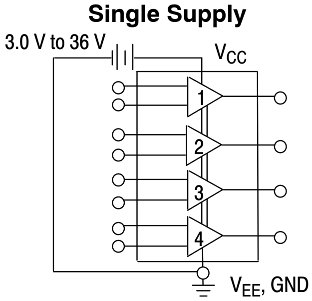


SOIC−14
D SUFFIX
CASE 751A

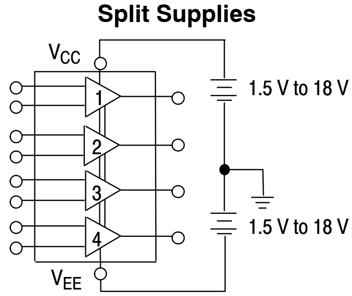
Features

- Short Circuit Protected Outputs
- Class AB Output Stage for Minimal Crossover Distortion
- True Differential Input Stage
- Single Supply Operation: 3.0 V to 36 V
- Split Supply Operation: ±1.5 V to ±18 V
- Low Input Bias Currents: 500 nA Max
- Four Amplifiers Per Package
- Internally Compensated
- Similar Performance to Popular MC1741C
- Industry Standard Pin−outs
- ESD Diodes Added for Increased Ruggedness
- Pb−Free Packages are Available

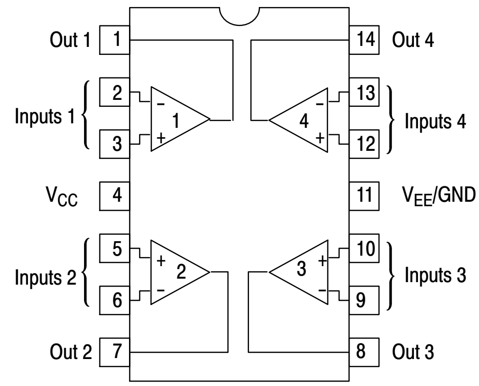
Single Supply



Split Supplies

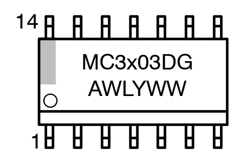


PIN CONNECTIONS



(Top View)

MARKING DIAGRAM



x = 3 or 4
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 8.

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
 V_{CC} V_{CC}, V_{EE}	Power Supply Voltages Single Supply Split Supplies	 36 ±18	Vdc
V_{IDR}	Input Differential Voltage Range (Note 1)	±36	Vdc
V_{ICR}	Input Common Mode Voltage Range (Notes 1 and 2)	±18	Vdc
T_{stg}	Storage Temperature Range	−55 to +125	°C
T_A	Operating Ambient Temperature Range MC3303 MC3403	 −40 to +85 0 to +70	°C
T_J	Junction Temperature	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Split power supplies.
2. For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +15 V, V_{EE} = −15 V for MC3403; V_{CC} = +14 V, V_{EE} = GND for MC3303 T_A = 25°C, unless otherwise noted.)

Symbol	Characteristic	MC3403			MC3303			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage T_A = T_{high} to T_{low} (Note 3)	– –	2.0 –	10 12	– –	2.0 –	8.0 10	mV
I_{IO}	Input Offset Current T_A = T_{high} to T_{low}	– –	30 –	50 200	– –	30 –	75 250	nA
A_{VOL}	Large Signal Open Loop Voltage Gain V_O = ±10 V, R_L = 2.0 kΩ T_A = T_{high} to T_{low}	 20 15	 200 –	 – –	 20 15	 200 –	 – –	V/mV
I_{IB}	Input Bias Current T_A = T_{high} to T_{low}	– –	−200 –	−500 −800	– –	−200 –	−500 −1000	nA
z_o	Output Impedance f = 20 Hz	–	75	–	–	75	–	Ω
z_i	Input Impedance f = 20 Hz	0.3	1.0	–	0.3	1.0	–	MΩ
V_O	Output Voltage Range R_L = 10 kΩ R_L = 2.0 kΩ R_L = 2.0 kΩ, T_A = T_{high} to T_{low}	 ±12 ±10 ±10	 ±13.5 ±13 –	 – – –	 12 10 10	 12.5 12 –	 – – –	V
V_{ICR}	Input Common Mode Voltage Range	+13 V $-V_{EE}$	+13 V $-V_{EE}$	–	+12 V $-V_{EE}$	+12.5 V $-V_{EE}$	–	V
CMR	Common Mode Rejection R_S ≤ 10 kΩ	70	90	–	70	90	–	dB
I_{CC}, I_{EE}	Power Supply Current (V_O = 0) R_L = ∞	–	2.8	7.0	–	2.8	7.0	mA
I_{SC}	Individual Output Short−Circuit Current (Note 4)	±10	±20	±45	±10	±30	±45	mA
PSRR+	Positive Power Supply Rejection Ratio	–	30	150	–	30	150	μV/V
PSRR−	Negative Power Supply Rejection Ratio	–	30	150	–	30	150	μV/V
$\Delta I_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Current T_A = T_{high} to T_{low}	–	50	–	–	50	–	pA/°C
$\Delta V_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage T_A = T_{high} to T_{low}	–	10	–	–	10	–	μV/°C
BWp	Power Bandwidth A_V = 1, R_L = 10 kΩ, V_O = 20 V(p−p), THD = 5%	–	9.0	–	–	9.0	–	kHz
BW	Small−Signal Bandwidth A_V = 1, R_L = 10 kΩ, V_O = 50 mV	–	1.0	–	–	1.0	–	MHz
SR	Slew Rate A_V = 1, V_i = −10 V to +10 V	–	0.6	–	–	0.6	–	V/μs
t_{TLH}	Rise Time A_V = 1, R_L = 10 kΩ, V_O = 50 mV	–	0.35	–	–	0.35	–	μs
t_{TLH}	Fall Time A_V = 1, R_L = 10 kΩ, V_O = 50 mV	–	0.35	–	–	0.35	–	μs
os	Overshoot A_V = 1, R_L = 10 kΩ, V_O = 50 mV	–	20	–	–	20	–	%
φm	Phase Margin A_V = 1, R_L = 2.0 kΩ, V_O = 200 pF	–	60	–	–	60	–	°
–	Crossover Distortion (V_{in} = 30 mVpp,V_{out}= 2.0 Vpp, f = 10 kHz)	–	1.0	–	–	1.0	–	%

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. MC3303: T_{low} = −40°C, T_{high} = +85°C, MC3403: T_{low} = 0°C, T_{high} = +70°C
4. Not to exceed maximum package power dissipation.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = GND, T_A = 25°C, unless otherwise noted.)

Symbol	Characteristic	MC3403			MC3303			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage	–	2.0	10	–	–	10	mV
I_{IO}	Input Offset Current	–	30	50	–	–	75	nA
I_{IB}	Input Bias Current	–	–200	–500	–	–	–500	nA
A_{VOL}	Large Signal Open Loop Voltage Gain R_L = 2.0 kΩ	10	200	–	10	200	–	V/mV
PSRR	Power Supply Rejection Ratio	–	–	150	–	–	150	μV/V
V_{OR}	Output Voltage Range (Note 5) R_L = 10 kΩ, V_{CC} = 5.0 V R_L = 10 kΩ, 5.0 ≤ V_{CC} ≤ 30 V	 3.3 V_{CC}–2.0	 3.5 V_{CC}–1.7	 – –	 3.3 V_{CC}–2.0	 3.5 V_{CC}–1.7	 – –	V_{pp}
I_{CC}	Power Supply Current	–	2.5	7.0	–	2.5	7.0	mA
CS	Channel Separation f = 1.0 kHz to 20 kHz (Input Referenced)	–	–120	–	–	–120	–	dB

5. Output will swing to ground with a 10 kΩ pull down resistor.

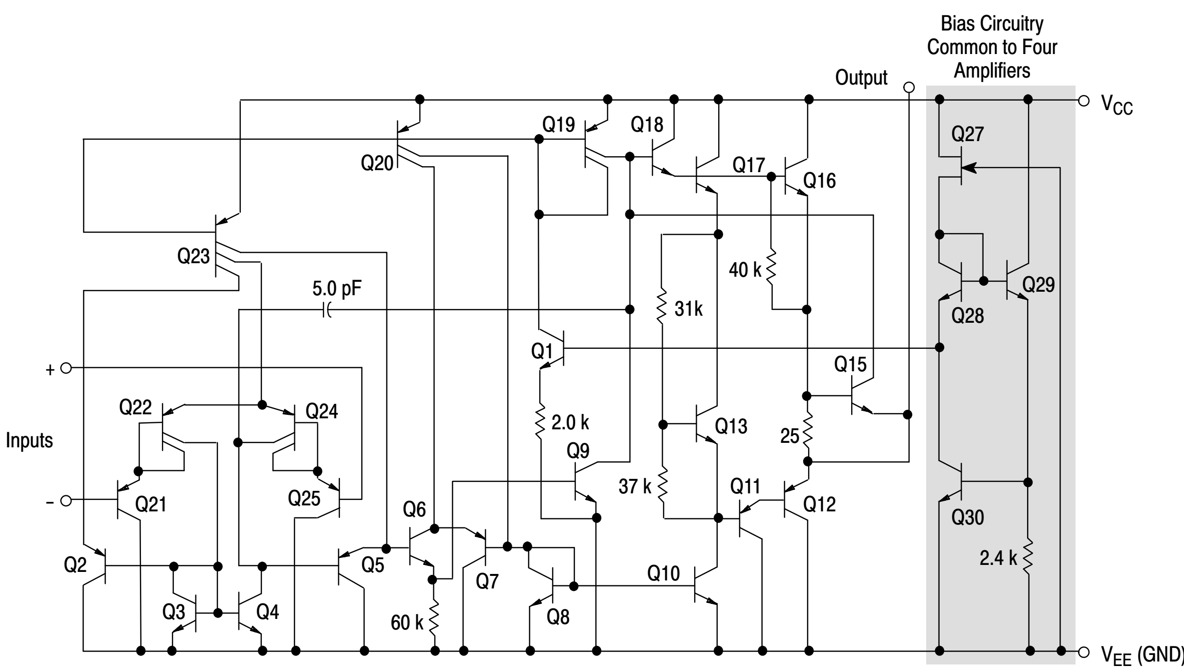


Figure 1. Representative Schematic Diagram
(1/4 of Circuit Shown)

CIRCUIT DESCRIPTION

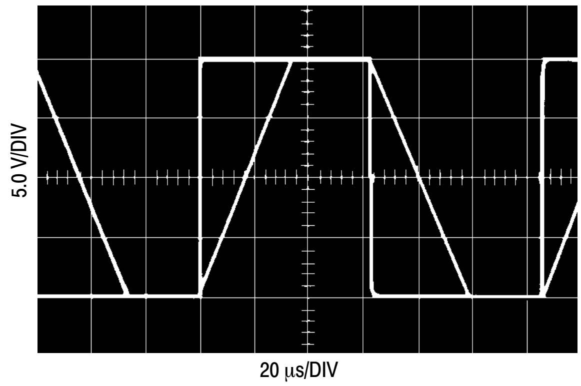


Figure 2. Inverter Pulse Response

The MC3403/3303 is made using four internally compensated, two–stage operational amplifiers. The first stage of each consists of differential input device Q24 and Q22 with input buffer transistors Q25 and Q21 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and Transconductance reduction functions. By reducing the Transconductance, a smaller compensation capacitor (only 5.0 pF) can be employed, thus saving chip area. The Transconductance reduction is accomplished by splitting the collectors of Q24 and Q22. Another feature of this input stage is that the input common mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single–ended converter. The second stage consists of a standard current source load amplifier stage.

The output stage is unique because it allows the output to swing to ground in single supply operation and yet does not exhibit any crossover distortion in split supply operation. This is possible because Class AB operation is utilized.

Each amplifier is biased from an internal voltage regulator which has a low temperature coefficient, thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

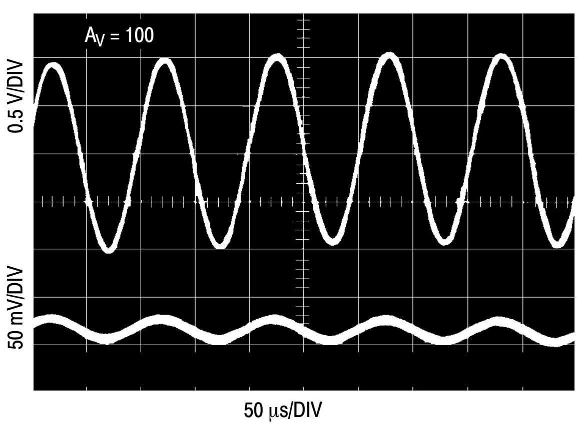


Figure 3. Sine Wave Response

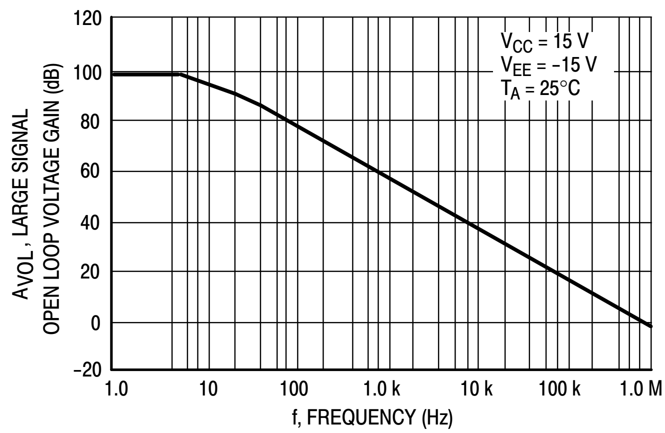


Figure 4. Open Loop Frequency Response

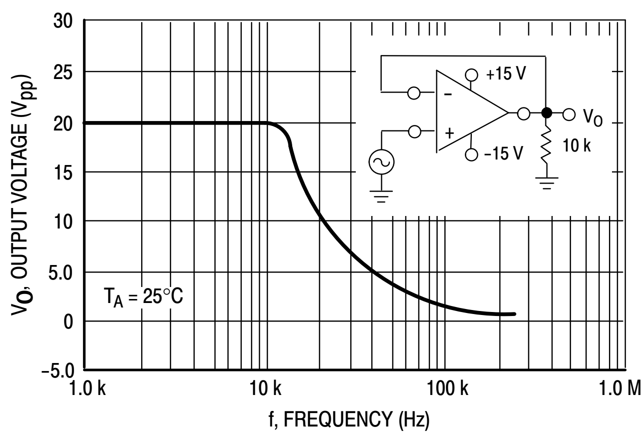


Figure 5. Power Bandwidth

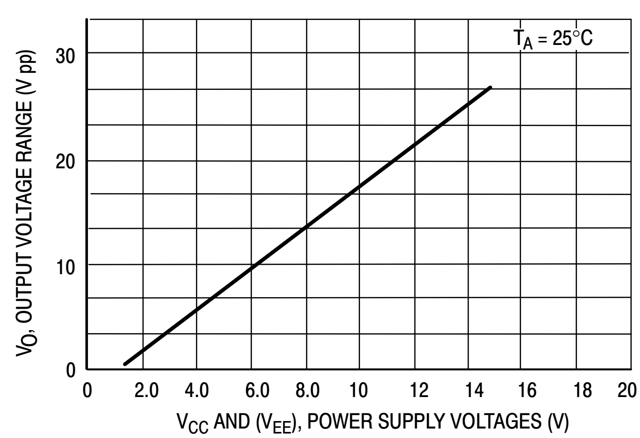


Figure 6. Output Swing versus Supply Voltage

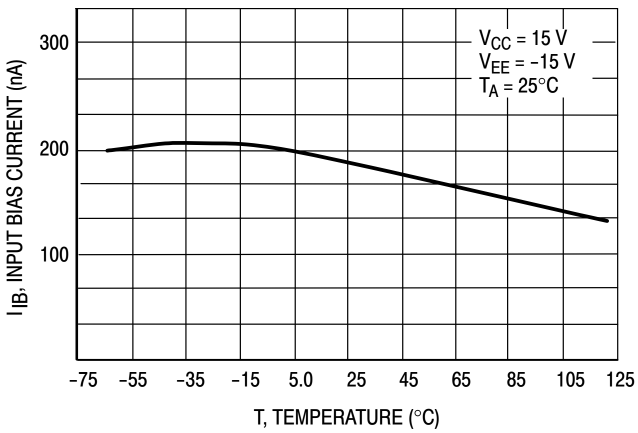


Figure 7. Input Bias Current versus Temperature

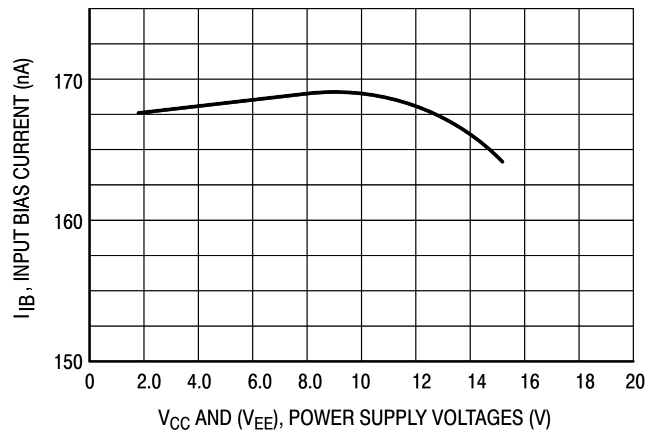


Figure 8. Input Bias Current versus Supply Voltage

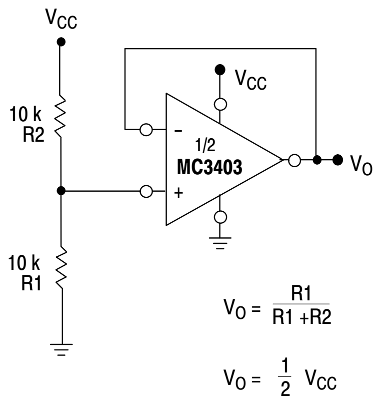


Figure 9. Voltage Reference

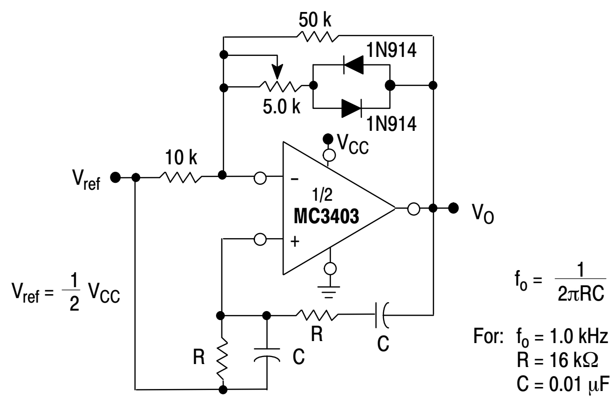


Figure 10. Wien Bridge Oscillator

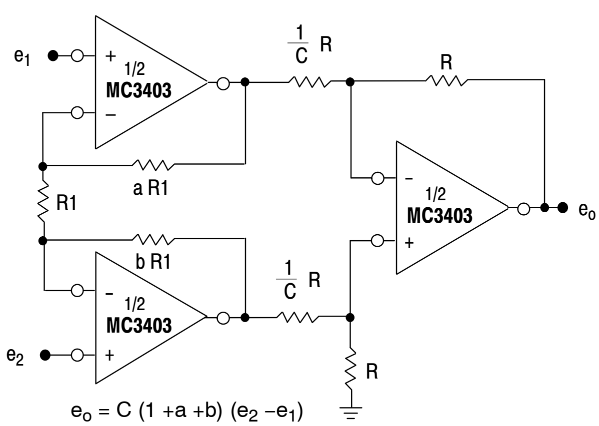


Figure 11. High Impedance Differential Amplifier

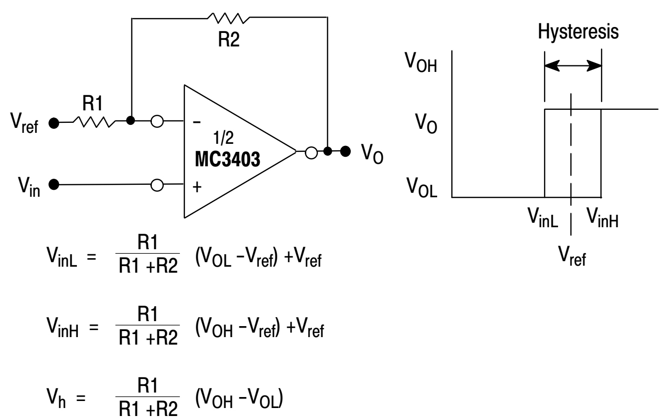


Figure 12. Comparator with Hysteresis

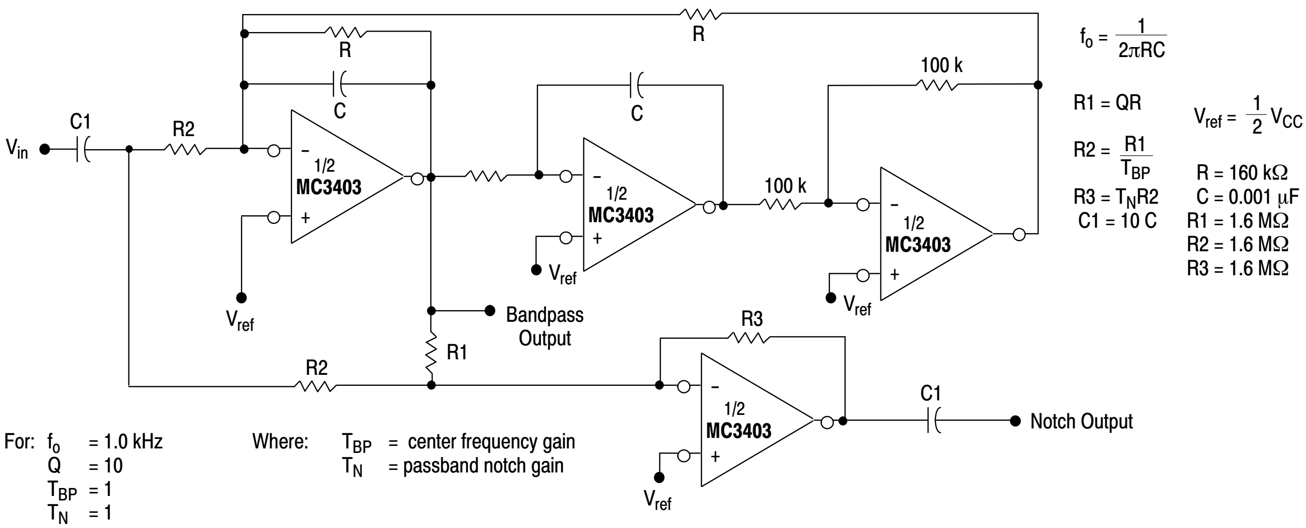
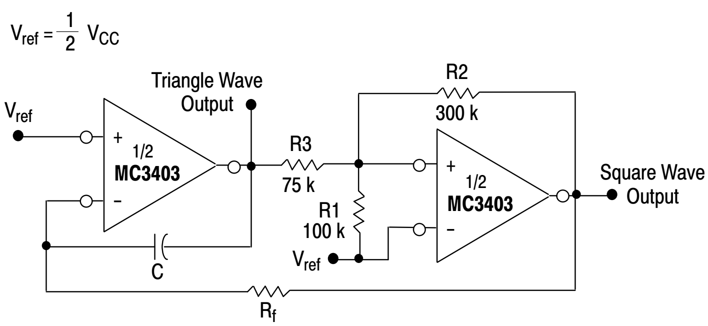
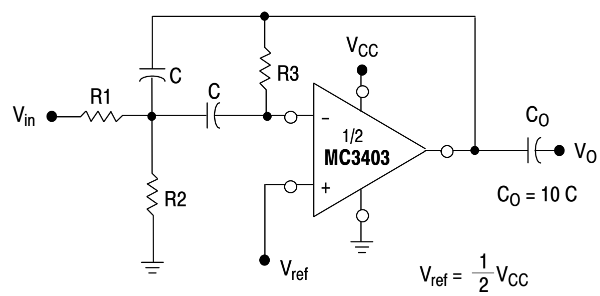


Figure 13. Bi−Quad Filter



$$f = \frac{R1 + R_C}{4\ CR_f\ R1} \quad \text{if } R3 = \frac{R2\ R1}{R2 + R1}$$

Figure 14. Function Generator



Given: f_o = center frequency

$A(f_o)$ = gain at center frequency

Choose value f_o, C

Then: $R3 = \frac{Q}{\pi f_o C}$ $R1 = \frac{R3}{2\ A(f_o)}$ $R2 = \frac{R1\ R5}{4Q^2\ R1 - R5}$

For less than 10% error from operational amplifier $\frac{O_o f_o}{BW} < 0.1$ where f_o and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

Figure 15. Multiple Feedback Bandpass Filter

ORDERING INFORMATION

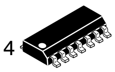
Device	Package	Shipping†
MC3303DR2G	SOIC−14 (Pb−Free)	2,500 Tape & Reel
MC3403DR2G	SOIC−14 (Pb−Free)	2,500 Tape & Reel

DISCONTINUED (Note 6)

MC3303D	SOIC−14	55 Units / Rail
MC3303DG	SOIC−14 (Pb−Free)	
MC3303DR2	SOIC−14	2,500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

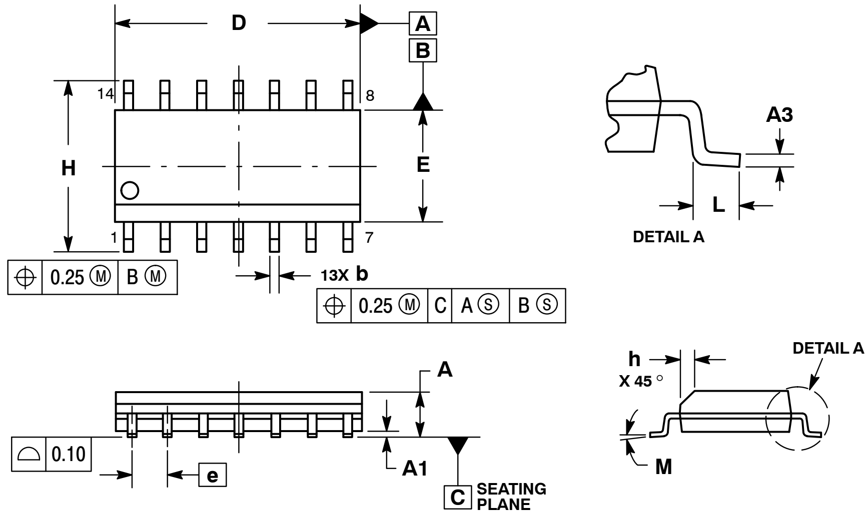
6. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.



SCALE 1:1

SOIC−14 NB
CASE 751A−03
ISSUE L

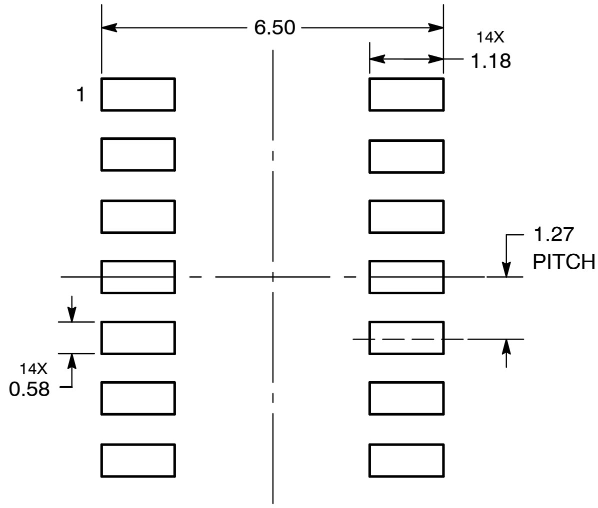
DATE 03 FEB 2016



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

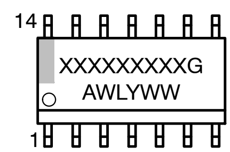
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42565B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SOIC−14 NB	PAGE 1 OF 2

SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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