# Programmable Timer

# MC14536B

The MC14536B programmable timer is a 24-stage binary ripple counter with 16 stages selectable by a binary code. Provisions for an on-chip RC oscillator or an external clock are provided. An on-chip monostable circuit incorporating a pulse-type output has been included. By selecting the appropriate counter stage in conjunction with the appropriate input clock frequency, a variety of timing can be achieved.

### Features

- 24 Flip-Flop Stages − Will Count From $2^0$ to $2^{24}$
- Last 16 Stages Selectable By Four-Bit Select Code
- 8-Bypass Input Allows Bypassing of First Eight Stages
- Set and Reset Inputs
- Clock Inhibit and Oscillator Inhibit Inputs
- On-Chip RC Oscillator Provisions
- On-Chip Monostable Output Provisions
- Clock Conditioning Circuit Permits Operation with Very Long Rise and Fall Times
- Test Mode Allows Fast Test Sequence
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

**MAXIMUM RATINGS** (Voltages Referenced to $V_{SS}$)

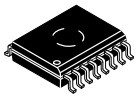
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| DC Supply Voltage Range | $V_{DD}$ | −0.5 to +18.0 | V |
| Input or Output Voltage Range (DC or Transient) | $V_{in}$, $V_{out}$ | −0.5 to $V_{DD}$ + 0.5 | V |
| Input or Output Current (DC or Transient) per Pin | $I_{in}$, $I_{out}$ | ±10 | mA |
| Power Dissipation per Package (Note 1) | $P_D$ | 500 | mW |
| Ambient Temperature Range | $T_A$ | −55 to +125 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |
| Lead Temperature, (8-Second Soldering) | $T_L$ | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. Operating the device outside its recommended conditions, but still within its maximum rated limits may not cause immediate damage. However, doing so can lead to reduced performance, unpredictable behavior, and potentially shorten the device's lifespan or reliability.

1. Temperature Derating: "D/DW" Packages: –7.0 mW/°C from 65 °C to 125 °C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$). Unused outputs must be left open.



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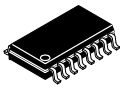
**SOIC-16 WB**
**DW SUFFIX**
**CASE 751G**



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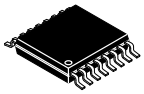
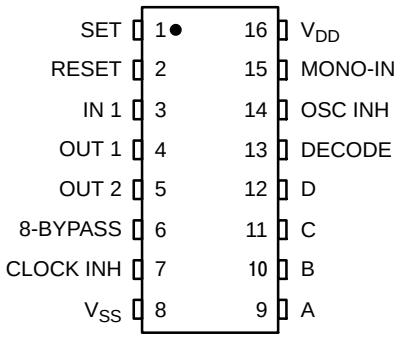
**SOEIAJ-16**
**F SUFFIX**
**CASE 966**



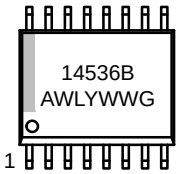
1

**TSSOP-16**
**DT SUFFIX**
**CASE 948F**

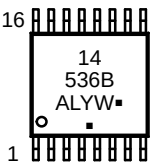
### PIN ASSIGNMENT



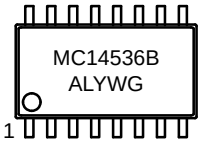

### MARKING DIAGRAMS




**SOIC-16 WB**




**TSSOP-16**




**SOEIAJ-16**

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 12.

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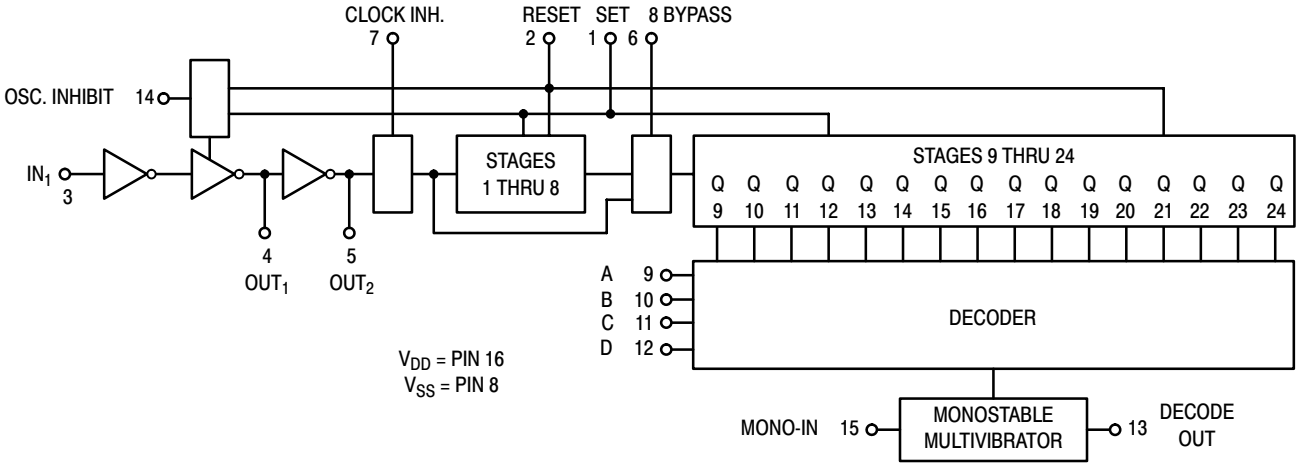


**Figure 1. Block Diagram**

## FUNCTION TABLE

| $In_1$ | Set | Reset | Clock Inh | OSC Inh | Out 1 | Out 2 | Decode Out |
|---|---|---|---|---|---|---|---|
| ⎍ | 0 | 0 | 0 | 0 | ⎍ | ⎺ | No Change |
| ⎺ | 0 | 0 | 0 | 0 | ⎺ | ⎍ | Advance to next state |
| X | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| X | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| X | 0 | 0 | 1 | 0 | – | – | No Change |
| X | 0 | 0 | 0 | 1 | 0 | 1 | No Change |
| 0 | 0 | 0 | 0 | X | 0 | 1 | No Change |
| 1 | 0 | 0 | 0 | ⎍ | ⎺ | ⎍ | Advance to next state |

X = Don't Care



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**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to $V_{SS}$)

| Characteristic | Symbol | $V_{DD}$ Vdc | −55 °C Min | −55 °C Max | 25 °C Min | 25 °C Typ (Note 2) | 25 °C Max | 125 °C Min | 125 °C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Output Voltage “0” Level<br>$V_{in}$ = $V_{DD}$ or 0 | $V_{OL}$ | 5.0<br>10<br>15 | –<br>–<br>– | 0.05<br>0.05<br>0.05 | –<br>–<br>– | 0<br>0<br>0 | 0.05<br>0.05<br>0.05 | –<br>–<br>– | 0.05<br>0.05<br>0.05 | Vdc |
| “1” Level<br>$V_{in}$ = 0 or $V_{DD}$ | $V_{OH}$ | 5.0<br>10<br>15 | 4.95<br>9.95<br>14.95 | –<br>–<br>– | 4.95<br>9.95<br>14.95 | 5.0<br>10<br>15 | –<br>–<br>– | 4.95<br>9.95<br>14.95 | –<br>–<br>– | Vdc |
| Input Voltage “0” Level<br>($V_O$ = 4.5 or 0.5 Vdc)<br>($V_O$ = 9.0 or 1.0 Vdc)<br>($V_O$ = 13.5 or 1.5 Vdc) | $V_{IL}$ | 5.0<br>10<br>15 | –<br>–<br>– | 1.5<br>3.0<br>4.0 | –<br>–<br>– | 2.25<br>4.50<br>6.75 | 1.5<br>3.0<br>4.0 | –<br>–<br>– | 1.5<br>3.0<br>4.0 | Vdc |
| “1” Level<br>($V_O$ = 0.5 or 4.5 Vdc)<br>($V_O$ = 1.0 or 9.0 Vdc)<br>($V_O$ = 1.5 or 13.5 Vdc) | $V_{IH}$ | 5.0<br>10<br>15 | 3.5<br>7.0<br>11 | –<br>–<br>– | 3.5<br>7.0<br>11 | 2.75<br>5.50<br>8.25 | –<br>–<br>– | 3.5<br>7.0<br>11 | –<br>–<br>– | Vdc |
| Output Drive Current<br>($V_{OH}$ = 2.5 Vdc) Source<br>($V_{OH}$ = 4.6 Vdc) Pins 4 & 5<br>($V_{OH}$ = 9.5 Vdc)<br>($V_{OH}$ = 13.5 Vdc) | $I_{OH}$ | 5.0<br>5.0<br>10<br>15 | –1.2<br>–0.25<br>–0.62<br>–1.8 | –<br>–<br>–<br>– | –1.0<br>–0.25<br>–0.5<br>–1.5 | –1.7<br>–0.36<br>–0.9<br>–3.5 | –<br>–<br>–<br>– | –0.7<br>–0.14<br>–0.35<br>–1.1 | –<br>–<br>–<br>– | mAdc |
| ($V_{OH}$ = 2.5 Vdc) Source<br>($V_{OH}$ = 4.6 Vdc) Pin 13<br>($V_{OH}$ = 9.5 Vdc)<br>($V_{OH}$ = 13.5 Vdc) | | 5.0<br>5.0<br>10<br>15 | –3.0<br>–0.64<br>–1.6<br>–4.2 | –<br>–<br>–<br>– | –2.4<br>–0.51<br>–1.3<br>–3.4 | –4.2<br>–0.88<br>–2.25<br>–8.8 | –<br>–<br>–<br>– | –1.7<br>–0.36<br>–0.9<br>–2.4 | –<br>–<br>–<br>– | mAdc |
| ($V_{OL}$ = 0.4 Vdc) Sink<br>($V_{OL}$ = 0.5 Vdc)<br>($V_{OL}$ = 1.5 Vdc) | $I_{OL}$ | 5.0<br>10<br>15 | 0.64<br>1.6<br>4.2 | –<br>–<br>– | 0.51<br>1.3<br>3.4 | 0.88<br>2.25<br>8.8 | –<br>–<br>– | 0.36<br>0.9<br>2.4 | –<br>–<br>– | mAdc |
| Input Current | $I_{in}$ | 15 | – | ±0.1 | – | ±0.00001 | ±0.1 | – | ±1.0 | μAdc |
| Input Capacitance<br>($V_{in}$ = 0) | $C_{in}$ | – | – | – | – | 5.0 | 7.5 | – | – | pF |
| Quiescent Current (Per Package) | $I_{DD}$ | 5.0<br>10<br>15 | –<br>–<br>– | 5.0<br>10<br>20 | –<br>–<br>– | 0.010<br>0.020<br>0.030 | 5.0<br>10<br>20 | –<br>–<br>– | 150<br>300<br>600 | μAdc |
| Total Supply Current (Note 3, 4)<br>(Dynamic plus Quiescent,<br>Per Package)<br>($C_L$ = 50 pF on all outputs, all buffers switching) | $I_T$ | 5.0<br>10<br>15 | $I_T$ = (1.50 μA/kHz) f + $I_{DD}$<br>$I_T$ = (2.30 μA/kHz) f + $I_{DD}$<br>$I_T$ = (3.55 μA/kHz) f + $I_{DD}$ | | | | | | | μAdc |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
3. The formulas given are for the typical characteristics only at 25 °C.
4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: $I_T$ is in μA (per package), $C_L$ in pF, V = ($V_{DD}$ – $V_{SS}$) in volts, f in kHz is input frequency, and k = 0.003.



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**SWITCHING CHARACTERISTICS** (Note 5) ($C_L$ = 50 pF, $T_A$ = 25 °C)

| Characteristic | Symbol | $V_{DD}$ | Min | Typ (Note 6) | Max | Unit |
|---|---|---|---|---|---|---|
| Output Rise and Fall Time (Pin 13) | $t_{TLH}$, $t_{THL}$ | | | | | ns |
| $t_{TLH}$, $t_{THL}$ = (1.5 ns/pF) $C_L$ + 25 ns | | 5.0 | – | 100 | 200 | |
| $t_{TLH}$, $t_{THL}$ = (0.75 ns/pF) $C_L$ + 12.5 ns | | 10 | – | 50 | 100 | |
| $t_{TLH}$, $t_{THL}$ = (0.55 ns/pF) $C_L$ + 9.5 ns | | 15 | – | 40 | 80 | |
| Propagation Delay Time | $t_{PLH}$, $t_{PHL}$ | | | | | ns |
| Clock to Q1, 8−Bypass (Pin 6) High | | | | | | |
| $t_{PLH}$, $t_{PHL}$ = (1.7 ns/pF) $C_L$ + 1715 ns | | 5.0 | – | 1800 | 3600 | |
| $t_{PLH}$, $t_{PHL}$ = (0.66 ns/pF) $C_L$ + 617 ns | | 10 | – | 650 | 1300 | |
| $t_{PLH}$, $t_{PHL}$ = (0.5 ns/pF) $C_L$ + 425 ns | | 15 | – | 450 | 1000 | |
| Clock to Q1, 8−Bypass (Pin 6) Low | $t_{PLH}$, $t_{PHL}$ | | | | | μs |
| $t_{PLH}$, $t_{PHL}$ = (1.7 ns/pF) $C_L$ + 3715 ns | | 5.0 | – | 3.8 | 7.6 | |
| $t_{PLH}$, $t_{PHL}$ = (0.66 ns/pF) $C_L$ + 1467 ns | | 10 | – | 1.5 | 3.0 | |
| $t_{PLH}$, $t_{PHL}$ = (0.5 ns/pF) $C_L$ + 1075 ns | | 15 | – | 1.1 | 2.3 | |
| Clock to Q16 | $t_{PLH}$, $t_{PHL}$ | | | | | μs |
| $t_{PHL}$, $t_{PLH}$ = (1.7 ns/pF) $C_L$ + 6915 ns | | 5.0 | – | 7.0 | 14 | |
| $t_{PHL}$, $t_{PLH}$ = (0.66 ns/pF) $C_L$ + 2967 ns | | 10 | – | 3.0 | 6.0 | |
| $t_{PHL}$, $t_{PLH}$ = (0.5 ns/pF) $C_L$ + 2175 ns | | 15 | – | 2.2 | 4.5 | |
| Reset to $Q_n$ | $t_{PHL}$ | | | | | ns |
| $t_{PHL}$ = (1.7 ns/pF) $C_L$ + 1415 ns | | 5.0 | – | 1500 | 3000 | |
| $t_{PHL}$ = (0.66 ns/pF) $C_L$ + 567 ns | | 10 | – | 600 | 1200 | |
| $t_{PHL}$ = (0.5 ns/pF) $C_L$ + 425 ns | | 15 | – | 450 | 900 | |
| Clock Pulse Width | $t_{WH}$ | 5.0 | 600 | 300 | – | ns |
| | | 10 | 200 | 100 | – | |
| | | 15 | 170 | 85 | – | |
| Clock Pulse Frequency (50% Duty Cycle) | $f_{cl}$ | 5.0 | – | 1.2 | 0.4 | MHz |
| | | 10 | – | 3.0 | 1.5 | |
| | | 15 | – | 5.0 | 2.0 | |
| Clock Rise and Fall Time | $t_{TLH}$, $t_{THL}$ | 5.0 | No Limit | | | – |
| | | 10 | | | | |
| | | 15 | | | | |
| Reset Pulse Width | $t_{WH}$ | 5.0 | 1000 | 500 | – | ns |
| | | 10 | 400 | 200 | – | |
| | | 15 | 300 | 150 | – | |

5. The formulas given are for the typical characteristics only at 25 °C.
6. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.



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## PIN DESCRIPTIONS

### INPUTS

**SET (Pin 1)** − A high on Set asynchronously forces Decode Out to a high level. This is accomplished by setting an output conditioning latch to a high level while at the same time resetting the 24 flip-flop stages. After Set goes low (inactive), the occurrence of the first negative clock transition on $IN_1$ causes Decode Out to go low. The counter's flip-flop stages begin counting on the second negative clock transition of $IN_1$. When Set is high, the on-chip RC oscillator is disabled. This allows for very low-power standby operation.

**RESET (Pin 2)** − A high on Reset asynchronously forces Decode Out to a low level; all 24 flip-flop stages are also reset to a low level. Like the Set input, Reset disables the on-chip RC oscillator for standby operation.

**$IN_1$ (Pin 3)** − The device's internal counters advance on the negative-going edge of this input. $IN_1$ may be used as an external clock input or used in conjunction with $OUT_1$ and $OUT_2$ to form an RC oscillator. When an external clock is used, both $OUT_1$ and $OUT_2$ may be left unconnected or used to drive 1 LSTTL or several CMOS loads.

**8-BYPASS (Pin 6)** − A high on this input causes the first 8 flip-flop stages to be bypassed. This device essentially becomes a 16-stage counter with all 16 stages selectable. Selection is accomplished by the A, B, C, and D inputs. (See the truth tables.)

**CLOCK INHIBIT (Pin 7)** − A high on this input disconnects the first counter stage from the clocking source. This holds the present count and inhibits further counting. However, the clocking source may continue to run. Therefore, when Clock Inhibit is brought low, no oscillator startup time is required. When Clock Inhibit is low, the counter will start counting on the occurrence of the first negative edge of the clocking source at $IN_1$.

**OSC INHIBIT (Pin 14)** − A high level on this pin stops the RC oscillator which allows for very low-power standby operation. May also be used, in conjunction with an external clock, with essentially the same results as the Clock Inhibit input.

**MONO-IN (Pin 15)** − Used as the timing pin for the on-chip monostable multivibrator. If the Mono-In input is connected to $V_{SS}$, the monostable circuit is disabled, and Decode Out is directly connected to the selected Q output. The monostable circuit is enabled if a resistor is connected between Mono-In and $V_{DD}$. This resistor and the device's internal capacitance will determine the minimum output pulse widths. With the addition of an external capacitor to $V_{SS}$, the pulse width range may be extended. For reliable operation the resistor value should be limited to the range of 5 kΩ to 100 kΩ and the capacitor value should be limited to a maximum of 1000 pf. (See figures 4, 5, 6, and 11).

**A, B, C, D (Pins 9, 10, 11, 12)** − These inputs select the flip-flop stage to be connected to Decode Out. (See the truth tables.)

### OUTPUTS

**$OUT_1$, $OUT_2$ (Pin 4, 5)** − Outputs used in conjunction with $IN_1$ to form an RC oscillator. These outputs are buffered and may be used for $2^0$ frequency division of an external clock.

**DECODE OUT (Pin 13)** − Output function depends on configuration. When the monostable circuit is disabled, this output is a 50% duty cycle square wave during free run.

### TEST MODE

The test mode configuration divides the 24 flip-flop stages into three 8-stage sections to facilitate a fast test sequence. The test mode is enabled when 8-Bypass, Set and Reset are at a high level. (See Figure 9.)

## TRUTH TABLES

| Input | | | | | Stage Selected for Decode Out |
|---|---|---|---|---|---|
| 8-Bypass | D | C | B | A | |
| 0 | 0 | 0 | 0 | 0 | 9 |
| 0 | 0 | 0 | 0 | 1 | 10 |
| 0 | 0 | 0 | 1 | 0 | 11 |
| 0 | 0 | 0 | 1 | 1 | 12 |
| 0 | 0 | 1 | 0 | 0 | 13 |
| 0 | 0 | 1 | 0 | 1 | 14 |
| 0 | 0 | 1 | 1 | 0 | 15 |
| 0 | 0 | 1 | 1 | 1 | 16 |
| 0 | 1 | 0 | 0 | 0 | 17 |
| 0 | 1 | 0 | 0 | 1 | 18 |
| 0 | 1 | 0 | 1 | 0 | 19 |
| 0 | 1 | 0 | 1 | 1 | 20 |
| 0 | 1 | 1 | 0 | 0 | 21 |
| 0 | 1 | 1 | 0 | 1 | 22 |
| 0 | 1 | 1 | 1 | 0 | 23 |
| 0 | 1 | 1 | 1 | 1 | 24 |

| Input | | | | | Stage Selected for Decode Out |
|---|---|---|---|---|---|
| 8-Bypass | D | C | B | A | |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 2 |
| 1 | 0 | 0 | 1 | 0 | 3 |
| 1 | 0 | 0 | 1 | 1 | 4 |
| 1 | 0 | 1 | 0 | 0 | 5 |
| 1 | 0 | 1 | 0 | 1 | 6 |
| 1 | 0 | 1 | 1 | 0 | 7 |
| 1 | 0 | 1 | 1 | 1 | 8 |
| 1 | 1 | 0 | 0 | 0 | 9 |
| 1 | 1 | 0 | 0 | 1 | 10 |
| 1 | 1 | 0 | 1 | 0 | 11 |
| 1 | 1 | 0 | 1 | 1 | 12 |
| 1 | 1 | 1 | 0 | 0 | 13 |
| 1 | 1 | 1 | 0 | 1 | 14 |
| 1 | 1 | 1 | 1 | 0 | 15 |
| 1 | 1 | 1 | 1 | 1 | 16 |



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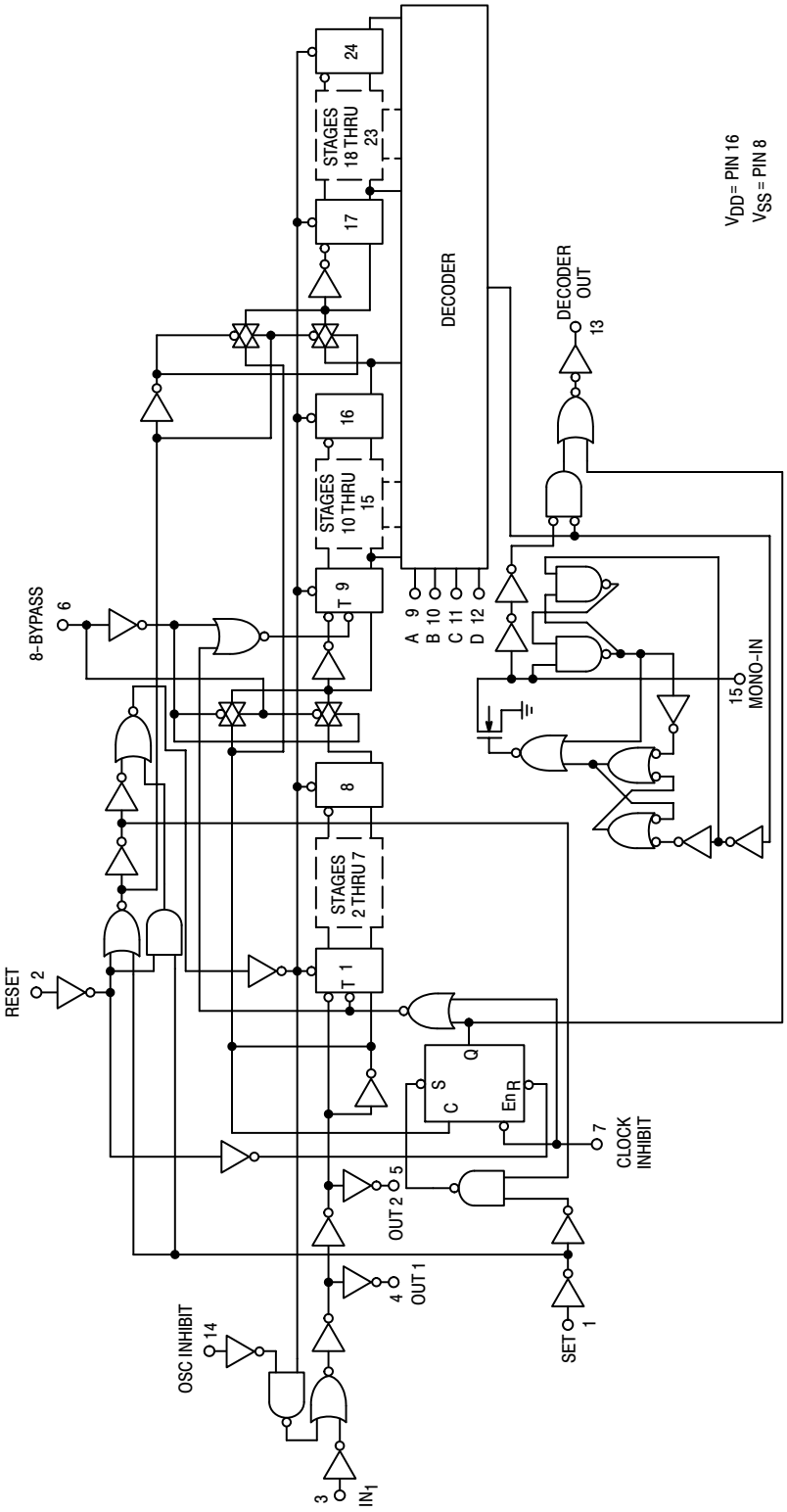
## LOGIC DIAGRAM



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## TYPICAL RC OSCILLATOR CHARACTERISTICS

**(For Circuit Diagram See Figure 12 In Application)**

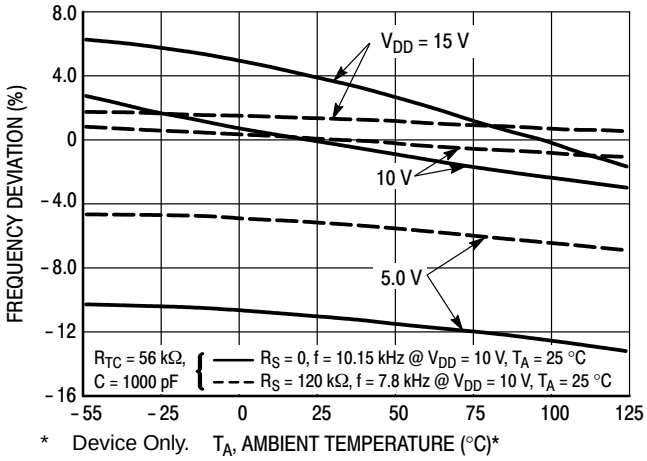


**Figure 2. RC Oscillator Stability**

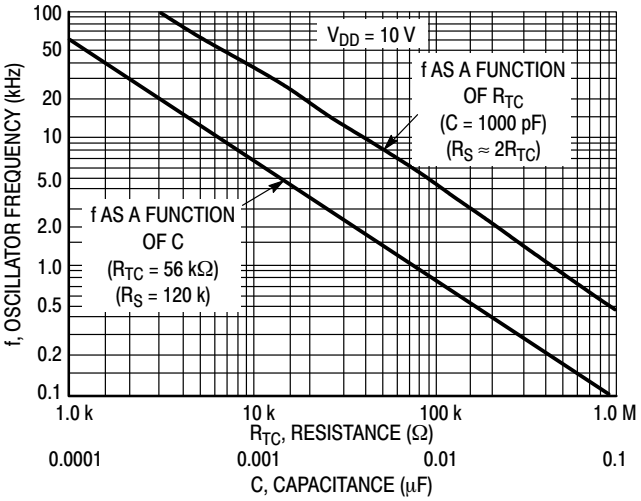


**Figure 3. RC Oscillator Frequency as a Function of $R_{TC}$ and C**

## MONOSTABLE CHARACTERISTICS

**(FOR CIRCUIT DIAGRAM SEE FIGURE 11 IN APPLICATION)**

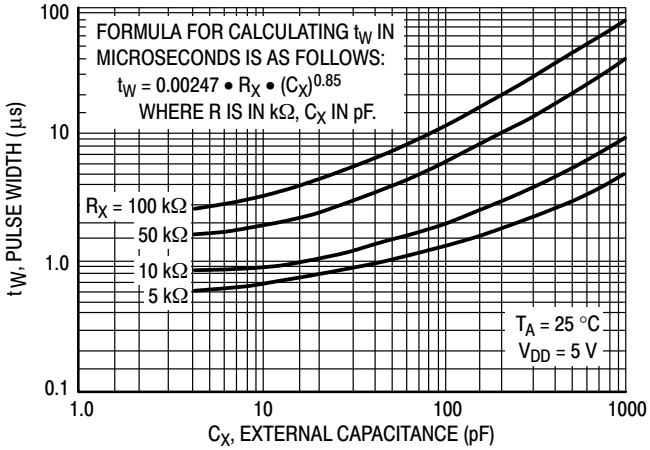


**Figure 4. Typical $C_X$ versus Pulse Width @ $V_{DD}$ = 5.0 V**

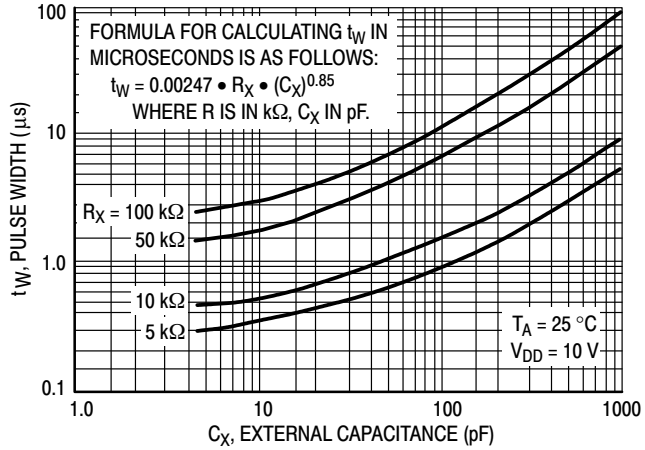


**Figure 5. Typical $C_X$ versus Pulse Width @ $V_{DD}$ = 10 V**

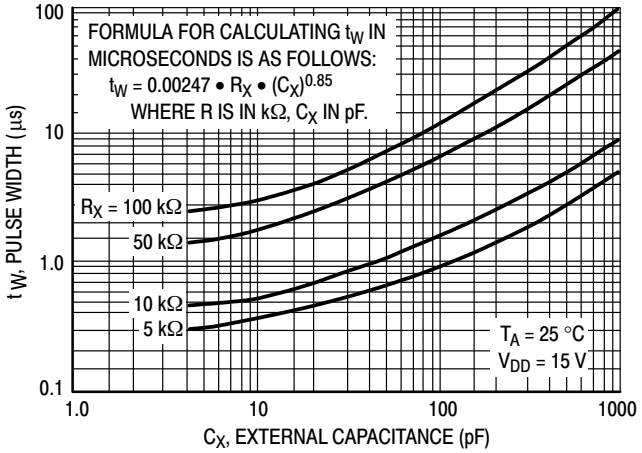


**Figure 6. Typical $C_X$ versus Pulse Width @ $V_{DD}$ = 15 V**



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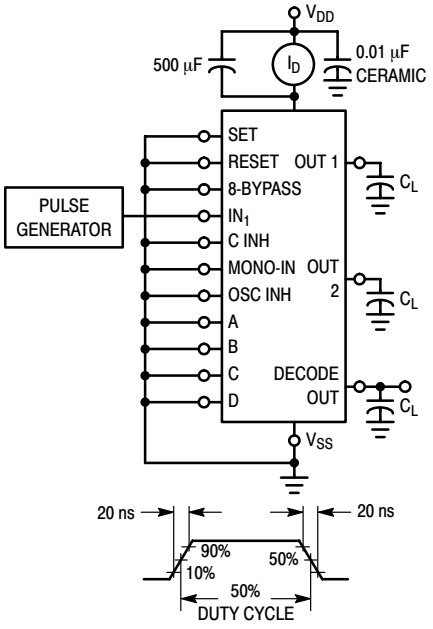


**Figure 7. Power Dissipation Test Circuit and Waveform**

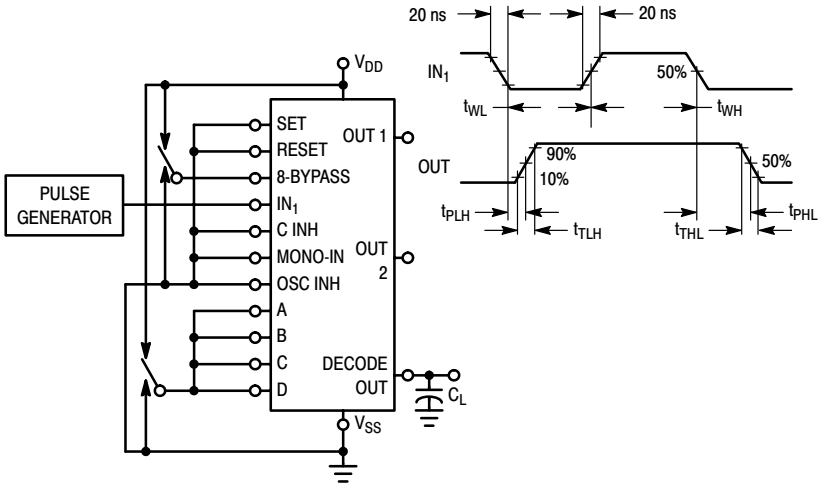


**Figure 8. Switching Time Test Circuit and Waveforms**

## FUNCTIONAL TEST SEQUENCE

Test function (Figure 9) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections and 255 counts are loaded in each of the 8-stage sections in parallel. All flip-flops are now at a “1”. The counter is now returned to the normal 24-stages in series configuration. One more pulse is entered into $In_1$ which will cause the counter to ripple from an all “1” state to an all “0” state.

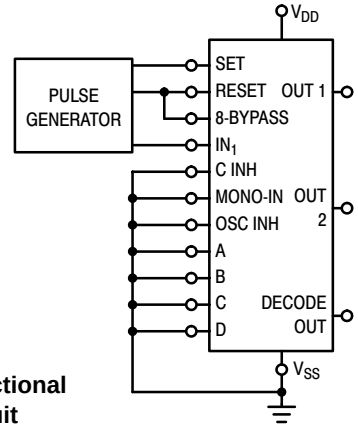


**Figure 9. Functional Test Circuit**

**FUNCTIONAL TEST SEQUENCE**

| Inputs | | | | Outputs | Comments |
|---|---|---|---|---|---|
| $In_1$ | Set | Reset | 8-Bypass | Decade Out Q1 thru Q24 | All 24 stages are in Reset mode. |
| 1 | 0 | 1 | 1 | 0 | |
| 1 | 1 | 1 | 1 | 0 | Counter is in three 8 stage sections in parallel mode. |
| 0 | 1 | 1 | 1 | 0 | First “1” to “0” transition of clock. |
| 1<br>0<br>–<br>–<br>– | 1 | 1 | 1 | | 255 “1” to “0” transitions are clocked in the counter. |
| 0 | 1 | 1 | 1 | 1 | The 255 “1” to “0” transition. |
| 0 | 0 | 0 | 0 | 1 | Counter converted back to 24 stages in series mode.<br>Set and Reset must be connected together and simultaneously go from “1” to “0”. |
| 1 | 0 | 0 | 0 | 1 | $In_1$ Switches to a “1”. |
| 0 | 0 | 0 | 0 | 0 | Counter Ripples from an all “1” state to an all “0” state. |



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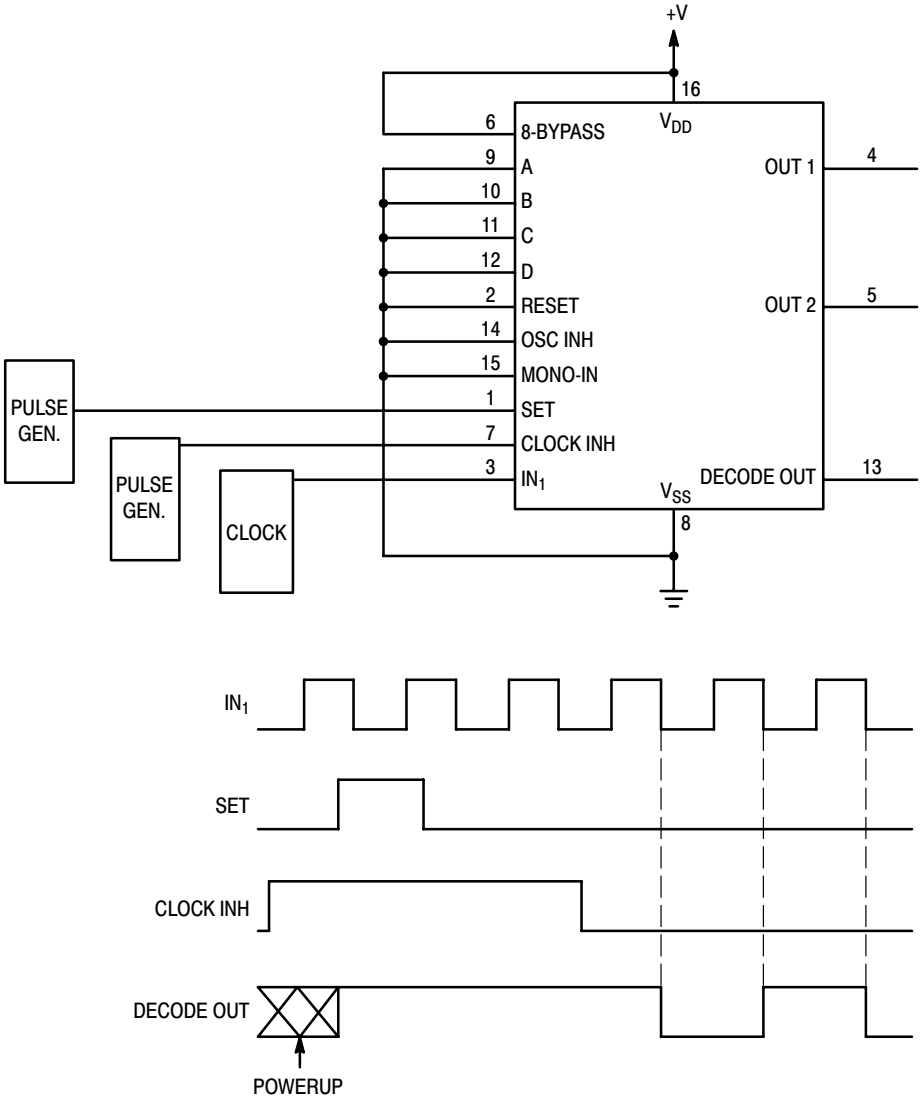


NOTE: When power is first applied to the device, DECODE OUT can be either at a high or low state. On the rising edge of a SET pulse the output goes high if initially at a low state. The output remains high if initially at a high state. Because CLOCK INH is held high, the clock source on the input pin has no effect on the output. Once CLOCK INH is taken low, the output goes low on the first negative clock transition. The output returns high depending on the 8-BYPASS, A, B, C, and D inputs, and the clock input period. A $2^n$ frequency division (where n = the number of stages selected from the truth table) is obtainable at DECODE OUT. A $2^0$–divided output of $IN_1$ can be obtained at $OUT_1$ and $OUT_2$.

**Figure 10. Time Interval Configuration Using an External Clock, Set, and Clock Inhibit Functions (Divide-by-2 Configured)**



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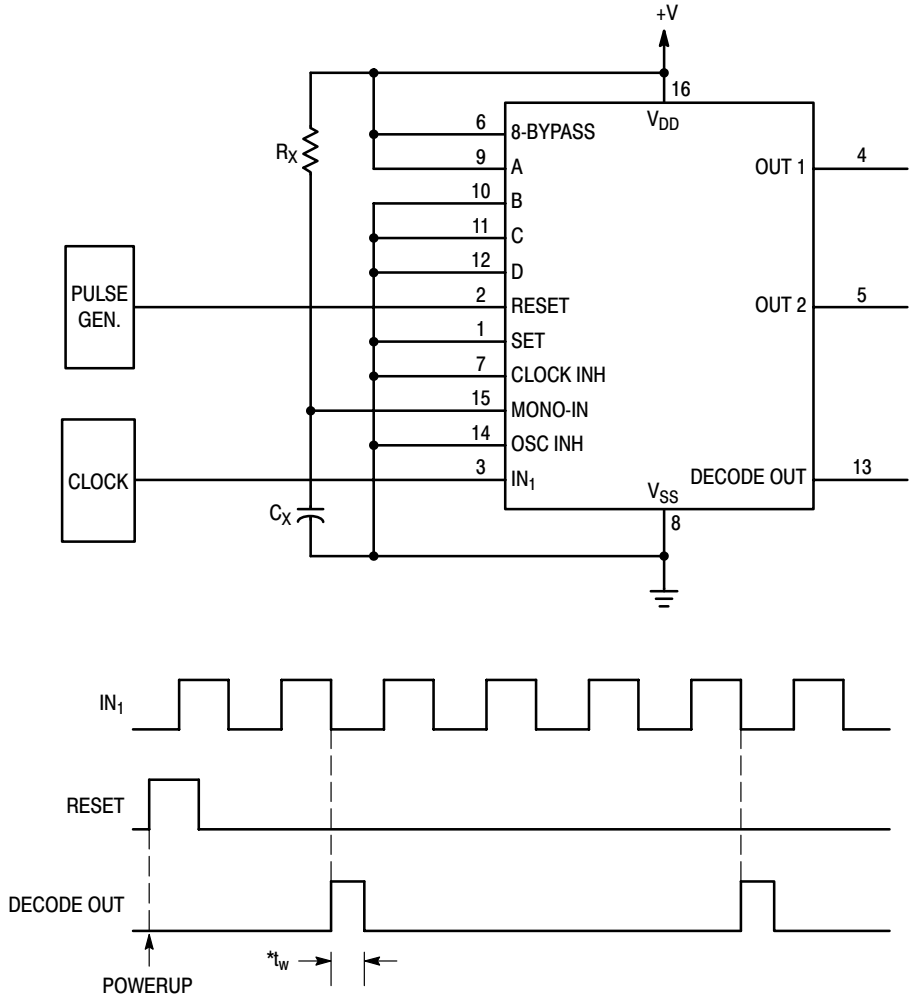


NOTE: When Power is first applied to the device with the RESET input going high, DECODE OUT initializes low. Bringing the RESET input low enables the chip's internal counters. After RESET goes low, the $2^n/2$ negative transition of the clock input causes DECODE OUT to go high. Since the MONO-IN input is being used, the output becomes monostable. The pulse width of the output is dependent on the external timing components. The second and all subsequent pulses occur at $2^n$ x (the clock period) intervals where n = the number of stages selected from the truth table.

**Figure 11. Time Interval Configuration Using an External Clock, Reset, and Output Monostable to Achieve a Pulse Output (Divide-by-4 Configured)**



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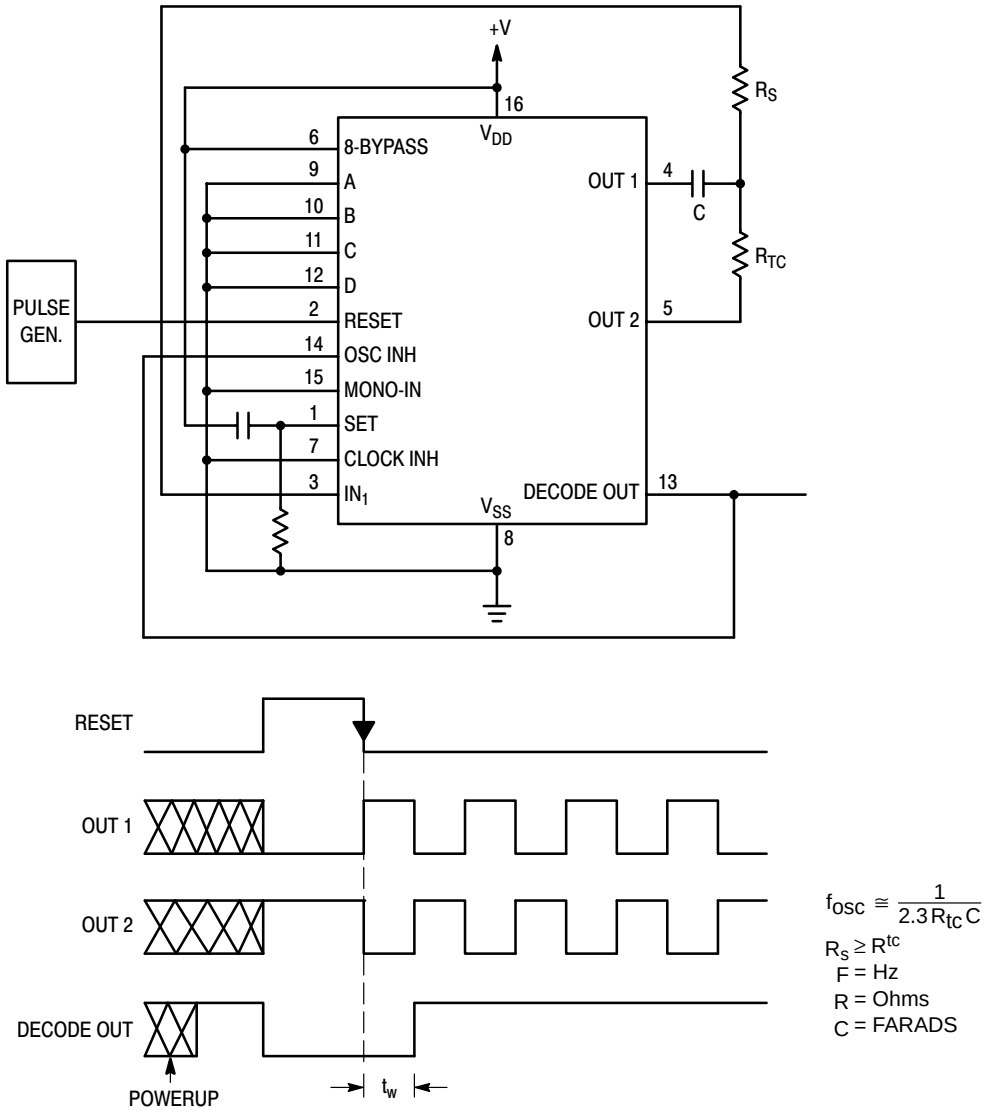


NOTE: This circuit is designed to use the on-chip oscillation function. The oscillator frequency is determined by the external R and C components. When power is first applied to the device, DECODE OUT initializes to a high state. Because this output is tied directly to the OSC INH input, the oscillator is disabled. This puts the device in a low-current standby condition. The rising edge of the RESET pulse will cause the output to go low. This in turn causes OSC INH to go low. However, while RESET is high, the oscillator is still disabled (i.e.: standby condition). After RESET goes low, the output remains low for $2^n/2$ of the oscillator's period. After the part times out, the output again goes high.

**Figure 12. Time Interval Configuration Using On-Chip RC Oscillator and Reset Input to Initiate Time Interval (Divide-by-2 Configured)**



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## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC14536BDWG | SOIC-16 WB<br>(Pb-Free) | 47 Units / Rail |
| MC14536BDWR2G | SOIC-16 WB<br>(Pb-Free) | 1000 / Tape & Reel |
| NLV14536BDWR2G* | SOIC-16 WB<br>(Pb-Free) | 1000 / Tape & Reel |
| NLV14536BDTR2G*<br>(In Development) | TSSOP-16<br>(Pb-Free) | 2500 / Tape & Reel |

**DISCONTINUED** (Note 7)

| | | |
|---|---|---|
| NLV14536BDWG* | SOIC-16 WB<br>(Pb-Free) | 47 Units / Rail |
| MC14536BFELG | SOEIAJ-16<br>(Pb-Free) | 2000 / Tape & Reel |

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

* NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

7. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.



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## REVISION HISTORY

| Revision | Description of Changes | Date |
|---|---|---|
| 15 | Rebranded the Data Sheet to **onsemi** format.<br>NLV14536BDWG, MC14536BFELG OPNs marked as Discontinued. | 10/3/2025 |

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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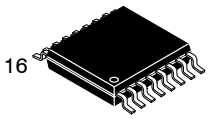
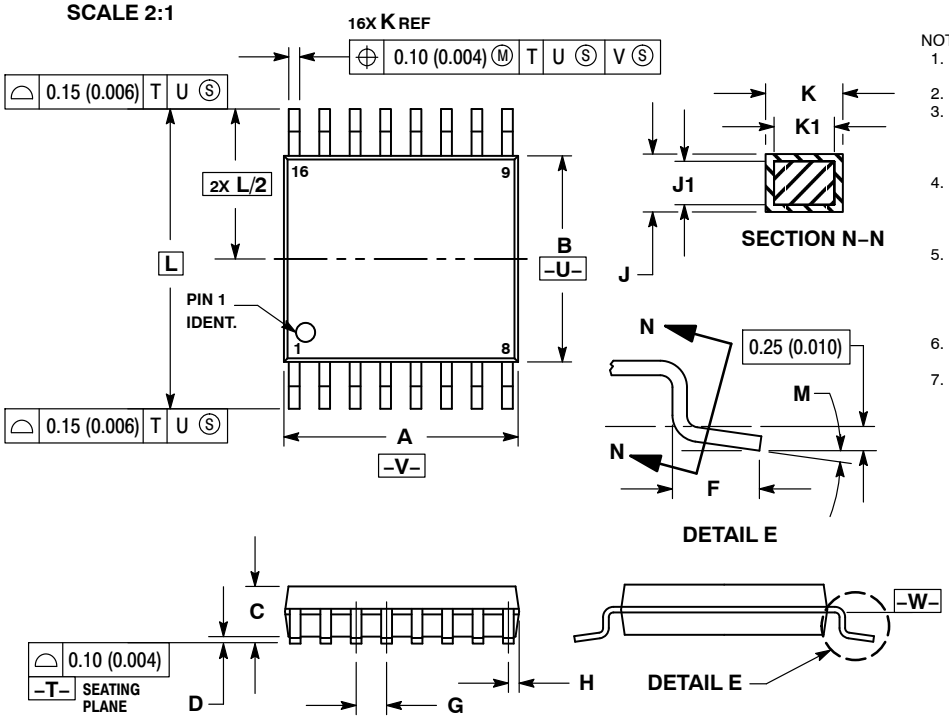



SCALE 2:1

**TSSOP−16 WB**
CASE 948F
ISSUE B

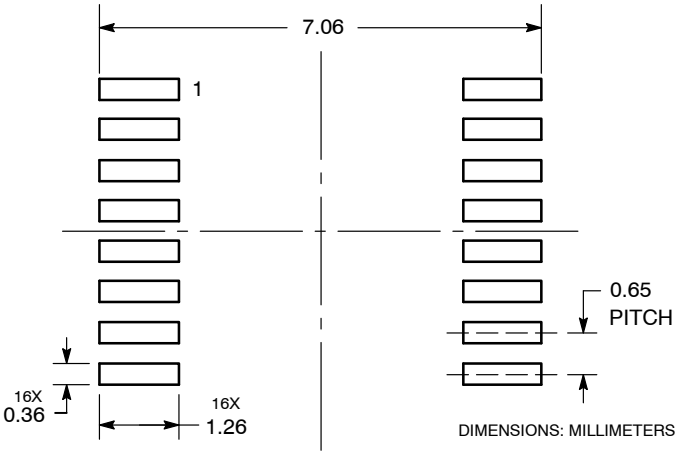
DATE 19 OCT 2006




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

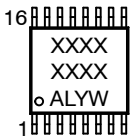
| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | −−− | 1.20 | −−− | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

## RECOMMENDED SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




| | |
|---|---|
| XXXX | = Specific Device Code |
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| W | = Work Week |
| G or ▪ | = Pb−Free Package |

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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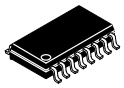
**SOEIAJ−16**
CASE 966−01
ISSUE A

DATE 27 OCT 2005



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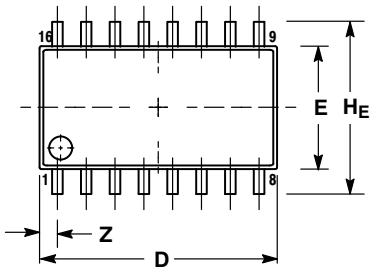
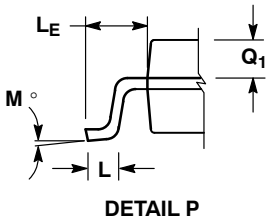
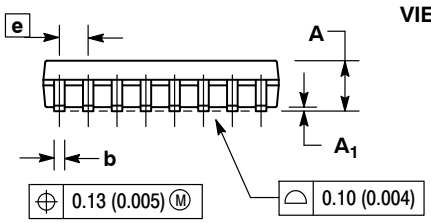
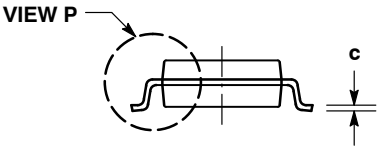



**DETAIL P**




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 ( 0.018).

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| $A_1$ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.10 | 0.20 | 0.007 | 0.011 |
| D | 9.90 | 10.50 | 0.390 | 0.413 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| $H_E$ | 7.40 | 8.20 | 0.291 | 0.323 |
| L | 0.50 | 0.85 | 0.020 | 0.033 |
| $L_E$ | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0 ° | 10 ° | 0 ° | 10 ° |
| $Q_1$ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 0.78 | --- | 0.031 |

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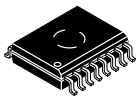
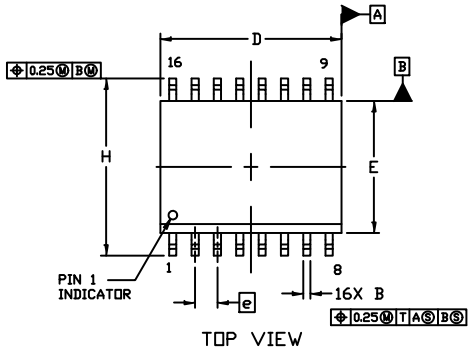


1

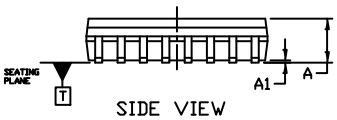
**SCALE 1:1**

**SOIC−16 WB**
CASE 751G
ISSUE E

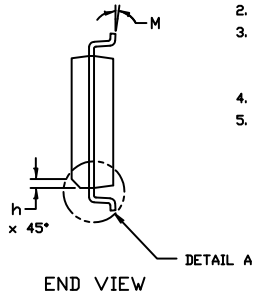
DATE 08 OCT 2021



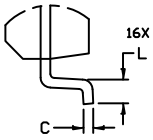

TOP VIEW




SIDE VIEW




END VIEW

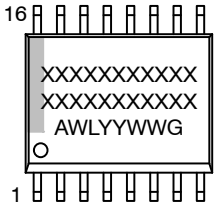



DETAIL A
2X SCALE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION OR FLASH TO BE 0.15 PER SIDE.

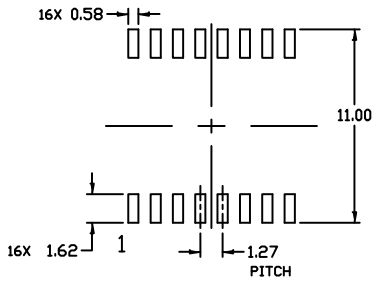
| | MILLIMETERS | |
|---|---|---|
| DIM | MIN. | MAX. |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 10.15 | 10.45 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.53 REF | |
| L | 0.50 | 0.90 |
| M | 0° | 7° |

## GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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