MC14503B

Hex Non-Inverting 3-State Buffer

The MC14503B is a hex non−inverting buffer with 3−state outputs, and a high current source and sink capability. The 3−state outputs make it useful in common bussing applications. Two disable controls are provided. A high level on the Disable A input causes the outputs of buffers 1 through 4 to go into a high impedance state and a high level on the Disable B input causes the outputs of buffers 5 and 6 to go into a high impedance state.

Features

- 3−State Outputs
- TTL Compatible − Will Drive One TTL Load Over Full Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Two Disable Controls for Added Versatility
- Pin for Pin Replacement for MM80C97 and 340097
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This Device is Pb−Free and is RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1)

Parameter	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	−0.5 to +18.0	V
Input or Output Voltage Range (DC or Transient)	V_{in}, V_{out}	−0.5 to V_{DD} + 0.5	V
Input Current (DC or Transient) per Pin	I_{in}	±10	mA
Output Current (DC or Transient) per Pin	I_{out}	±25	mA
Power Dissipation, per Package (Note 2)	P_D	500	mW
Ambient Temperature Range	T_A	−55 to +125	°C
Storage Temperature Range		−65 to +150	°C
Lead Temperature (8−Second Soldering)		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:
   "D/DW" Package: –7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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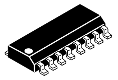

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SOIC−16
D SUFFIX
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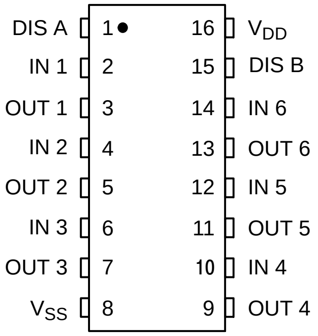
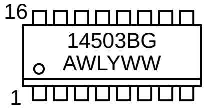
PIN ASSIGNMENT



MARKING DIAGRAM



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb−Free Package

TRUTH TABLE

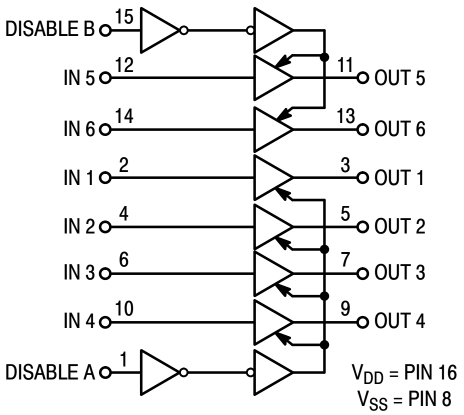
In_n	Appropriate Disable Input	Out_n
0	0	0
1	0	1
X	1	High Impedance

X = Don't Care

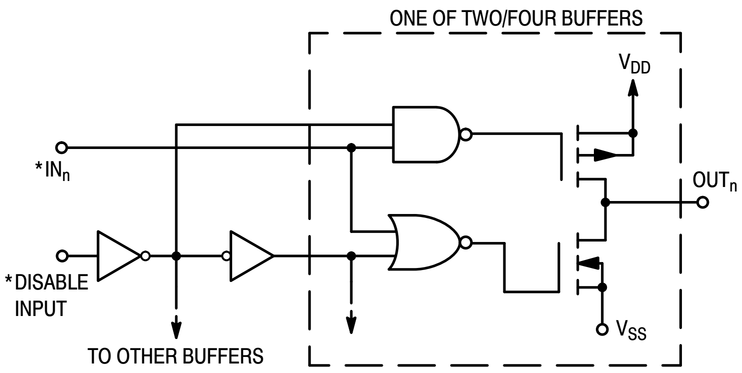
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

LOGIC DIAGRAM



CIRCUIT DIAGRAM



*Diode protection on all inputs (not shown)

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (Note 3)	Max	Min	Max	
Output Voltage "0" Level V_{in} = 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level V_{in} = V_{DD}	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 3.6 or 1.4 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 7.2 or 2.8 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 11.5 or 3.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 1.4 or 3.6 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 2.8 or 7.2 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 3.5 or 11.5 Vdc)		15	11	–	11	8.25	–	11	–	
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		4.5	–4.3	–	–3.6	–5.0	–	–2.5	–	
(V_{OH} = 2.5 Vdc)		5.0	–5.8	–	–4.8	–6.1	–	–3.0	–	
(V_{OH} = 4.6 Vdc)		5.0	–1.2	–	–1.02	–1.4	–	–0.7	–	
(V_{OH} = 9.5 Vdc)		10	–3.1	–	–2.6	–3.7	–	–1.8	–	
(V_{OH} = 13.5 Vdc)		15	–8.2	–	–6.8	–14.1	–	–4.8	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	4.5	2.2	–	1.8	2.1	–	1.2	–	mAdc
(V_{OL} = 0.4 Vdc)		5.0	2.6	–	2.1	2.3	–	1.3	–	
(V_{OL} = 0.5 Vdc)		10	6.5	–	5.5	6.2	–	3.8	–	
(V_{OL} = 1.5 Vdc)		15	19.2	–	16.1	25	–	11.2	–	
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Capacitance, (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current, (Per Package)	I_Q	5.0	–	1.0	–	0.002	1.0	–	30	µAdc
		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Total Supply Current (Note 4, 5)	I_T									µAdc
(Dynamic plus Quiescent,		5.0	I_T = (2.5 µA/kHz) f + I_{DD}							
Per Package)										
(C_L = 50 pF on all outputs)		10	I_T = (6.0 µA/kHz) f + I_{DD}							
(All outputs switching,		15	I_T = (10 µA/kHz) f + I_{DD}							
50% Duty Cycle)										
3−State Output Leakage Current	I_{TL}	15	–	±0.1	–	±0.0001	±0.1	–	±3.0	µAdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
4. The formulas given are for the typical characteristics only at 25°C.
5. To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50\ pF) + (C_L – 50)$ Vfk where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.006.

SWITCHING CHARACTERISTICS (Note 6) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} V_{CC}	All Types Typ (Note 7)	 Max	Unit
Output Rise Time	t_{TLH}				ns
t_{TLH} = (0.5 ns/pF) C_L + 20 ns		5.0	45	90	
t_{TLH} = (0.3 ns/pF) C_L + 8.0 ns		10	23	45	
t_{TLH} = (0.2 ns/pF) C_L + 8.0 ns		15	18	35	
Output Fall Time	t_{THL}				ns
t_{THL} = (0.5 ns/pF) C_L + 20 ns		5.0	45	90	
t_{THL} = (0.3 ns/pF) C_L + 8.0 ns		10	23	45	
t_{THL} = (0.2 ns/pF) C_L + 8.0 ns		15	18	35	
Turn−Off Delay Time, all Outputs	t_{PLH}				ns
t_{PLH} = (0.3 ns/pF) C_L + 60 ns		5.0	75	150	
t_{PLH} = (0.15 ns/pF) C_L + 27 ns		10	35	70	
t_{PLH} = (0.1 ns/pF) C_L + 20 ns		15	25	50	
Turn−On Delay Time, all Outputs	t_{PHL}				ns
t_{PHL} = (0.3 ns/pF) C_L + 60 ns		5.0	75	150	
t_{PHL} = (0.15 ns/pF) C_L + 27 ns		10	35	70	
t_{PHL} = (0.1 ns/pF) C_L + 20 ns		15	25	50	
3−State Propagation Delay Time	t_{PHZ}	5.0	75	150	ns
Output “1” to High Impedance		10	40	80	
		15	35	70	
Output “0” to High Impedance	t_{PLZ}	5.0	80	160	ns
		10	40	80	
		15	35	70	
High Impedance to “1” Level	t_{PZH}	5.0	65	130	ns
		10	25	50	
		15	20	40	
High Impedance to “0” Level	t_{PZL}	5.0	100	200	ns
		10	35	70	
		15	25	50	

6. The formulas given are for the typical characteristics only at 25°C.
7. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

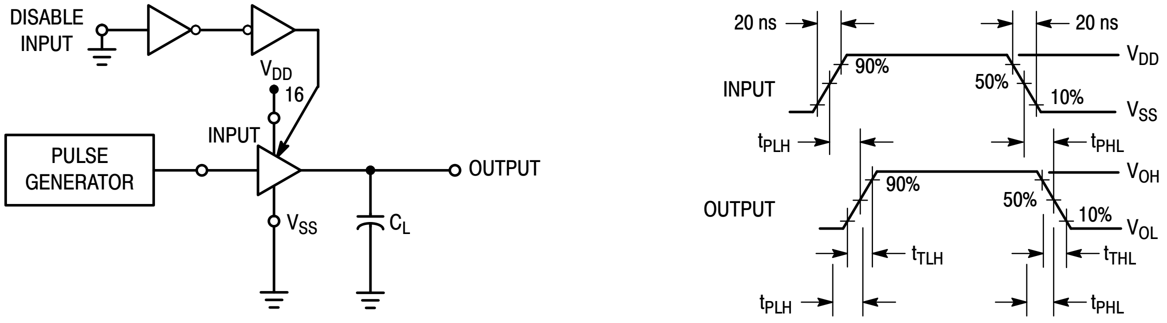


Figure 1. Switching Time Test Circuit and Waveforms
(t_{TLH}, t_{THL}, t_{PHL}, and t_{PLH})

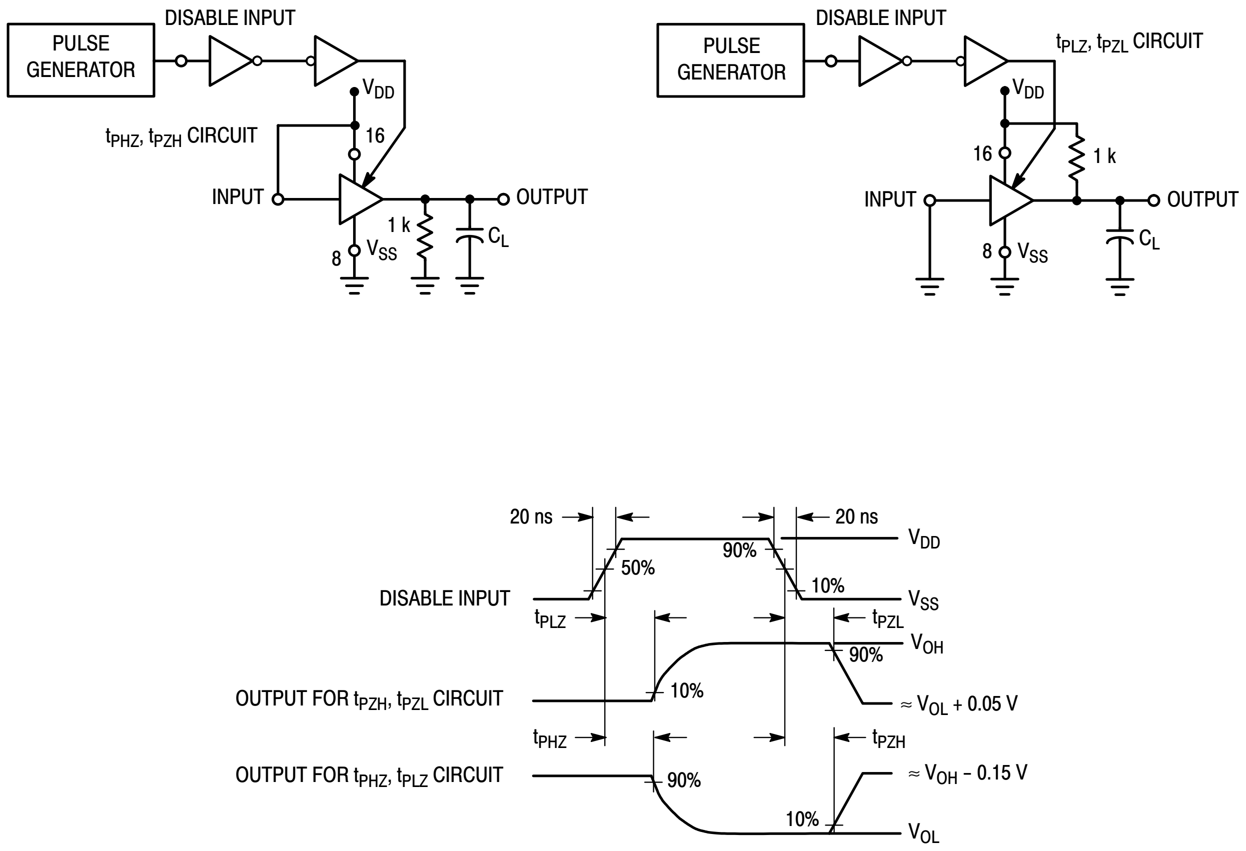


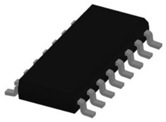
Figure 2. 3−State AC Test Circuit and Waveforms (t_{PLZ}, t_{PHZ}, t_{PZH}, t_{PZL})

ORDERING INFORMATION

Device	Package	Shipping†
MC14503BDG	SOIC−16 (Pb−Free)	48 / Rail
MC14503BDR2G	SOIC−16 (Pb−Free)	2500 / Tape & Reel
NLV14503BDR2G*	SOIC−16 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.



SOIC-16 9.90x3.90x1.37 1.27P
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ISSUE M

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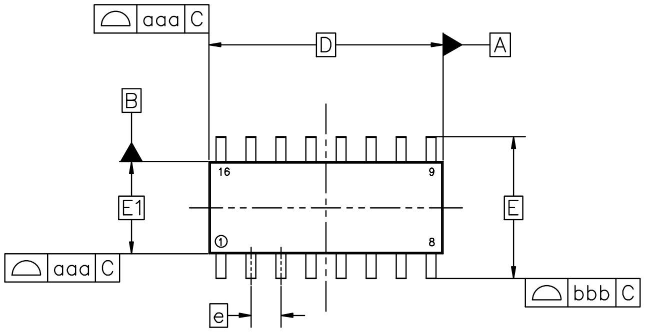
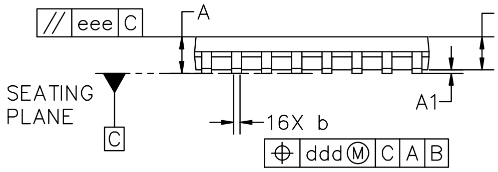
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.

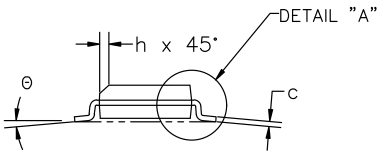
	MILLIMETERS		
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	---	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
Θ	0°	---	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



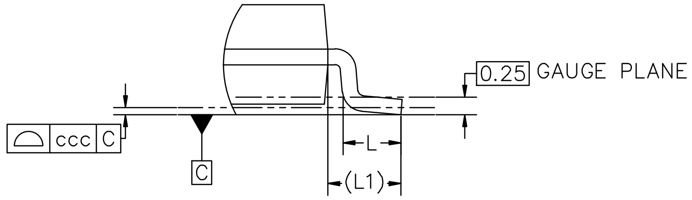
TOP VIEW



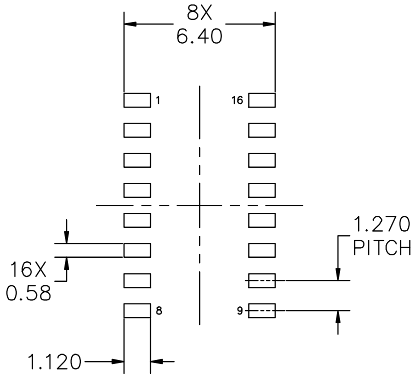
SIDE VIEW



END VIEW



DETAIL "A"
Scale 3:1



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

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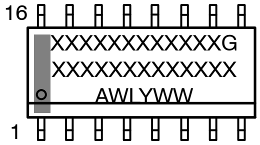
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

PIN	STYLE 1:	STYLE 2:	STYLE 3:	STYLE 4:
PIN 1.	COLLECTOR	CATHODE	COLLECTOR, DYE #1	COLLECTOR, DYE #1
2.	BASE	ANODE	BASE, #1	COLLECTOR, #1
3.	EMITTER	NO CONNECTION	EMITTER, #1	COLLECTOR, #2
4.	NO CONNECTION	CATHODE	COLLECTOR, #1	COLLECTOR, #2
5.	EMITTER	CATHODE	COLLECTOR, #2	COLLECTOR, #3
6.	BASE	NO CONNECTION	BASE, #2	COLLECTOR, #3
7.	COLLECTOR	ANODE	EMITTER, #2	COLLECTOR, #4
8.	COLLECTOR	CATHODE	COLLECTOR, #2	COLLECTOR, #4
9.	BASE	CATHODE	COLLECTOR, #3	BASE, #4
10.	EMITTER	ANODE	BASE, #3	EMITTER, #4
11.	NO CONNECTION	NO CONNECTION	EMITTER, #3	BASE, #3
12.	EMITTER	CATHODE	COLLECTOR, #3	EMITTER, #3
13.	BASE	CATHODE	COLLECTOR, #4	BASE, #2
14.	COLLECTOR	NO CONNECTION	BASE, #4	EMITTER, #2
15.	EMITTER	ANODE	EMITTER, #4	BASE, #1
16.	COLLECTOR	CATHODE	COLLECTOR, #4	EMITTER, #1

PIN	STYLE 5:	STYLE 6:	STYLE 7:
PIN 1.	DRAIN, DYE #1	CATHODE	SOURCE N-CH
2.	DRAIN, #1	CATHODE	COMMON DRAIN (OUTPUT)
3.	DRAIN, #2	CATHODE	COMMON DRAIN (OUTPUT)
4.	DRAIN, #2	CATHODE	GATE P-CH
5.	DRAIN, #3	CATHODE	COMMON DRAIN (OUTPUT)
6.	DRAIN, #3	CATHODE	COMMON DRAIN (OUTPUT)
7.	DRAIN, #4	CATHODE	COMMON DRAIN (OUTPUT)
8.	DRAIN, #4	CATHODE	SOURCE P-CH
9.	GATE, #4	ANODE	SOURCE P-CH
10.	SOURCE, #4	ANODE	COMMON DRAIN (OUTPUT)
11.	GATE, #3	ANODE	COMMON DRAIN (OUTPUT)
12.	SOURCE, #3	ANODE	COMMON DRAIN (OUTPUT)
13.	GATE, #2	ANODE	GATE N-CH
14.	SOURCE, #2	ANODE	COMMON DRAIN (OUTPUT)
15.	GATE, #1	ANODE	COMMON DRAIN (OUTPUT)
16.	SOURCE, #1	ANODE	SOURCE N-CH

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