

CMOS SSI

Quad Exclusive "OR" and "NOR" Gates

MC14070B, MC14077B

The MC14070B quad exclusive OR gate and the MC14077B quad exclusive NOR gate are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

Features

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- MC14070B – Replacement for CD4030B and CD4070B Types
- MC14077B – Replacement for CD4077B Type
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

| Symbol | Parameter | Value | Unit |
|------------------------------------|---|-------------------------------|------|
| V _{DD} | DC Supply Voltage Range | -0.5 to +18.0 | V |
| V _{in} , V _{out} | Input or Output Voltage Range (DC or Transient) | -0.5 to V _{DD} + 0.5 | V |
| I _{in} , I _{out} | Input or Output Current (DC or Transient) per Pin | ±10 | mA |
| P _D | Power Dissipation, per Package (Note 1) | 500 | mW |
| T _A | Ambient Temperature Range | -55 to +125 | °C |
| T _{stg} | Storage Temperature Range | -65 to +150 | °C |
| T _L | Lead Temperature (8-Second Soldering) | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Packages: -7.0 mW/°C From 65 °C To 125 °C

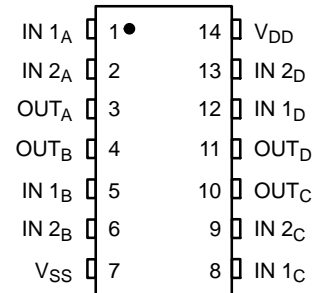
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

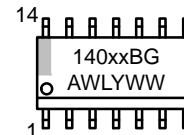


SOIC-14
D SUFFIX
CASE 751A

PIN ASSIGNMENT



MARKING DIAGRAM



- xx = Specific Device Code
- A = Assembly Location
- WL, L = Wafer Lot
- YY, Y = Year
- WW, W = Work Week
- G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MC14070B, MC14077B

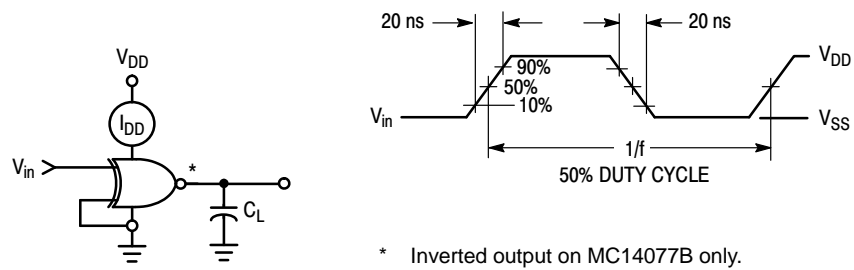
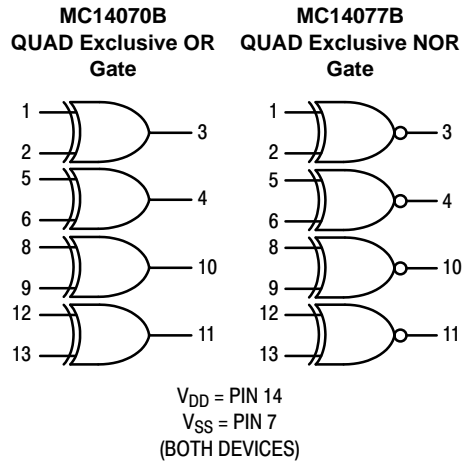


Figure 1. Power Dissipation Test Circuit and Waveform

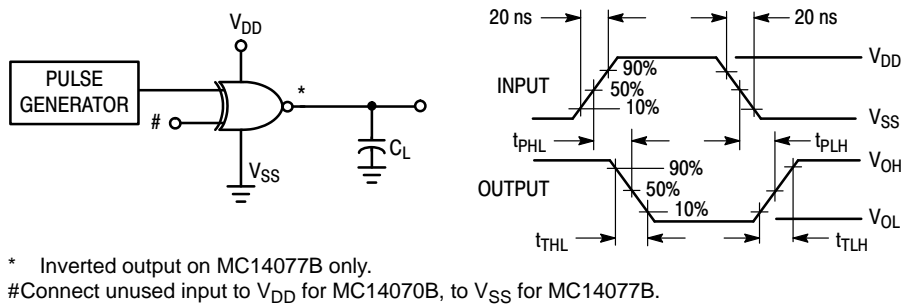


Figure 2. Switching Time Test Circuit and Waveforms

MC14070B, MC14077B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

| Characteristic | Symbol | V _{DD} Vdc | -55 °C | | 25 °C | | | 125 °C | | Unit | |
|--|--|------------------------|---|-------|-------|-----------------|-------|--------|-------|------|------|
| | | | Min | Max | Min | Typ (Note 2) | Max | Min | Max | | |
| Output Voltage V _{in} = V _{DD} or 0 | "0" Level | V _{OL} | 5.0 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | Vdc |
| | | | 10 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | |
| | | | 15 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | |
| | "1" Level | V _{OH} | 5.0 | 4.95 | – | 4.95 | 5.0 | – | 4.95 | – | Vdc |
| | | | 10 | 9.95 | – | 9.95 | 10 | – | 9.95 | – | |
| | | | 15 | 14.95 | – | 14.95 | 15 | – | 14.95 | – | |
| Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) | "0" Level | V _{IL} | 5.0 | – | 1.5 | – | 2.25 | 1.5 | – | 1.5 | Vdc |
| | | | 10 | – | 3.0 | – | 4.50 | 3.0 | – | 3.0 | |
| | | | 15 | – | 4.0 | – | 6.75 | 4.0 | – | 4.0 | |
| | "1" Level | V _{IH} | 5.0 | 3.5 | – | 3.5 | 2.75 | – | 3.5 | – | Vdc |
| | | | 10 | 7.0 | – | 7.0 | 5.50 | – | 7.0 | – | |
| | | | 15 | 11 | – | 11 | 8.25 | – | 11 | – | |
| Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) | Source | I _{OH} | 5.0 | –3.0 | – | –2.4 | –4.2 | – | –1.7 | – | mAdc |
| | | | 5.0 | –0.64 | – | –0.51 | –0.88 | – | –0.36 | – | |
| | | | 10 | –1.6 | – | –1.3 | –2.25 | – | –0.9 | – | |
| | Sink | I _{OL} | 5.0 | 0.64 | – | 0.51 | 0.88 | – | 0.36 | – | mAdc |
| | | | 10 | 1.6 | – | 1.3 | 2.25 | – | 0.9 | – | |
| | | | 15 | 4.2 | – | 3.4 | 8.8 | – | 2.4 | – | |
| Input Current | I _{in} | 15 | – | ±0.1 | – | ±0.00001 | ±0.1 | – | ±1.0 | μAdc | |
| Input Capacitance (V _{in} = 0) | C _{in} | – | – | – | – | 5.0 | 7.5 | – | – | pF | |
| Quiescent Current (Per Package) | I _{DD} | 5.0 | – | 0.25 | – | 0.0005 | 0.25 | – | 7.5 | μAdc | |
| | | 10 | – | 0.5 | – | 0.0010 | 0.5 | – | 15 | | |
| | | 15 | – | 1.0 | – | 0.0015 | 1.0 | – | 30 | | |
| Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching) | I _T | 5.0 | I _T = (0.3 μA/kHz) f + I _{DD} | | | | | | | μAdc | |
| | | 10 | I _T = (0.6 μA/kHz) f + I _{DD} | | | | | | | | |
| | | 15 | I _T = (0.9 μA/kHz) f + I _{DD} | | | | | | | | |
| Output Rise and Fall Times (Note 3) (C _L = 50 pF) t _{TLH} , t _{THL} = (1.35 ns/pF) C _L + 33 ns t _{TLH} , t _{THL} = (0.60 ns/pF) C _L + 20 ns t _{TLH} , t _{THL} = (0.40 ns/pF) C _L + 20 ns | t _{TLH} , t _{THL} | 5.0 | – | – | – | 100 | 200 | – | – | ns | |
| | | 10 | – | – | – | 50 | 100 | – | – | | |
| | | 15 | – | – | – | 40 | 80 | – | – | | |
| | | – | – | – | – | – | – | – | – | | |
| Propagation Delay Times (Note 3) (C _L = 50 pF) t _{PLH} , t _{PHL} = (0.90 ns/pF) C _L + 130 ns t _{PLH} , t _{PHL} = (0.36 ns/pF) C _L + 57 ns t _{PLH} , t _{PHL} = (0.26 ns/pF) C _L + 37 ns | t _{PLH} , t _{PHL} | 5.0 | – | – | – | 175 | 350 | – | – | ns | |
| | | 10 | – | – | – | 75 | 150 | – | – | | |
| | | 15 | – | – | – | 55 | 110 | – | – | | |
| | | – | – | – | – | – | – | – | – | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25 °C.

4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V f k$$

where: I_T is in μH (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

MC14070B, MC14077B

ORDERING INFORMATION

| Device | Package | Shipping† |
|----------------|----------------------|--------------------|
| MC14070BDG | SOIC-14 (Pb-Free) | 55 Units / Rail |
| MC14070BDR2G | SOIC-14 (Pb-Free) | 2500 / Tape & Reel |
| NLV14070BDR2G* | SOIC-14 (Pb-Free) | 2500 / Tape & Reel |

| | | |
|----------------|----------------------|--------------------|
| MC14077BDG | SOIC-14 (Pb-Free) | 55 Units / Rail |
| MC14077BDR2G | SOIC-14 (Pb-Free) | 2500 / Tape & Reel |
| NLV14077BDR2G* | SOIC-14 (Pb-Free) | 2500 / Tape & Reel |

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

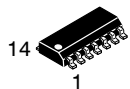
* NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

MC14070B, MC14077B

REVISION HISTORY

| Revision | Description of Changes | Date |
|----------|---|-----------|
| 11 | Rebranded the Data Sheet to onsemi format. | 8/26/2025 |

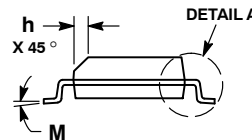
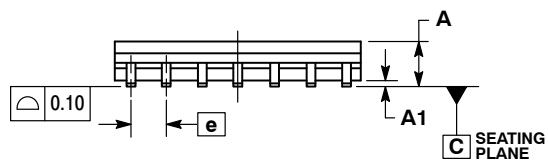
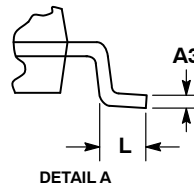
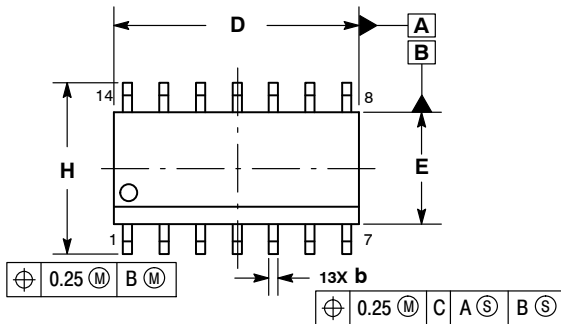
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



SCALE 1:1

SOIC-14 NB
CASE 751A-03
ISSUE L

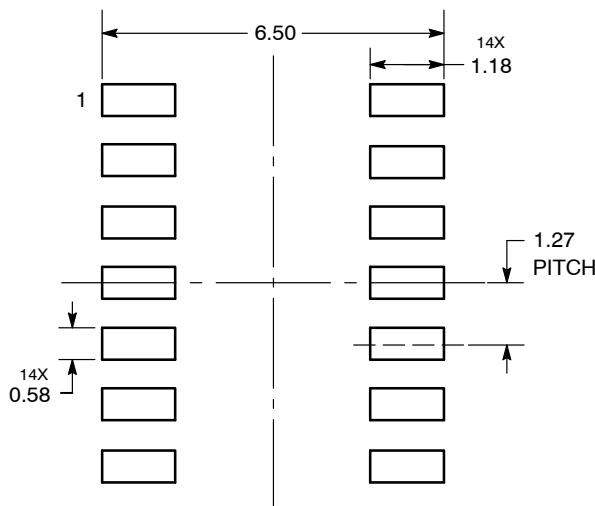
DATE 03 FEB 2016



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
 5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.054 | 0.068 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A3 | 0.19 | 0.25 | 0.008 | 0.010 |
| b | 0.35 | 0.49 | 0.014 | 0.019 |
| D | 8.55 | 8.75 | 0.337 | 0.344 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.019 |
| L | 0.40 | 1.25 | 0.016 | 0.049 |
| M | 0° | 7° | 0° | 7° |

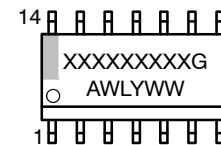
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

| | | |
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ISSUE L

DATE 03 FEB 2016

STYLE 1:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. NO CONNECTION
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 2:
 CANCELLED

STYLE 3:
 PIN 1. NO CONNECTION
 2. ANODE
 3. ANODE
 4. NO CONNECTION
 5. ANODE
 6. NO CONNECTION
 7. ANODE
 8. ANODE
 9. ANODE
 10. NO CONNECTION
 11. ANODE
 12. ANODE
 13. NO CONNECTION
 14. COMMON CATHODE

STYLE 4:
 PIN 1. NO CONNECTION
 2. CATHODE
 3. CATHODE
 4. NO CONNECTION
 5. CATHODE
 6. NO CONNECTION
 7. CATHODE
 8. CATHODE
 9. CATHODE
 10. NO CONNECTION
 11. CATHODE
 12. CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 5:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. COMMON ANODE
 8. COMMON CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 6:
 PIN 1. CATHODE
 2. CATHODE
 3. CATHODE
 4. CATHODE
 5. CATHODE
 6. CATHODE
 7. CATHODE
 8. ANODE
 9. ANODE
 10. ANODE
 11. ANODE
 12. ANODE
 13. ANODE
 14. ANODE

STYLE 7:
 PIN 1. ANODE/CATHODE
 2. COMMON ANODE
 3. COMMON CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. COMMON CATHODE
 12. COMMON ANODE
 13. ANODE/CATHODE
 14. ANODE/CATHODE

STYLE 8:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. COMMON ANODE
 8. COMMON ANODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. NO CONNECTION
 12. ANODE/CATHODE
 13. ANODE/CATHODE
 14. COMMON CATHODE

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