5 V ECL ÷4 Divider

MC10EL33, MC100EL33

Description
The MC10EL/100EL33 is an integrated ÷4 divider. The differential clock inputs and the V_{BB} allow a differential, single-ended or AC coupled interface to the device. The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flops will attain a random state; the reset allows for the synchronization of multiple EL33’s in a system.

The 100 Series contains temperature compensation.

Features
• 650 ps Propagation Delay
• 4.0 GHz Toggle Frequency
• ESD Protection:
  ♦ > 1 kV Human Body Model
  ♦ > 100 V Machine Model
• PECL Mode Operating Range: V_{CC} = 4.2 V to 5.7 V with V_{EE} = 0 V
• NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = −4.2 V to −5.7 V
• Internal Input Pulldown Resistors on CLK(s) and R.
• Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
• Moisture Sensitivity:
  ♦ Level 1 for SOIC–8 NB
  ♦ For Additional Information, see Application Note AND8003/D
• Flammability Rating: UL 94 V–0 @ 0.125 in,
  Oxygen Index: 28 to 34
• Transistor Count = 95 Devices
• These Devices are Pb-Free, Halogen Free and are RoHS Compliant

MARKING DIAGRAM

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package</th>
<th>Shipping</th>
</tr>
</thead>
<tbody>
<tr>
<td>MC10EL33DG</td>
<td>SOIC–8 (Pb-Free)</td>
<td>98 Units / Tube</td>
</tr>
<tr>
<td>MC100EL33DG</td>
<td>SOIC–8 (Pb-Free)</td>
<td>98 Units / Tube</td>
</tr>
</tbody>
</table>

(Note: Microdot may be in either location)
"For additional marking information, refer to Application Note AND8002/D."
MC10EL33, MC100EL33

Figure 1. Logic Diagram and Pinout Assignment

Table 1. PIN DESCRIPTION

<table>
<thead>
<tr>
<th>Pin</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK, CLK</td>
<td>ECL Clock Inputs*</td>
</tr>
<tr>
<td>Reset</td>
<td>ECL Asynch Reset*</td>
</tr>
<tr>
<td>Q, Q</td>
<td>ECL Data Outputs</td>
</tr>
<tr>
<td>VBB</td>
<td>Reference Voltage Output</td>
</tr>
<tr>
<td>VCC</td>
<td>Positive Supply</td>
</tr>
<tr>
<td>VEE</td>
<td>Negative Supply</td>
</tr>
</tbody>
</table>

*Pins will default low when left open.

Table 2. MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition 1</th>
<th>Condition 2</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>PECL Mode Power Supply</td>
<td>VEE = 0 V</td>
<td></td>
<td>8</td>
<td>V</td>
</tr>
<tr>
<td>VEE</td>
<td>NECL Mode Power Supply</td>
<td>VCC = 0 V</td>
<td></td>
<td>−8</td>
<td>V</td>
</tr>
<tr>
<td>VI</td>
<td>PECL Mode Input Voltage</td>
<td>VEE = 0 V</td>
<td>VCC = 0 V</td>
<td>V ≤ VCC</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>NECL Mode Input Voltage</td>
<td></td>
<td>V ≥ VEE</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>Iout</td>
<td>Output Current</td>
<td>Continuous</td>
<td>Surge</td>
<td>50</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>IBB</td>
<td>VBB Sink/Source</td>
<td></td>
<td></td>
<td>±0.5</td>
<td>mA</td>
</tr>
<tr>
<td>TA</td>
<td>Operating Temperature Range</td>
<td></td>
<td>−40 to +85</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Tstg</td>
<td>Storage Temperature Range</td>
<td></td>
<td>−65 to +150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>θJA</td>
<td>Thermal Resistance (Junction-to-Ambient)</td>
<td>0 lfpm</td>
<td>SOIC–8 NB</td>
<td>190</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500 lfpm</td>
<td>SOIC–8 NB</td>
<td>130</td>
<td>°C/W</td>
</tr>
<tr>
<td>θJC</td>
<td>Thermal Resistance (Junction-to-Case)</td>
<td>Standard Board</td>
<td>SOIC–8 NB</td>
<td>41 to 44</td>
<td>°C/W</td>
</tr>
<tr>
<td>Tsol</td>
<td>Wave Solder (Pb-Free)</td>
<td>&lt; 2 to 3 sec @ 260°C</td>
<td></td>
<td>265</td>
<td>°C</td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
### Table 3. 10EL SERIES PECL DC CHARACTERISTICS ($V_{CC} = 5.0$ V, $V_{EE} = 0.0$ V (Note 1))

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>$-40^\circ$C</th>
<th></th>
<th>$25^\circ$C</th>
<th></th>
<th>$85^\circ$C</th>
<th></th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Min</td>
<td>Typ</td>
</tr>
<tr>
<td>$I_{EE}$</td>
<td>Power Supply Current</td>
<td>27</td>
<td>33</td>
<td>27</td>
<td>33</td>
<td>27</td>
<td>33</td>
<td>27</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Output HIGH Voltage (Note 2)</td>
<td>3920</td>
<td>4010</td>
<td>4110</td>
<td>4020</td>
<td>4105</td>
<td>4190</td>
<td>4090</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output LOW Voltage (Note 2)</td>
<td>3050</td>
<td>3200</td>
<td>3350</td>
<td>3050</td>
<td>3210</td>
<td>3370</td>
<td>3050</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Input HIGH Voltage (Single-Ended)</td>
<td>3770</td>
<td>4110</td>
<td>3870</td>
<td>4190</td>
<td>3940</td>
<td>4280</td>
<td>3940</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input LOW Voltage (Single-Ended)</td>
<td>3050</td>
<td>3500</td>
<td>3050</td>
<td>3520</td>
<td>3050</td>
<td>3555</td>
<td>3050</td>
</tr>
<tr>
<td>$V_{BB}$</td>
<td>Output Voltage Reference</td>
<td>3.57</td>
<td>3.7</td>
<td>3.65</td>
<td>3.7</td>
<td>3.69</td>
<td>3.81</td>
<td></td>
</tr>
<tr>
<td>$V_{IHCMR}$</td>
<td>Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)</td>
<td>2.5</td>
<td>4.6</td>
<td>2.5</td>
<td>4.6</td>
<td>2.5</td>
<td>4.6</td>
<td></td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>Input HIGH Current</td>
<td>0.5</td>
<td>150</td>
<td>0.5</td>
<td>150</td>
<td>0.3</td>
<td>150</td>
<td></td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input LOW Current</td>
<td>0.5</td>
<td>150</td>
<td>0.5</td>
<td>150</td>
<td>0.3</td>
<td>150</td>
<td></td>
</tr>
</tbody>
</table>

**NOTE:** Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpfm.

1. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.25 V / −0.5 V.
2. Outputs are terminated through a 50 $\Omega$ resistor to $V_{CC} − 2.0$ V.
3. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between $V_{PP\text{min}}$ and 1 V.

### Table 4. 10EL SERIES NECL DC CHARACTERISTICS ($V_{CC} = 0.0$ V, $V_{EE} = −5.0$ V (Note 1))

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>$-40^\circ$C</th>
<th></th>
<th>$25^\circ$C</th>
<th></th>
<th>$85^\circ$C</th>
<th></th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Min</td>
<td>Typ</td>
</tr>
<tr>
<td>$I_{EE}$</td>
<td>Power Supply Current</td>
<td>27</td>
<td>33</td>
<td>27</td>
<td>33</td>
<td>27</td>
<td>33</td>
<td>27</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Output HIGH Voltage (Note 2)</td>
<td>−1080</td>
<td>−990</td>
<td>−890</td>
<td>−890</td>
<td>−895</td>
<td>−810</td>
<td>−810</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output LOW Voltage (Note 2)</td>
<td>−1950</td>
<td>−1800</td>
<td>−1650</td>
<td>−1650</td>
<td>−1790</td>
<td>−1630</td>
<td>−1950</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Input HIGH Voltage (Single-Ended)</td>
<td>−1230</td>
<td>−890</td>
<td>−1130</td>
<td>−810</td>
<td>−1060</td>
<td>−720</td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input LOW Voltage (Single-Ended)</td>
<td>−1950</td>
<td>−1500</td>
<td>−1950</td>
<td>−1480</td>
<td>−1950</td>
<td>−1445</td>
<td></td>
</tr>
<tr>
<td>$V_{BB}$</td>
<td>Output Voltage Reference</td>
<td>−1.43</td>
<td>−1.30</td>
<td>−1.35</td>
<td>−1.25</td>
<td>−1.31</td>
<td>−1.19</td>
<td></td>
</tr>
<tr>
<td>$V_{IHCMR}$</td>
<td>Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)</td>
<td>−2.5</td>
<td>−0.4</td>
<td>−2.5</td>
<td>−0.4</td>
<td>−2.5</td>
<td>−0.4</td>
<td></td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>Input HIGH Current</td>
<td>0.5</td>
<td>150</td>
<td>0.5</td>
<td>150</td>
<td>0.3</td>
<td>150</td>
<td></td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input LOW Current</td>
<td>0.5</td>
<td>150</td>
<td>0.5</td>
<td>150</td>
<td>0.3</td>
<td>150</td>
<td></td>
</tr>
</tbody>
</table>

**NOTE:** Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpfm.

1. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.25 V / −0.5 V.
2. Outputs are terminated through a 50 $\Omega$ resistor to $V_{CC} − 2.0$ V.
3. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between $V_{PP\text{min}}$ and 1 V.
### Table 5. 100EL SERIES PECL DC CHARACTERISTICS \((V_{CC} = 5.0 \text{ V}; V_{EE} = 0.0 \text{ V (Note 1)})\)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>−40°C</th>
<th>25°C</th>
<th>85°C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>IEE</td>
<td>27</td>
<td>33</td>
<td></td>
<td>27</td>
</tr>
<tr>
<td>VOH</td>
<td>3915</td>
<td>3995</td>
<td>4120</td>
<td>3975</td>
</tr>
<tr>
<td>VOL</td>
<td>3170</td>
<td>3305</td>
<td>3445</td>
<td>3190</td>
</tr>
<tr>
<td>VIH</td>
<td>3835</td>
<td>4120</td>
<td></td>
<td>3835</td>
</tr>
<tr>
<td>VIIL</td>
<td>3190</td>
<td>3525</td>
<td></td>
<td>3190</td>
</tr>
<tr>
<td>VBB</td>
<td>3.62</td>
<td>3.74</td>
<td></td>
<td>3.62</td>
</tr>
<tr>
<td>VIHCMR</td>
<td>2.5</td>
<td>4.6</td>
<td></td>
<td>2.5</td>
</tr>
<tr>
<td>IIH</td>
<td>150</td>
<td>150</td>
<td></td>
<td>150</td>
</tr>
<tr>
<td>IIL</td>
<td>0.5</td>
<td>0.5</td>
<td></td>
<td>0.5</td>
</tr>
</tbody>
</table>

**NOTE:** Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

1. Input and output parameters vary 1:1 with \(V_{CC}\). \(V_{EE}\) can vary +0.8 V / −0.5 V.
2. Outputs are terminated through a 50 Ω resistor to \(V_{CC} − 2.0 \text{ V}\).
3. \(V_{IHCMR}\) min varies 1:1 with \(V_{EE}\), \(V_{IHCMR}\) max varies 1:1 with \(V_{CC}\). The \(V_{IHCMR}\) range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between \(V_{PP\text{min}}\) and 1 V.

### Table 6. 100EL SERIES NECL DC CHARACTERISTICS \((V_{CC} = 0.0 \text{ V}; V_{EE} = −5.0 \text{ V (Note 1)})\)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>−40°C</th>
<th>25°C</th>
<th>85°C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>IEE</td>
<td>27</td>
<td>33</td>
<td></td>
<td>27</td>
</tr>
<tr>
<td>VOH</td>
<td>−1065</td>
<td>−1005</td>
<td>−880</td>
<td>−1025</td>
</tr>
<tr>
<td>VOL</td>
<td>−1830</td>
<td>−1695</td>
<td>−1555</td>
<td>−1810</td>
</tr>
<tr>
<td>VIH</td>
<td>−1165</td>
<td>−880</td>
<td></td>
<td>−1165</td>
</tr>
<tr>
<td>VIIL</td>
<td>−1810</td>
<td>−1475</td>
<td></td>
<td>−1810</td>
</tr>
<tr>
<td>VBB</td>
<td>−1.38</td>
<td>−1.26</td>
<td></td>
<td>−1.38</td>
</tr>
<tr>
<td>VIHCMR</td>
<td>−2.5</td>
<td>−0.4</td>
<td></td>
<td>−2.5</td>
</tr>
<tr>
<td>IIH</td>
<td>150</td>
<td>150</td>
<td></td>
<td>150</td>
</tr>
</tbody>
</table>

**NOTE:** Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

1. Input and output parameters vary 1:1 with \(V_{CC}\). \(V_{EE}\) can vary +0.8 V / −0.5 V.
2. Outputs are terminated through a 50 Ω resistor to \(V_{CC} − 2.0 \text{ V}\).
3. \(V_{IHCMR}\) min varies 1:1 with \(V_{EE}\), \(V_{IHCMR}\) max varies 1:1 with \(V_{CC}\). The \(V_{IHCMR}\) range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between \(V_{PP\text{min}}\) and 1 V.
### Table 7. AC CHARACTERISTICS (VCC = 5.0 V; VEE = 0.0 V or VCC = 0.0 V; VEE = −5.0 V (Note 1))

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>-40°C</th>
<th>25°C</th>
<th>85°C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>fmax</td>
<td>Maximum Toggle Frequency</td>
<td>3.4</td>
<td>4.2</td>
<td>3.8</td>
</tr>
<tr>
<td>tPLH</td>
<td>Propagation Delay</td>
<td>560</td>
<td>670</td>
<td>860</td>
</tr>
<tr>
<td></td>
<td>CLK to Q</td>
<td>400</td>
<td>540</td>
<td>700</td>
</tr>
<tr>
<td>tPHL</td>
<td>Reset to Q</td>
<td>560</td>
<td>670</td>
<td>860</td>
</tr>
<tr>
<td></td>
<td>Propagation Delay</td>
<td>400</td>
<td>540</td>
<td>700</td>
</tr>
<tr>
<td>trr</td>
<td>Set/Reset Recovery</td>
<td>400</td>
<td>200</td>
<td>400</td>
</tr>
<tr>
<td>vPP</td>
<td>Input Swing (Note 2)</td>
<td>150</td>
<td>1000</td>
<td>150</td>
</tr>
<tr>
<td>tJITTER</td>
<td>Cycle-to-Cycle Jitter</td>
<td>1.0</td>
<td></td>
<td>1.0</td>
</tr>
<tr>
<td>tr</td>
<td>Output Rise/Fall Times Q (20%–80%)</td>
<td>100</td>
<td>225</td>
<td>350</td>
</tr>
</tbody>
</table>

**NOTE:** Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

1. 10 Series: VEE can vary +0.25 V / −0.5 V.
2. 100 Series: VEE can vary +0.8 V / −0.5 V.
3. VPP(min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

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**Figure 2. Timing Diagram**

**Figure 3. Typical Termination for Output Driver and Device Evaluation**

(See Application Note AND8020/D – Termination of ECL Logic Devices)
### Resource Reference of Application Notes

| AN1405/D | - | ECL Clock Distribution Techniques |
| AN1406/D | - | Designing with PECL (ECL at +5.0 V) |
| AN1503/D | - | ECLinPS™ I/O SPICE Modeling Kit |
| AN1504/D | - | Metastability and the ECLinPS Family |
| AN1568/D | - | Interfacing Between LVDS and ECL |
| AN1672/D | - | The ECL Translator Guide |
| AND8001/D | - | Odd Number Counters Design |
| AND8002/D | - | Marking and Date Codes |
| AND8020/D | - | Termination of ECL Logic Devices |
| AND8066/D | - | Interfacing with ECLinPS |
| AND8090/D | - | AC Characteristics of ECL Devices |

ECLinPS is a trademark of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries.
NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

<table>
<thead>
<tr>
<th>DIM</th>
<th>MIN</th>
<th>MAX</th>
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*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
**STYLE 1:**
- **PIN 1.** Emitter
- **PIN 2.** Collector
- **PIN 3.** Collector
- **PIN 4.** Emitter
- **PIN 5.** Emitter
- **PIN 6.** Base
- **PIN 7.** Base
- **PIN 8.** Emitter

**STYLE 2:**
- **PIN 1.** Collector, Die, #1
- **PIN 2.** Collector, Die, #1
- **PIN 3.** Collector, Die, #2
- **PIN 4.** Collector, Die, #2
- **PIN 5.** Emitter, Die, #2
- **PIN 6.** Emitter, Die, #2
- **PIN 7.** Base, Die #2
- **PIN 8.** Emitter, Die, #1

**STYLE 3:**
- **PIN 1.** Drain, Die #1
- **PIN 2.** Drain, Die #1
- **PIN 3.** Drain, Die #2
- **PIN 4.** Drain, Die #2
- **PIN 5.** Emitter, Die #2
- **PIN 6.** Emitter, Die #2
- **PIN 7.** Base, Die #1
- **PIN 8.** Emitter, Die, #1

**STYLE 4:**
- **PIN 1.** Collector, Die #1
- **PIN 2.** Collector, Die #1
- **PIN 3.** Collector, Die #2
- **PIN 4.** Collector, Die #2
- **PIN 5.** Emitter, #2
- **PIN 6.** Emitter, #2
- **PIN 7.** Base, #2
- **PIN 8.** Collector, #1

**STYLE 5:**
- **PIN 1.** Drain
- **PIN 2.** Drain
- **PIN 3.** Drain
- **PIN 4.** Drain
- **PIN 5.** Gate
- **PIN 6.** Gate
- **PIN 7.** Source
- **PIN 8.** Source

**STYLE 6:**
- **PIN 1.** Source
- **PIN 2.** Source
- **PIN 3.** Source
- **PIN 4.** Source
- **PIN 5.** Gate
- **PIN 6.** Gate
- **PIN 7.** Drain
- **PIN 8.** Source

**STYLE 7:**
- **PIN 1.** Collector, Die, #1
- **PIN 2.** Collector, Die, #1
- **PIN 3.** Collector, Die, #2
- **PIN 4.** Collector, Die, #2
- **PIN 5.** Emitter, Die, #2
- **PIN 6.** Emitter, Die, #2
- **PIN 7.** Base, Die #1
- **PIN 8.** Collector, #1

**STYLE 8:**
- **PIN 1.** Collector, Die #1
- **PIN 2.** Collector, Die #1
- **PIN 3.** Collector, Die #2
- **PIN 4.** Collector, Die #2
- **PIN 5.** Collector, Die, #2
- **PIN 6.** Collector, Die, #2
- **PIN 7.** Collector, Die #1
- **PIN 8.** Collector, Die #1

**STYLE 9:**
- **PIN 1.** Emitter, Common
- **PIN 2.** Collector, Die #1
- **PIN 3.** Collector, Die #2
- **PIN 4.** Collector, Common
- **PIN 5.** Emitter, Common
- **PIN 6.** Base, Die #2
- **PIN 7.** Base, Die #1
- **PIN 8.** Emitter, Common

**STYLE 10:**
- **PIN 1.** Ground
- **PIN 2.** Bias 1
- **PIN 3.** Output
- **PIN 4.** Ground
- **PIN 5.** Ground
- **PIN 6.** Bias 2
- **PIN 7.** Drain
- **PIN 8.** Ground

**STYLE 11:**
- **PIN 1.** Source 1
- **PIN 2.** Source 1
- **PIN 3.** Source 2
- **PIN 4.** Gate 2
- **PIN 5.** Drain 2
- **PIN 6.** Drain 2
- **PIN 7.** Drain 1
- **PIN 8.** Drain 1

**STYLE 12:**
- **PIN 1.** Emitter, Die #1
- **PIN 2.** Anode 1
- **PIN 3.** Anode 1
- **PIN 4.** Anode 1
- **PIN 5.** Cathode, Common
- **PIN 6.** Cathode, Common
- **PIN 7.** Cathode, Common
- **PIN 8.** Cathode, Common

**STYLE 13:**
- **PIN 1.** N.C.
- **PIN 2.** Source
- **PIN 3.** Source
- **PIN 4.** Gate
- **PIN 5.** Drain
- **PIN 6.** Drain
- **PIN 7.** Drain
- **PIN 8.** Drain

**STYLE 14:**
- **PIN 1.** N-Source
- **PIN 2.** Source
- **PIN 3.** Source
- **PIN 4.** Gate
- **PIN 5.** Drain
- **PIN 6.** Drain
- **PIN 7.** Drain
- **PIN 8.** Drain

**STYLE 15:**
- **PIN 1.** Anode 1
- **PIN 2.** Anode 1
- **PIN 3.** Anode 1
- **PIN 4.** Anode 1
- **PIN 5.** Cathode, Common
- **PIN 6.** Cathode, Common
- **PIN 7.** Cathode, Common
- **PIN 8.** Cathode, Common

**STYLE 16:**
- **PIN 1.** Collector, Die #1
- **PIN 2.** Collector, Die #1
- **PIN 3.** Collector, Die #2
- **PIN 4.** Collector, Die #2
- **PIN 5.** Collector, Die, #2
- **PIN 6.** Collector, Die, #2
- **PIN 7.** Collector, Die #1
- **PIN 8.** Collector, Die #1

**STYLE 17:**
- **PIN 1.** Vcc
- **PIN 2.** V2OUT
- **PIN 3.** VOUT
- **PIN 4.** TXE
- **PIN 5.** RXE
- **PIN 6.** VEE
- **PIN 7.** GND
- **PIN 8.** ACC

**STYLE 18:**
- **PIN 1.** Anode
- **PIN 2.** Anode
- **PIN 3.** Source
- **PIN 4.** Gate
- **PIN 5.** Drain
- **PIN 6.** Drain
- **PIN 7.** Drain
- **PIN 8.** Drain

**STYLE 19:**
- **PIN 1.** Cathode 1
- **PIN 2.** Cathode 2
- **PIN 3.** Cathode 3
- **PIN 4.** Cathode 4
- **PIN 5.** Cathode 5
- **PIN 6.** Common Anode
- **PIN 7.** Common Anode
- **PIN 8.** Cathode 6

**STYLE 20:**
- **PIN 1.** Cathode 1
- **PIN 2.** Cathode 2
- **PIN 3.** Cathode 3
- **PIN 4.** Cathode 4
- **PIN 5.** Cathode 5
- **PIN 6.** Common Anode
- **PIN 7.** Common Anode
- **PIN 8.** Cathode 6

**STYLE 21:**
- **PIN 1.** Source 1
- **PIN 2.** Source 1
- **PIN 3.** Source 2
- **PIN 4.** Gate 2
- **PIN 5.** Drain 2
- **PIN 6.** Drain 2
- **PIN 7.** Drain 1
- **PIN 8.** Drain 1

**STYLE 22:**
- **PIN 1.** Line 1
- **PIN 2.** Line 1
- **PIN 3.** Line 2
- **PIN 4.** Line 2
- **PIN 5.** Line 2
- **PIN 6.** Line 2
- **PIN 7.** Line 1
- **PIN 8.** Line 1

**STYLE 23:**
- **PIN 1.** Base
- **PIN 2.** Emitter
- **PIN 3.** Collector
- **PIN 4.** Collector
- **PIN 5.** Collector
- **PIN 6.** Collector
- **PIN 7.** Collector
- **PIN 8.** Collector

**STYLE 24:**
- **PIN 1.** Ground
- **PIN 2.** GND
- **PIN 3.** Enable
- **PIN 4.** ILIMIT
- **PIN 5.** Source
- **PIN 6.** Source
- **PIN 7.** Source
- **PIN 8.** Source

**STYLE 25:**
- **PIN 1.** VCC
- **PIN 2.** N/C
- **PIN 3.** REXT
- **PIN 4.** GND
- **PIN 5.** OVT
- **PIN 6.** IOU
- **PIN 7.** IOU
- **PIN 8.** IOU

**STYLE 26:**
- **PIN 1.** I/O Line 1
- **PIN 2.** I/O Line 1
- **PIN 3.** I/O Line 2
- **PIN 4.** I/O Line 2
- **PIN 5.** I/O Line 2
- **PIN 6.** I/O Line 2
- **PIN 7.** I/O Line 2
- **PIN 8.** I/O Line 2

**STYLE 27:**
- **PIN 1.** Drain 1
- **PIN 2.** Drain 1
- **PIN 3.** GATE 2
- **PIN 4.** GATE 2
- **PIN 5.** SOURCE 2
- **PIN 6.** SOURCE 2
- **PIN 7.** SOURCE 2
- **PIN 8.** SOURCE 2

**STYLE 28:**
- **PIN 1.** Drain 1
- **PIN 2.** Drain 1
- **PIN 3.** GATE 2
- **PIN 4.** GATE 2
- **PIN 5.** SOURCE 2
- **PIN 6.** SOURCE 2
- **PIN 7.** SOURCE 2
- **PIN 8.** SOURCE 2

**STYLE 29:**
- **PIN 1.** Base, Die #1
- **PIN 2.** Emitter, #1
- **PIN 3.** Base, #2
- **PIN 4.** Emitter, #2
- **PIN 5.** Collector, #2
- **PIN 6.** Collector, #2
- **PIN 7.** Collector, #1
- **PIN 8.** Collector, #1

**STYLE 30:**
- **PIN 1.** Drain 1
- **PIN 2.** Drain 1
- **PIN 3.** GATE 2
- **PIN 4.** GATE 2
- **PIN 5.** SOURCE 2
- **PIN 6.** SOURCE 2
- **PIN 7.** SOURCE 2
- **PIN 8.** SOURCE 2