MC100EPT21

3.3V Differential LVPECL/LVDS/CML to LVTTL/LVCMOS Translator

The MC100EPT21 is a Differential LVPECL/LVDS/CML to LVTTL/LVCMOS translator. Because LVPECL (Positive ECL), LVDS, and positive CML input levels and LVTTL/LVCMOS output levels are used, only +3.3 V and ground are required. The small outline 8–lead SOIC package makes the EPT21 ideal for applications which require the translation of a clock or data signal.

The \( V_{BB} \) output allows this EPT21 to be cap coupled in either single–ended or differential input mode. When single–ended cap coupled, \( V_{BB} \) output is tied to the \( D \) input and \( D \) is driven for a non–inverting buffer, or \( V_{BB} \) output is tied to the \( D \) input and \( \overline{D} \) is driven for an inverting buffer. When cap coupled differentially, \( V_{BB} \) output is connected through a resistor to each input pin. If used, the \( V_{BB} \) pin should be bypassed to \( V_{CC} \) via a 0.01 \( \mu \)F capacitor. For additional information see AND8020/D. For a single–ended direct connection use an external voltage reference source such as a resistor divider. Do not use \( V_{BB} \) for a single–ended direct connection or port to another device.

**Features**

- 1.4 ns Typical Propagation Delay
- Maximum Frequency > 275 MHz Typical
- LVPECL/LVDS/CML Inputs, LVTTL/LVCMOS Outputs
- 24 mA TTL outputs
- Operating Range: \( V_{CC} = 3.0 \) V to 3.6 V with GND = 0 V
- The 100 Series Contains Temperature Compensation
- \( V_{BB} \) Output
- These Devices are Pb–Free and are RoHS Compliant

**MARKING DIAGRAMS**

For additional marking information, refer to Application Note AND8002/D.

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.
Table 1. PIN DESCRIPTION

<table>
<thead>
<tr>
<th>PIN</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q</td>
<td>LVTTL/LVCMOS Output</td>
</tr>
<tr>
<td>D*, D*</td>
<td>Differential LVPECL/LVDS/CML Input</td>
</tr>
<tr>
<td>VCC</td>
<td>Positive Supply</td>
</tr>
<tr>
<td>VBB</td>
<td>Output Reference Voltage</td>
</tr>
<tr>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>NC</td>
<td>No Connect</td>
</tr>
<tr>
<td>EP</td>
<td>(DFN8 only) Thermal exposed pad must be</td>
</tr>
<tr>
<td></td>
<td>connected to a sufficient thermal conduit.</td>
</tr>
<tr>
<td></td>
<td>Electrically connect to the most negative</td>
</tr>
<tr>
<td></td>
<td>supply (GND) or leave unconnected, floating</td>
</tr>
<tr>
<td></td>
<td>open.</td>
</tr>
</tbody>
</table>

* Pin will default to 1/2 of VCC when left open.

Table 2. ATTRIBUTES

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Internal Input Pulldown Resistor D</td>
<td>50 kΩ</td>
</tr>
<tr>
<td>Internal Input Pulldown Resistor D, D</td>
<td>50 kΩ</td>
</tr>
<tr>
<td>Internal Input Pullup Resistor D, D</td>
<td>50 kΩ</td>
</tr>
<tr>
<td>ESD Protection</td>
<td></td>
</tr>
<tr>
<td>Human Body Model</td>
<td>&gt; 1.5 kV</td>
</tr>
<tr>
<td>Machine Model</td>
<td>&gt; 100 V</td>
</tr>
<tr>
<td>Charged Device Model</td>
<td>&gt; 2 kV</td>
</tr>
<tr>
<td>Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)</td>
<td></td>
</tr>
<tr>
<td>SOIC–8</td>
<td>Level 1</td>
</tr>
<tr>
<td>TSSOP–8</td>
<td>Level 3</td>
</tr>
<tr>
<td>DFN8</td>
<td>Level 1</td>
</tr>
<tr>
<td>Flammability Rating</td>
<td>Oxygen Index: 28 to 34</td>
</tr>
<tr>
<td></td>
<td>UL 94 V−0 @ 0.125 in</td>
</tr>
<tr>
<td>Transistor Count</td>
<td>81 Devices</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test</td>
<td></td>
</tr>
</tbody>
</table>

1. For additional information, see Application Note AND8003/D.

Figure 1. Logic Diagram and 8–Lead Pinout (Top View)
### Table 3. MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition 1</th>
<th>Condition 2</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>PECL Power Supply</td>
<td>GND = 0 V</td>
<td></td>
<td>3.8</td>
<td>V</td>
</tr>
<tr>
<td>VIN</td>
<td>PECL Input Voltage</td>
<td>GND = 0 V</td>
<td>VI ≤ VCC</td>
<td>0 to 3.8</td>
<td>V</td>
</tr>
<tr>
<td>IBB</td>
<td>VBB Sink/Source</td>
<td></td>
<td>± 0.5 mA</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>TA</td>
<td>Operating Temperature Range</td>
<td></td>
<td></td>
<td>−40 to +85</td>
<td>°C</td>
</tr>
<tr>
<td>Tstg</td>
<td>Storage Temperature Range</td>
<td></td>
<td></td>
<td>−65 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>θJA</td>
<td>Thermal Resistance (Junction−to−Ambient)</td>
<td>0 lpm</td>
<td>SO−8</td>
<td>190</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500 lpm</td>
<td>SO−8</td>
<td>130</td>
<td>°C/W</td>
</tr>
<tr>
<td>θJC</td>
<td>Thermal Resistance (Junction−to−Case)</td>
<td>Standard Board</td>
<td>SO−8</td>
<td>41 to 44</td>
<td>°C/W</td>
</tr>
<tr>
<td>θJA</td>
<td>Thermal Resistance (Junction−to−Ambient)</td>
<td>0 lpm</td>
<td>TSSOP−8</td>
<td>185</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500 lpm</td>
<td>TSSOP−8</td>
<td>140</td>
<td>°C/W</td>
</tr>
<tr>
<td>θJC</td>
<td>Thermal Resistance (Junction−to−Case)</td>
<td>Standard Board</td>
<td>TSSOP−8</td>
<td>41 to 44</td>
<td>°C/W</td>
</tr>
<tr>
<td>θJA</td>
<td>Thermal Resistance (Junction−to−Ambient)</td>
<td>0 lpm</td>
<td>DFN8</td>
<td>129</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500 lpm</td>
<td>DFN8</td>
<td>84</td>
<td>°C/W</td>
</tr>
<tr>
<td>θJC</td>
<td>Thermal Resistance (Junction−to−Case)</td>
<td>(Note 2)</td>
<td>DFN8</td>
<td>35 to 40</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

### Table 4. PECL INPUT DC CHARACTERISTICS $V_{CC} = 3.3$ V, $GND = 0.0$ V (Note 3)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>$-40^\circ C$</th>
<th>$25^\circ C$</th>
<th>$85^\circ C$</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>VIH</td>
<td>Input HIGH Voltage (Single−Ended)</td>
<td>2075</td>
<td>2420</td>
<td></td>
<td>2075</td>
</tr>
<tr>
<td>VIL</td>
<td>Input LOW Voltage (Single−Ended)</td>
<td>1355</td>
<td>1675</td>
<td></td>
<td>1355</td>
</tr>
<tr>
<td>VBB</td>
<td>Output Voltage Reference</td>
<td>1775</td>
<td>1875</td>
<td>1975</td>
<td>1775</td>
</tr>
<tr>
<td>VIHCMR</td>
<td>Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4)</td>
<td>1.2</td>
<td>3.3</td>
<td></td>
<td>1.2</td>
</tr>
<tr>
<td>IH</td>
<td>Input HIGH Current</td>
<td>150</td>
<td></td>
<td></td>
<td>150</td>
</tr>
<tr>
<td>IL</td>
<td>Input LOW Current</td>
<td>−150</td>
<td></td>
<td></td>
<td>−150</td>
</tr>
</tbody>
</table>

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Input parameters vary 1:1 with $V_{CC}$.
4. $V_{IHCMR}$ min varies 1:1 with $GND$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.
Table 5. LVTTL/LVCMOS OUTPUT DC CHARACTERISTICS $V_{CC} = 3.3$ V, $GND = 0.0$ V, $T_A = -40^\circ$C to $85^\circ$C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OH}$</td>
<td>Output HIGH Voltage</td>
<td>$I_{OH} = -3.0$ mA</td>
<td>2.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output LOW Voltage</td>
<td>$I_{OL} = 24$ mA</td>
<td>0.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{CH}$</td>
<td>Power Supply Current</td>
<td>Outputs set to HIGH</td>
<td>5</td>
<td>17</td>
<td>25</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{CL}$</td>
<td>Power Supply Current</td>
<td>Outputs set to LOW</td>
<td>8</td>
<td>21</td>
<td>30</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td>Output Short Circuit Current</td>
<td></td>
<td>$-130$</td>
<td>$-80$</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 6. AC CHARACTERISTICS $V_{CC} = 3.0$ V to $3.6$ V, $GND = 0.0$ V (Note 5)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>$-40^\circ$C</th>
<th>$25^\circ$C</th>
<th>$85^\circ$C</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{max}$</td>
<td>Maximum Frequency (Figure 2)</td>
<td>275</td>
<td>350</td>
<td>275</td>
<td>350</td>
</tr>
<tr>
<td>$t_{PLH}$, $t_{PHL}$</td>
<td>Propagation Delay to Output Differential</td>
<td>800</td>
<td>1400</td>
<td>2050</td>
<td>800</td>
</tr>
<tr>
<td>$t_{SKW}$</td>
<td>Duty Cycle Skew (Note 6)</td>
<td>45</td>
<td>50</td>
<td>55</td>
<td>45</td>
</tr>
<tr>
<td>$t_{SKPP}$</td>
<td>Part-to-Part Skew (Note 6)</td>
<td>500</td>
<td>500</td>
<td>500</td>
<td>500</td>
</tr>
<tr>
<td>$t_{JITTER}$</td>
<td>Random Clock Jitter (RMS)</td>
<td>3.5</td>
<td>5</td>
<td>3.5</td>
<td>5</td>
</tr>
<tr>
<td>$V_{PP}$</td>
<td>Input Voltage Swing (Differential Configuration)</td>
<td>150</td>
<td>800</td>
<td>1200</td>
<td>150</td>
</tr>
<tr>
<td>$t_{r}$</td>
<td>Output Rise/Fall Times ($0.8V - 2.0V$)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Measured with a 750 mV 50% duty–cycle clock source. $R_L = 500$ $\Omega$ to GND and $C_L = 20$ pF to GND. Refer to Figure 3.

6. Skews are measured between outputs under identical transitions. Duty cycle skew is measured between differential outputs using the deviations of the sum $T_{PW-}$ and $T_{PW+}$.
Figure 2. $F_{\text{max}}$

Figure 3. TTL Output Loading Used For Device Evaluation

* $C_L$ includes fixture capacitance

AC TEST LOAD

GND

CHARACTERISTIC TEST

TTL RECEIVER

APPLICATION
## ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package</th>
<th>Shipping</th>
</tr>
</thead>
<tbody>
<tr>
<td>MC100EPT21DG</td>
<td>SOIC−8 (Pb−Free)</td>
<td>98 Units / Rail</td>
</tr>
<tr>
<td>MC100EPT21DR2G</td>
<td>SOIC−8 (Pb−Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td>MC100EPT21DTG</td>
<td>TSSOP−8 (Pb−Free)</td>
<td>100 Units / Rail</td>
</tr>
<tr>
<td>MC100EPT21DTR2G</td>
<td>TSSOP−8 (Pb−Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
<tr>
<td>MC100EPT21MNR4G</td>
<td>DFN8 (Pb−Free)</td>
<td>1000 / Tape &amp; Reel</td>
</tr>
</tbody>
</table>

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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### Resource Reference of Application Notes

- **AN1405/D** – ECL Clock Distribution Techniques
- **AN1406/D** – Designing with PECL (ECL at +5.0 V)
- **AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- **AN1504/D** – Metastability and the ECLinPS Family
- **AN1568/D** – Interfacing Between LVDS and ECL
- **AN1672/D** – The ECL Translator Guide
- **AND8001/D** – Odd Number Counters Design
- **AND8002/D** – Marking and Date Codes
- **AND8020/D** – Termination of ECL Logic Devices
- **AND8066/D** – Interfacing with ECLinPS
- **AND8090/D** – AC Characteristics of ECL Devices

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ECLinPS is a trademark of Semiconductor Components Industries, LLC (SCILLC).
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

**DFN8 2x2, 0.5P**
CASE 506AA
ISSUE F

DATE 04 MAY 2016

NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

**RECOMMENDED SOLDERING FOOTPRINT***

**GENERAL MARKING DIAGRAM***

- **XX** = Specific Device Code
- **M** = Date Code
- **Pb-Free Device**

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**NOTE 3**

**NOTE 4**

- **A1** = 0.00 0.05
- **A3** = 0.20 REP
- **B** = 0.20 0.30
- **D** = 2.00 BSC
- **E2** = 0.70 0.90
- **e** = 0.50 BSC
- **K** = 0.30 REP
- **L** = 0.25 0.35
- **L1** = 0.10

**DIMENSIONS: MILLIMETERS**

- **A** = 0.60 1.00
- **A1** = 0.00 0.05
- **A3** = 0.20 REP
- **B** = 0.20 0.30
- **D** = 2.00 BSC
- **E** = 2.00 BSC
- **E2** = 0.70 0.90
- **e** = 0.50 BSC
- **K** = 0.30 REP
- **L** = 0.25 0.35
- **L1** = 0.10

**PACKAGING OUTLINE**

- **DIM** = 1.30
- **MAX** = 2.30
- **MIN** = 0.90
- **PITCH** = 0.50

**PACKAGE OUTLINE**

- **0.10**
- **0.05**
- **0.00**
- **0.08**
- **0.10**

**SCALE 4:1**

**TOP VIEW**

**SIDE VIEW**

**BOTTOM VIEW**

**A**

**B**

**C**

**D**

**E**

**L**

**DETAIL A**

**DETAIL B**

**OPTIONAL CONSTRUCTIONS**

**ALTERNATE CONSTRUCTIONS**

**SEATING PLANE**

**NOTE 4**

**NOTE 3**

**A1**

**A3**

**A3**

**A1**

**0.10**

**0.05**

**0.00**

**0.10**

**0.08**

**0.10**

**0.10**

**0.05**

**NOTES:**

2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

**A1**

**A3**

**A3**

**A1**

**0.10**

**0.05**

**0.00**

**0.10**

**0.08**

**0.10**

**0.10**

**0.05**

**NOTES:**

2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

**DFN8 2x2, 0.5P**
CASE 506AA
ISSUE F

DATE 04 MAY 2016

NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

**GENERAL MARKING DIAGRAM***

- **XX** = Specific Device Code
- **M** = Date Code
- **Pb-Free Device**

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “*”, may or may not be present. Some products may not follow the Generic Marking.
**NOTES:**

2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

**SOLDERING FOOTPRINT**

- **DIMENSIONS:**
  - A: 4.80 (0.019)
  - B: 3.80 (0.15)
  - C: 1.35 (0.053)
  - D: 0.33 (0.013)
  - G: 0.10 (0.004)
  - H: 0.10 (0.004)
  - J: 0.19 (0.007)
  - K: 0.40 (0.016)
  - M: 0.25 (0.010)
  - N: 0.25 (0.010)
  - S: 5.80 (0.228)

- **SCALE:** 6:1

**GENERIC MARKING DIAGRAM**

- **MARKING:**
  - IC: XXXXX AYYWW
  - IC (Pb-Free): XXXXX AYYWW

- **MARKING DETAILS:**
  - XXXXX = Specific Device Code
  - A = Assembly Location
  - Y = Year
  - WW = Work Week
  - Pb-Free Package:
  - *This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "\#", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**STYLES ON PAGE 2**
**STYLE 1:**
1. EMITTER
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. SOURCE
8. SOURCE

**STYLE 2:**
1. COLLECTOR, DIE, #1
2. N-GATE
3. Collector, #2
4. Collector, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

**STYLE 3:**
1. DRAIN, DIE #1
2. DRAIN
3. SOURCE
4. SOURCE
5. GATE, #2
6. GATE
7. GATE
8. SOURCE, #1

**STYLE 4:**
1. ANODE
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. ANODE
8. COMMON CATHODE

**STYLE 5:**
1. DRAIN
2. DRAIN
3. DRAIN
4. GATE
5. DRAIN
6. DRAIN
7. SOURCE
8. SOURCE

**STYLE 6:**
1. SOURCE
2. SOURCE
3. SOURCE
4. SOURCE
5. DRAIN
6. DRAIN
7. GATE
8. GROUND

**STYLE 7:**
1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. DRAIN
7. SECOND STAGE Vd
8. FIRST STAGE Vd

**STYLE 8:**
1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. ANODE
8. COMMON CATHODE

**STYLE 9:**
1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

**STYLE 10:**
1. GROUND
2. GROUND
3. GROUND
4. SOURCE
5. SOURCE
6. SOURCE
7. SOURCE
8. SOURCE

**STYLE 11:**
1. SOURCE 1
2. SOURCE 1
3. SOURCE 1/DRAIN 2
4. GATE 1
5. DRAIN 1
6. DRAIN 1
7. INPUT
8. DRAIN

**STYLE 12:**
1. SOURCE
2. SOURCE
3. SOURCE
4. SOURCE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

**STYLE 13:**
1. N.C.
2. SOURCE
3. SOURCE
4. SOURCE
5. SOURCE
6. SOURCE
7. DRAIN
8. DRAIN

**STYLE 14:**
1. N-SOURCE
2. SOURCE
3. SOURCE
4. SOURCE
5. GATE
6. DRAIN
7. DRAIN
8. DRAIN

**STYLE 15:**
1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

**STYLE 16:**
1. EMITTER, DIE #1
2. EMITTER, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

**STYLE 17:**
1. VCC
2. V2OUT
3. YOUT
4. Txe
5. Rxe
6. Vee
7. GND
8. ACC

**STYLE 18:**
1. ANODE
2. ANODE
3. SOURCE
4. SOURCE
5. GATE
6. DRAIN
7. CATHODE
8. CATHODE

**STYLE 19:**
1. SOURCE 1
2. SOURCE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. MIRROR 2
8. DRAIN

**STYLE 20:**
1. SOURCE (N)
2. SOURCE (N)
3. SOURCE
4. GATE (P)
5. DRAIN
6. MIRROR
7. DRAIN
8. DRAIN

**STYLE 21:**
1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. COMMON ANODE

**STYLE 22:**
1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. COMMON CATHODE/VCC
5. COMMON ANODE/GND
6. I/O LINE 4
7. COMMON ANODE/GND
8. COMMON ANODE/GND

**STYLE 23:**
1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

**STYLE 24:**
1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. COLLECTOR/ANODE
6. COLLECTOR/ANODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

**STYLE 25:**
1. VIN
2. N/C
3. RXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

**STYLE 26:**
1. GND
2. Emitter, #1
3. SOURCE
4. SOURCE
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

**STYLE 27:**
1. I/LIMIT
2. GATE
3. SOURCE
4. SOURCE
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

**STYLE 28:**
1. SW_TO GND
2. DASIC OFF
3. DASIC SW DET
4. GND
5. V_MON
6. V_BULK
7. V_BULK
8. VIN
TSSOP 8
CASE 948R-02
ISSUE A
DATE 04/07/2000

NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

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SCALE 2:1