3.3 V/5 V ECL 8-Bit Serial/Parallel Converter

MC100EP445

Description
The MC100EP445 is an integrated 8–bit differential serial to parallel data converter with asynchronous data synchronization. The device has two modes of operation. CKSEL HIGH mode is designed to operate NRZ data rates of up to 3.3 Gb/s, while CKSEL LOW mode is designed to operate at twice the internal clock data rate of up to 5.0 Gb/s. The conversion sequence was chosen to convert the first serial bit to Q0, the second bit to Q1, etc. Two selectable differential serial inputs, which are selected by SINSEL, provide this device with loop–back testing capability. The MC100EP445 has a SYNC pin which, when held high for at least two consecutive clock cycles, will swallow one bit of data shifting the start of the conversion data from Dn to Dn+1. Each additional shift requires an additional pulse to be applied to the SYNC pin.

Control pins are provided to reset and disable internal clock circuitry. Additionally, VBB pin is provided for single–ended input condition.

The 100 Series contains temperature compensation.

Features
- 1530 ps Propagation Delay
- 5.0 Gb/s Typical Data Rate for CLKSEL LOW Mode
- Differential Clock and Serial Inputs
- VBB Output for Single-Ended Input Applications
- Asynchronous Data Synchronization (SYNC)
- Asynchronous Master Reset (RESET)
- PECL Mode Operating Range: VCC = 3.0 V to 5.5 V with VEE = 0 V
- NECL Mode Operating Range: VCC = 0 V with VEE = −3.0 V to −5.5 V
- Open Input Default State
- CLK ENABLE Immune to Runt Pulse Generation
- These Devices are Pb–Free and are RoHS Compliant

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package</th>
<th>Shipping</th>
</tr>
</thead>
<tbody>
<tr>
<td>MC100EP445FAG</td>
<td>LQFP–32</td>
<td>250 Units / Tray</td>
</tr>
<tr>
<td></td>
<td>(Pb–Free)</td>
<td></td>
</tr>
<tr>
<td>MC100EP445MNG</td>
<td>QFN–32</td>
<td>74 Units / Tube</td>
</tr>
<tr>
<td></td>
<td>(Pb–Free)</td>
<td></td>
</tr>
</tbody>
</table>

(Note: Microdot may be in either location)
*For additional marking information, refer to Application Note AND8002/D.
Warning: All VCC and VEE pins must be externally connected to Power Supply to guarantee proper operation.

Table 1. PIN DESCRIPTION

<table>
<thead>
<tr>
<th>Pin</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>SINA*, SINA*</td>
<td>ECL Differential Serial Data Input A</td>
</tr>
<tr>
<td>SINB*, SINB*</td>
<td>ECL Differential Serial Data Input B</td>
</tr>
<tr>
<td>SINSEL*</td>
<td>ECL Serial Input Selector Pin</td>
</tr>
<tr>
<td>CLK*, CLK*</td>
<td>ECL Differential Clock Inputs</td>
</tr>
<tr>
<td>PCLK, PCLK</td>
<td>ECL Differential Parallel Clock Output</td>
</tr>
<tr>
<td>SYNC*</td>
<td>ECL Conversion Synchronizing Input</td>
</tr>
<tr>
<td>CKSEL*</td>
<td>ECL Clock Input Selector Pin</td>
</tr>
<tr>
<td>VBB0, VBB1</td>
<td>Output Reference Voltage</td>
</tr>
<tr>
<td>RESET*</td>
<td>ECL Reset Pin</td>
</tr>
<tr>
<td>VCC</td>
<td>Positive Supply</td>
</tr>
<tr>
<td>VEE</td>
<td>Negative Supply</td>
</tr>
<tr>
<td>EP</td>
<td>The exposed pad (EP) on the QFN–32 package bottom is thermally connected to the die for improved heat transfer out of the package. The exposed pad must be attached to a heat–sinking conduit. The pad is electrically connected to VEE.</td>
</tr>
</tbody>
</table>

* Pins will default logic LOW or differential logic LOW when left open.
### Table 2. TRUTH TABLE

<table>
<thead>
<tr>
<th>PIN</th>
<th>Function</th>
<th>High</th>
<th>Low</th>
</tr>
</thead>
<tbody>
<tr>
<td>SINSEL</td>
<td>Select SINB Input</td>
<td>Select SINA Input</td>
<td></td>
</tr>
<tr>
<td>CKSEL</td>
<td></td>
<td>Q: PCLK = 8:1</td>
<td>Q: PCLK = 8:1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CLK: Q = 1:1</td>
<td>CLK: Q = 1:2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>clk</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Q</td>
<td>Q</td>
</tr>
<tr>
<td>CKEN</td>
<td>Synchronously Disable Internal Clock Circuitry</td>
<td>Synchronously Enable Internal Clock Circuitry</td>
<td></td>
</tr>
<tr>
<td>RESET</td>
<td>Asynchronous Master Reset</td>
<td>Synchronous Enable</td>
<td></td>
</tr>
<tr>
<td>SYNC</td>
<td>Asynchronously Applied to Swallow a Data Bit</td>
<td>Normal Conversion Process</td>
<td></td>
</tr>
</tbody>
</table>

### Figure 3. Logic Diagram
Table 3. ATTRIBUTES

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Value</th>
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</thead>
<tbody>
<tr>
<td>Internal Input Pulldown Resistor</td>
<td>75 kΩ</td>
</tr>
<tr>
<td>Internal Input Pull−up Resistor</td>
<td>N/A</td>
</tr>
<tr>
<td>ESD Protection</td>
<td></td>
</tr>
<tr>
<td>Human Body Model</td>
<td>&gt; 2 kV</td>
</tr>
<tr>
<td>Machine Model</td>
<td>&gt; 200 V</td>
</tr>
<tr>
<td>Charged Device Model</td>
<td>&gt; 2 kV</td>
</tr>
<tr>
<td>Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)</td>
<td>Pb−Free Pkg</td>
</tr>
<tr>
<td>LQFP−32</td>
<td>Level 2</td>
</tr>
<tr>
<td>QFN−32</td>
<td>Level 1</td>
</tr>
<tr>
<td>Flammability Rating</td>
<td></td>
</tr>
<tr>
<td>Oxygen Index: 28 to 34</td>
<td>UL 94 V−0 @ 0.125 in</td>
</tr>
<tr>
<td>Transistor Count</td>
<td>993 Devices</td>
</tr>
<tr>
<td>Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test</td>
<td></td>
</tr>
</tbody>
</table>

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition 1</th>
<th>Condition 2</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>PECL Mode Power Supply</td>
<td>VEE = 0 V</td>
<td></td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>VEE</td>
<td>NECL Mode Power Supply</td>
<td>VCC = 0 V</td>
<td></td>
<td>−6</td>
<td>V</td>
</tr>
<tr>
<td>VI</td>
<td>PECL Mode Input Voltage</td>
<td>VEE = 0 V</td>
<td>VCC ≤ VI</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>NECL Mode Input Voltage</td>
<td>VCC = 0 V</td>
<td>VI ≥ VEE</td>
<td>−6</td>
<td>V</td>
</tr>
<tr>
<td>Iout</td>
<td>Output Current</td>
<td>Continuous</td>
<td></td>
<td>50</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Surge</td>
<td></td>
<td>100</td>
<td>mA</td>
</tr>
<tr>
<td>IBB</td>
<td>VBB Sink/Source</td>
<td></td>
<td></td>
<td>±0.5</td>
<td>mA</td>
</tr>
<tr>
<td>TA</td>
<td>Operating Temperature Range</td>
<td>−40 to +85°C</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Tstg</td>
<td>Storage Temperature Range</td>
<td>−65 to +150°C</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>θJA</td>
<td>Thermal Resistance (Junction−to−Ambient)</td>
<td>0 lpfm</td>
<td>32 LQFP</td>
<td>80</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500 lpfm</td>
<td>32 LQFP</td>
<td>55</td>
<td>°C/W</td>
</tr>
<tr>
<td>θJC</td>
<td>Thermal Resistance (Junction−to−Case)</td>
<td>Standard Board</td>
<td>32 LQFP</td>
<td>12 to 17</td>
<td>°C/W</td>
</tr>
<tr>
<td>θJA</td>
<td>Thermal Resistance (Junction−to−Ambient)</td>
<td>0 lpfm</td>
<td>QFN−32</td>
<td>31</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500 lpfm</td>
<td>QFN−32</td>
<td>27</td>
<td>°C/W</td>
</tr>
<tr>
<td>θJC</td>
<td>Thermal Resistance (Junction−to−Case)</td>
<td>2S2P</td>
<td>QFN−32</td>
<td>12</td>
<td>°C/W</td>
</tr>
<tr>
<td>Tsol</td>
<td>Wave Solder (Pb−Free)</td>
<td>&lt;2 to 3 sec @ 260°C</td>
<td></td>
<td>265</td>
<td>°C</td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
Table 5. 100EP DC CHARACTERISTICS, PECL, $V_{CC} = 3.3\, V$, $V_{EE} = 0\, V$ (Note 2)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>$-40^\circ C$</th>
<th>$25^\circ C$</th>
<th>$85^\circ C$</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>IEE</td>
<td>Power Supply Current</td>
<td>95</td>
<td>119</td>
<td>143</td>
<td>98</td>
</tr>
<tr>
<td>VOH</td>
<td>Output HIGH Voltage (Note 3)</td>
<td>2155</td>
<td>2280</td>
<td>2405</td>
<td>2155</td>
</tr>
<tr>
<td>VOL</td>
<td>Output LOW Voltage (Note 3)</td>
<td>1305</td>
<td>1480</td>
<td>1605</td>
<td>1305</td>
</tr>
<tr>
<td>VIH</td>
<td>Input HIGH Voltage (Single–Ended)</td>
<td>2075</td>
<td>2420</td>
<td>2420</td>
<td>2075</td>
</tr>
<tr>
<td>VIL</td>
<td>Input LOW Voltage (Single–Ended)</td>
<td>1305</td>
<td>1675</td>
<td>1675</td>
<td>1305</td>
</tr>
<tr>
<td>VBB</td>
<td>Output Voltage Reference</td>
<td>1775</td>
<td>1875</td>
<td>1975</td>
<td>1775</td>
</tr>
<tr>
<td>VIHCMR</td>
<td>Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4)</td>
<td>2.0</td>
<td>3.3</td>
<td>3.3</td>
<td>2.0</td>
</tr>
<tr>
<td>IIH</td>
<td>Input HIGH Current</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>IIL</td>
<td>Input LOW Current</td>
<td>150</td>
<td>150</td>
<td>150</td>
<td>150</td>
</tr>
</tbody>
</table>

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

2. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary $+0.3\, V$ to $-2.2\, V$.

3. All loading with $50\, \Omega$ to $V_{CC} - 2.0\, V$.

4. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$. $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

Table 6. 100EP DC CHARACTERISTICS, PECL, $V_{CC} = 5.0\, V$, $V_{EE} = 0\, V$ (Note 5)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>$-40^\circ C$</th>
<th>$25^\circ C$</th>
<th>$85^\circ C$</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>IEE</td>
<td>Power Supply Current (Note 6)</td>
<td>95</td>
<td>119</td>
<td>143</td>
<td>98</td>
</tr>
<tr>
<td>VOH</td>
<td>Output HIGH Voltage (Note 7)</td>
<td>3855</td>
<td>3980</td>
<td>4105</td>
<td>3855</td>
</tr>
<tr>
<td>VOL</td>
<td>Output LOW Voltage (Note 7)</td>
<td>3005</td>
<td>3180</td>
<td>3305</td>
<td>3005</td>
</tr>
<tr>
<td>VIH</td>
<td>Input HIGH Voltage (Single–Ended)</td>
<td>3775</td>
<td>4120</td>
<td>4120</td>
<td>3775</td>
</tr>
<tr>
<td>VIL</td>
<td>Input LOW Voltage (Single–Ended)</td>
<td>3005</td>
<td>3375</td>
<td>3375</td>
<td>3005</td>
</tr>
<tr>
<td>VBB</td>
<td>Output Voltage Reference</td>
<td>3475</td>
<td>3575</td>
<td>3675</td>
<td>3475</td>
</tr>
<tr>
<td>VIHCMR</td>
<td>Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 8)</td>
<td>2.0</td>
<td>5.0</td>
<td>5.0</td>
<td>2.0</td>
</tr>
<tr>
<td>IIH</td>
<td>Input HIGH Current</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>IIL</td>
<td>Input LOW Current</td>
<td>150</td>
<td>150</td>
<td>150</td>
<td>150</td>
</tr>
</tbody>
</table>

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

5. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary $+2.0\, V$ to $-0.5\, V$.

6. Required 500 lfpm air flow when using $+5\, V$ power supply. For $(V_{CC} - V_{EE}) > 3.3\, V$, $5\, \Omega$ to $10\, \Omega$ in line with $V_{EE}$ required for maximum thermal protection at elevated temperatures. Recommend $V_{CC} - V_{EE}$ operation at $\leq 3.3\, V$.

7. All loading with $50\, \Omega$ to $V_{CC} - 2.0\, V$.

8. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$. $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.
### Table 7. 100EP DC CHARACTERISTICS, NECL

| Symbol | Characteristic | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Unit |
|-------|----------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|
| VCC   | Power Supply Current (Note 10) | 95  | 119 | 143 | 98  | 122 | 146 | 100 | 125 | 150 | mA   |
| VOH   | Output HIGH Voltage (Note 11) | −1145 | −1020 | −895 | −1145 | −1020 | −895 | −1145 | −1020 | −895 | mV   |
| VIL   | Input HIGH Voltage (Note 11) | −1995 | −1820 | −1695 | −1995 | −1820 | −1695 | −1995 | −1820 | −1695 | mV   |
| VIL   | Input LOW Voltage (Differential Configuration) | 0.5  | 0.5  | 150  | 0.5  | 0.5  | 150  | 0.5  | 0.5  | 150  | μA   |

Note: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

9. Input and output parameters vary 1:1 with VCC.
10. Required 500 lfpm air flow when using −5.0 V power supply. For (VCC − VEE) > 3.3 V, 5 Ω to 10 Ω in line with VEE required for maximum thermal protection at elevated temperatures. Recommend VCC − VEE operation at ≤ 3.3 V.
11. All loading with 50 Ω to VCC − 2.0 V.
12. VIHMR min varies 1:1 with VEE. VILR max varies 1:1 with VCC. The VIHCMR range is referenced to the most positive side of the differential input signal.

### Table 8. AC CHARACTERISTICS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>40°C</th>
<th>25°C</th>
<th>85°C</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>fmax</td>
<td>Maximum Input CLK Frequency (See Figure 13. Fmax/JITTER)</td>
<td>2.0</td>
<td>2.0</td>
<td>2.0</td>
<td>MHz</td>
</tr>
<tr>
<td>ts</td>
<td>Setup Time</td>
<td>−400</td>
<td>−459</td>
<td>−420</td>
<td>ps</td>
</tr>
<tr>
<td>th</td>
<td>Hold Time</td>
<td>533</td>
<td>474</td>
<td>490</td>
<td>ps</td>
</tr>
<tr>
<td>fRR/FRR2</td>
<td>Reset Recovery (Figure 4)</td>
<td>350</td>
<td>180</td>
<td>350</td>
<td>ps</td>
</tr>
<tr>
<td>fPW</td>
<td>Minimum Pulse Width</td>
<td>400</td>
<td>400</td>
<td>400</td>
<td>ps</td>
</tr>
</tbody>
</table>

Note: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

13. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to VCC − 2.0 V.
14. VPP(min) is the minimum input swing for which AC parameters are guaranteed.
Figure 4. Reset Recovery

Figure 5. Data Setup and Hold Time

Figure 6. CKEN Setup and Hold Time
The MC100EP445 is an integrated 1:8 serial to parallel converter with two modes of operation selected by CKSEL (Pin 7). CKSEL HIGH mode only latches data on the rising edge of the input CLK and CKSEL LOW mode latches data on both the rising and falling edge of the input CLK. CKSEL LOW is the open default state. Either of the two differential input serial data path provided for this device, SINA and SINB, can be chosen with the SINSEL pin (pin 25). SINA is the default input path when SINSEL pin is left floating. Because of internal pull-downs on the input pins, all input pins will default to logic low when left open. The two selectable serial data paths can be used for loop-back testing as well as the bit error testing.

Upon power–up, the internal flip–flops will attain a random state. To synchronize multiple flip–flops in the device, the Reset (pin 1) must be asserted. The reset pin will disable the internal clock signal irrespective of the CKEN state (CKEN disables the internal clock circuitry). The device will grab the first stream of data after the falling edge of RESET, followed by the falling edge of CLK, on second rising edge of CLK in either CKSEL modes. (See Figure 6)

![Figure 7. Reset Timing Diagram]
For CKSEL LOW operation, the data is latched on both the rising edge and the falling edge of the clock and the time from when the serial data is latched to when the data is seen on the parallel output is 6 clock cycles (see Figure 8).

Figure 8. Timing Diagram A. 1:8 Serial to Parallel Conversion with CKSEL LOW
Similarly, for CKSEL HIGH operation, the data is latched only on the rising edge of the clock and the time from when the serial data is latched to when the data is seen on the parallel output is 12 clock cycles (see Figure 9).

Figure 9. Timing Diagram A. 1:8 Serial to Parallel Conversion with CKSEL HIGH
To allow the user to synchronize the output byte data correctly, the start bit for conversion can be moved using the SYNC input pin (pin 2). Asynchronously asserting the SYNC pin will force the internal clock to swallow a clock pulse, effectively shifting a bit from the $Q_n$ to the $Q_{n-1}$ output as shown in Figure 10 and Figure 11. For CKSEL LOW, a single pulse applied asynchronously for two consecutive clock cycles shifts the start bit for conversion from $Q_n$ to $Q_{n-1}$. The bit is swallowed following the two clock cycle pulse width of SYNC on the next triggering edge of clock (either on the rising or the falling edge of the clock). Each additional shift requires an additional pulse to be applied to the SYNC pin. (See Figure 10)

Figure 10. Timing Diagram A. 1:8 Serial to Parallel Conversion with SYNC Pulse at CKSEL LOW
For CKSEL HIGH, a single pulse applied asynchronously for three consecutive clock cycles shifts the start bit for conversion from $Q_n$ to $Q_{n-1}$. The bit is swallowed following the three clock cycle pulse width of SYNC on the next triggering edge of clock (on the rising edge of the clock only). Each additional shift requires an additional pulse to be applied to the SYNC pin. (See Figure 11)

Figure 11. Timing Diagram A. 1:8 Serial to Parallel Conversion with SYNC Pulse at CKSEL HIGH
The synchronous CKEN (pin 3) applied with at least one clock cycle pulse length will disable the internal clock signal. The synchronous CKEN will suspend all of the device activities and prevent runt pulses from being generated. The rising edge of CKEN followed by the falling edge of CLK will suspend all activities. The first data bit will clock on the rising edge, since the falling edge of CKEN followed by the falling edge of the incoming clock triggers the enabling of the internal process. (See Figure 12)

![Figure 12. Timing Diagram with CKEN with CKSEL HIGH](image)

The differential PCLK output (pins 22 and 23) is a word framer and can help the user to synchronize the parallel data outputs. During CKSEL LOW operation, the PCLK will provide a divide by 4–clock frequency, which frames the serial data in period of PCLK output. Likewise during CKSEL HIGH operation, the PCLK will provide a divide by 8–clock frequency.

The VBB pin, an internally generated voltage supply, is available to this device only. For single–ended input conditions, the unused differential input is connected to VBB as a switching reference voltage. VBB may also rebias AC coupled inputs. When used, decouple VBB and VCC via a 0.01 μF capacitor, which will limit the current sourcing or sinking to 0.5mA. When not used, VBB should be left open. Also, both outputs of the differential pair must be terminated (50 Ω to VTT = VCC – 2 V) even if only one output is used.
Figure 13. $F_{\text{max}}$/Jitter

Figure 14. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques
AN1406/D – Designing with PECL (ECL at +5.0 V)
AN1503/D – ECLinPS ™ I/O SPICE Modeling Kit
AN1504/D – Metastability and the ECLinPS Family
AN1568/D – Interfacing Between LVDS and ECL
AN1672/D – The ECL Translator Guide
AND8001/D – Odd Number Counters Design
AND8002/D – Marking and Date Codes
AND8020/D – Termination of ECL Logic Devices
AND8066/D – Interfacing with ECLinPS
AND8090/D – AC Characteristics of ECL Devices

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