3.3V ECL Phase-Frequency Detector

MC100EP140

Description

The MC100EP140 is a three state phase frequency detector intended for phase-locked loop applications which require a minimum amount of phase and frequency difference at lock. Since the part is designed with fully differential internal gates, the noise is reduced throughout the circuit, especially at high speeds. The basic operation of a Phase/Frequency Detector (PFD) is to “compare” an incoming signal (feedback) to a set reference signal. When the Reference (R) and Feedback (FB) inputs are unequal in frequency and/or phase, the differential UP (U) and DOWN (D) outputs will provide pulse streams which, when subtracted and integrated, provide an error voltage for control of a VCO. Detector states of operation are shown in the Figure 2 and the State Table.

The typical output amplitude of the EP140 is 400 mV, allowing faster switching time and greater bandwidth. For proper operation, the input edge rate of the R and FB inputs should be less than 5 ns.

More information on Phase Lock Loop operation and application can be found in AND8040.

The pinout is shown in Figure 1, the logic diagram in Figure 3, and the typical termination in Figure 5.

Features

- 500 ps Typical Propagation Delay
- Maximum Frequency > 2.1 GHz Typical
- Fully Differential Internally
- Advanced High Band Output Swing of 400 mV
- Transfer Gain: 1.0 mV/Degree at 1.4 GHz
  1.2 mV/Degree at 1.0 GHz
- Rise and Fall Time: 100 ps Typical
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: \( V_{CC} = 3.0 \text{ V to } 3.6 \text{ V} \) with \( V_{EE} = 0 \text{ V} \)
- NECL Mode Operating Range: \( V_{CC} = 0 \text{ V} \) with \( V_{EE} = -3.0 \text{ V to } -3.6 \text{ V} \)
- Open Input Default State
- These are Pb-Free Devices

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.
Figure 1. 8-Lead Pinout (Top View)

Table 1. PIN DESCRIPTION

<table>
<thead>
<tr>
<th>PIN</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>D, D</td>
<td>Differential Down Outputs</td>
</tr>
<tr>
<td>U, U</td>
<td>Differential Up Outputs</td>
</tr>
<tr>
<td>R*</td>
<td>ECL Reference Input</td>
</tr>
<tr>
<td>FB*</td>
<td>ECL Feedback Input</td>
</tr>
<tr>
<td>VCC</td>
<td>Positive Supply</td>
</tr>
<tr>
<td>VEE</td>
<td>Negative Supply</td>
</tr>
</tbody>
</table>

* Pins will default LOW when left open.

Table 2. STATE TABLE

<table>
<thead>
<tr>
<th>PHASE DETECTOR STATE</th>
<th>INPUT</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>PUMP DOWN 2–1–2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>2–1</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>1–2</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>2</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>PUMP UP 2–3–2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>2–3</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>3–2</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>2</td>
<td>L</td>
<td>L</td>
</tr>
</tbody>
</table>

Figure 2. Phase Detector Logic Model

Figure 3. Logic Diagram
Table 3. ATTRIBUTES

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Internal Input Pulldown Resistor</td>
<td>75 kΩ</td>
</tr>
<tr>
<td>Internal Input Pullup Resistor</td>
<td>37.5 kΩ</td>
</tr>
<tr>
<td>ESD Protection</td>
<td></td>
</tr>
<tr>
<td>Human Body Model</td>
<td>&gt; 2 kV</td>
</tr>
<tr>
<td>Machine Model</td>
<td>&gt; 200 V</td>
</tr>
<tr>
<td>Charged Device Model</td>
<td>&gt; 2 kV</td>
</tr>
<tr>
<td>Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)</td>
<td>Pb Pkg</td>
</tr>
<tr>
<td></td>
<td>SOIC–8</td>
</tr>
<tr>
<td></td>
<td>Level 1</td>
</tr>
<tr>
<td></td>
<td>Level 1</td>
</tr>
<tr>
<td>Flammability Rating</td>
<td></td>
</tr>
<tr>
<td>Oxygen Index: 28 to 34</td>
<td>UL 94 V–0 @ 0.125 in</td>
</tr>
<tr>
<td>Transistor Count</td>
<td>457 Devices</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition 1</th>
<th>Condition 2</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>PECL Mode Power Supply</td>
<td>VEE = 0 V</td>
<td>VCC = 0 V</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>VEE</td>
<td>NECL Mode Power Supply</td>
<td></td>
<td>VEE = 0 V</td>
<td>–6</td>
<td>V</td>
</tr>
<tr>
<td>Vt</td>
<td>PECL Mode Input Voltage</td>
<td>VEE = 0 V</td>
<td>VCC = 0 V</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>NECL Mode Input Voltage</td>
<td>VEE = 0 V</td>
<td>VEE ≤ VCC</td>
<td>–6</td>
<td>V</td>
</tr>
<tr>
<td>Iout</td>
<td>Output Current</td>
<td>Continuous</td>
<td>Surge</td>
<td>50</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>100</td>
<td>mA</td>
</tr>
<tr>
<td>TA</td>
<td>Operating Temperature Range</td>
<td></td>
<td></td>
<td>–40 to +85</td>
<td>°C</td>
</tr>
<tr>
<td>Tstg</td>
<td>Storage Temperature Range</td>
<td></td>
<td></td>
<td>–65 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>θJA</td>
<td>Thermal Resistance (Junction–to–Ambient)</td>
<td>0 lfpm</td>
<td>500 lfpm</td>
<td>190</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SOIC–8</td>
<td>SOIC–8</td>
<td>130</td>
<td>°C/W</td>
</tr>
<tr>
<td>θJC</td>
<td>Thermal Resistance (Junction–to–Case)</td>
<td>Standard Board</td>
<td>SOIC–8</td>
<td>41 to 44</td>
<td>°C/W</td>
</tr>
<tr>
<td>Tsol</td>
<td>Wave Solder</td>
<td></td>
<td>Pb</td>
<td>265</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Pb–Free</td>
<td>265</td>
<td>°C</td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 5. 100EP DC CHARACTERISTICS, PECL VCC = 3.3 V, VEE = 0 V (Note 2)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>–40°C</th>
<th>25°C</th>
<th>85°C</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>IEE</td>
<td>Power Supply Current</td>
<td>45</td>
<td>65</td>
<td>85</td>
<td>50</td>
</tr>
<tr>
<td>VOH</td>
<td>Output HIGH Voltage (Note 3)</td>
<td>2255</td>
<td>2350</td>
<td>2475</td>
<td>2275</td>
</tr>
<tr>
<td>VDL</td>
<td>Output LOW Voltage (Note 3)</td>
<td>1755</td>
<td>1900</td>
<td>2025</td>
<td>1800</td>
</tr>
<tr>
<td>VIH</td>
<td>Input HIGH Voltage (Single–Ended)</td>
<td>2075</td>
<td>2420</td>
<td>2420</td>
<td>2075</td>
</tr>
<tr>
<td>VIL</td>
<td>Input LOW Voltage (Single–Ended)</td>
<td>1355</td>
<td>1675</td>
<td>1675</td>
<td>1355</td>
</tr>
<tr>
<td>IH</td>
<td>Input HIGH Current</td>
<td>0.5</td>
<td>0.5</td>
<td>150</td>
<td>0.5</td>
</tr>
<tr>
<td>IIL</td>
<td>Input LOW Current</td>
<td>0.5</td>
<td>0.5</td>
<td>150</td>
<td>0.5</td>
</tr>
</tbody>
</table>

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

2. Input and output parameters vary 1:1 with VCC. VEE can vary +0.3 V to –0.3 V.
3. All loading with 50 Ω to VCC – 2.0 V.
Table 6. 100EP DC CHARACTERISTICS, NECL \( V_{CC} = 0 \) V, \( V_{EE} = -3.6 \) V to \(-3.0 \) V (Note 4)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>(-40^\circ C)</th>
<th>(25^\circ C)</th>
<th>(85^\circ C)</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{EE} )</td>
<td>Power Supply Current</td>
<td>45</td>
<td>65</td>
<td>85</td>
<td>50</td>
</tr>
<tr>
<td>( V_{OH} )</td>
<td>Output HIGH Voltage (Note 5)</td>
<td>(-1075)</td>
<td>(-950)</td>
<td>(-825)</td>
<td>(-1025)</td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>Output LOW Voltage (Note 5)</td>
<td>(-1525)</td>
<td>(-1400)</td>
<td>(-1275)</td>
<td>(-1500)</td>
</tr>
<tr>
<td>( V_{IH} )</td>
<td>Input HIGH Voltage (Single–Ended)</td>
<td>(-1225)</td>
<td>(-880)</td>
<td>(-1225)</td>
<td>(-880)</td>
</tr>
<tr>
<td>( V_{IL} )</td>
<td>Input LOW Voltage (Single–Ended)</td>
<td>(-1945)</td>
<td>(-1625)</td>
<td>(-1945)</td>
<td>(-1625)</td>
</tr>
<tr>
<td>( I_{IH} )</td>
<td>Input HIGH Current</td>
<td>150</td>
<td>150</td>
<td>150</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>( I_{IL} )</td>
<td>Input LOW Current</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>(\mu A)</td>
</tr>
</tbody>
</table>

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

4. Input and output parameters vary 1:1 with \( V_{CC} \).
5. All loading with 50 \(\Omega\) to \( V_{CC} – 2.0 \) V.

Table 7. AC CHARACTERISTICS \( V_{CC} = 0 \) V; \( V_{EE} = -3.0 \) V to \(-3.6 \) V or \( V_{CC} = 3.0 \) V to 3.6 V; \( V_{EE} = 0 \) V (Note 6)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>(-40^\circ C)</th>
<th>(25^\circ C)</th>
<th>(85^\circ C)</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{max} )</td>
<td>Maximum Frequency (Figure 4)</td>
<td>&gt; 2</td>
<td>&gt; 2</td>
<td>&gt; 2</td>
<td>GHz</td>
</tr>
<tr>
<td>( t_{PLH}, t_{PHL} )</td>
<td>Propagation Delay to R to U, FB to D</td>
<td>300</td>
<td>450</td>
<td>6002</td>
<td>325</td>
</tr>
<tr>
<td></td>
<td>Output Differential</td>
<td>400</td>
<td>600</td>
<td>800</td>
<td>450</td>
</tr>
<tr>
<td>( t_{JITTER} )</td>
<td>Cycle–to–Cycle Jitter (Figure 4)</td>
<td>.2</td>
<td>&lt; 1</td>
<td>.2</td>
<td>&lt; 1</td>
</tr>
<tr>
<td>( V_{PP} )</td>
<td>Input Voltage Swing</td>
<td>400</td>
<td>800</td>
<td>1200</td>
<td>400</td>
</tr>
<tr>
<td>( t_{r}, t_{f} )</td>
<td>Output Rise/Fall Times (20% – 80%)</td>
<td>Q, (\overline{Q})</td>
<td>50</td>
<td>90</td>
<td>180</td>
</tr>
</tbody>
</table>

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

6. Measured using a 750 mV \( V_{PP} \) pk–pk, 50% duty cycle, clock source. All loading with 50 \(\Omega\) to \( V_{CC} – 2.0 \) V.
Figure 5. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package</th>
<th>Shipping†</th>
</tr>
</thead>
<tbody>
<tr>
<td>MC100EP140DG</td>
<td>SOIC–8 (Pb–Free)</td>
<td>98 Units / Rail</td>
</tr>
<tr>
<td>MC100EP140DR2G</td>
<td>SOIC–8 (Pb–Free)</td>
<td>2500 / Tape &amp; Reel</td>
</tr>
</tbody>
</table>

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

- AN1405/D – ECL Clock Distribution Techniques
- AN1406/D – Designing with PECL (ECL at +5.0 V)
- AN1503/D – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D – Metastability and the ECLinPS Family
- AN1568/D – Interfacing Between LVDS and ECL
- AN1672/D – The ECL Translator Guide
- AND8001/D – Odd Number Counters Design
- AND8002/D – Marking and Date Codes
- AND8020/D – Termination of ECL Logic Devices
- AND8066/D – Interfacing with ECLinPS
- AND8090/D – AC Characteristics of ECL Devices

ECLinPS is a trademark of Semiconductor Components Industries, LLC (SCILLC).
NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

<table>
<thead>
<tr>
<th>MILLIMETERS</th>
<th>INCHES</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIM</td>
<td>MIN</td>
</tr>
<tr>
<td>A</td>
<td>4.80</td>
</tr>
<tr>
<td>B</td>
<td>3.60</td>
</tr>
<tr>
<td>C</td>
<td>1.35</td>
</tr>
<tr>
<td>D</td>
<td>0.53</td>
</tr>
<tr>
<td>G</td>
<td>1.27</td>
</tr>
<tr>
<td>H</td>
<td>0.10</td>
</tr>
<tr>
<td>J</td>
<td>0.19</td>
</tr>
<tr>
<td>K</td>
<td>0.40</td>
</tr>
<tr>
<td>M</td>
<td>0</td>
</tr>
<tr>
<td>N</td>
<td>0.25</td>
</tr>
<tr>
<td>S</td>
<td>5.80</td>
</tr>
</tbody>
</table>

*This information is generic. Please refer to device data sheet for actual part marking.
Pb–Free indicator, “G” or microdot “×”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2
**DOCUMENT NUMBER:** 98ASB42564B  
**DESCRIPTION:** SOIC-8 NB

<table>
<thead>
<tr>
<th>STYLE 1</th>
<th>STYLE 2</th>
<th>STYLE 3</th>
<th>STYLE 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIN 1. EMITTER</td>
<td>PIN 1. COLLECTOR, DIE, #1</td>
<td>PIN 1. DRAIN, DIE #1</td>
<td>PIN 1. ANODE</td>
</tr>
<tr>
<td>2. SOURCE</td>
<td>3. SOURCE</td>
<td>4. GATE</td>
<td>2. BASE, DIE #1</td>
</tr>
<tr>
<td>4. EMITTER</td>
<td>5. EMITTER, #2</td>
<td>6. SOURCE, #2</td>
<td>3. ANODE</td>
</tr>
<tr>
<td>6. BASE</td>
<td>7. BASE</td>
<td>8. SOURCE, #1</td>
<td>4. ANODE</td>
</tr>
<tr>
<td>7. BASE</td>
<td></td>
<td></td>
<td>5. ANODE</td>
</tr>
<tr>
<td>8. EMITTER</td>
<td></td>
<td></td>
<td>6. ANODE</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>STYLE 5</th>
<th>STYLE 6</th>
<th>STYLE 7</th>
<th>STYLE 8</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIN 1. DRAIN</td>
<td>PIN 1. SOURCE</td>
<td>PIN 1. INPUT</td>
<td>PIN 1. COLLECTOR, DIE #1</td>
</tr>
<tr>
<td>2. DRAIN</td>
<td>3. DRAIN</td>
<td>2. BASE</td>
<td>3. BASE, DIE #2</td>
</tr>
<tr>
<td>3. DRAIN</td>
<td>4. SOURCE</td>
<td>3. COLLECTOR, DIE #2</td>
<td>4. COLLECTOR, #2</td>
</tr>
<tr>
<td>4. DRAIN</td>
<td>5. SOURCE</td>
<td>4. COLLECTOR, #2</td>
<td>5. COLLECTOR, #2</td>
</tr>
<tr>
<td>5. GATE</td>
<td>6. GATE</td>
<td>6. EMITTER, #2</td>
<td>6. EMITTER, #2</td>
</tr>
<tr>
<td>6. GATE</td>
<td>7. SOURCE</td>
<td>7. GATE</td>
<td>7. GATE</td>
</tr>
<tr>
<td>7. SOURCE</td>
<td>8. SOURCE</td>
<td>8. FIRST STAGE Vd</td>
<td>8. FIRST STAGE Vd</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>STYLE 9</th>
<th>STYLE 10</th>
<th>STYLE 11</th>
<th>STYLE 12</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIN 1. EMITTER, COMMON</td>
<td>PIN 1. GROUND</td>
<td>PIN 1. SOURCE</td>
<td>PIN 1. SOURCE</td>
</tr>
<tr>
<td>2. COLLECTOR, DIE #1</td>
<td>3. OUTPUT</td>
<td>2. SOURCE</td>
<td>2. SOURCE</td>
</tr>
<tr>
<td>3. COLLECTOR, DIE #2</td>
<td>4. GROUND</td>
<td>3. SOURCE</td>
<td>3. SOURCE</td>
</tr>
<tr>
<td>4. EMITTER, COMMON</td>
<td>5. GROUND</td>
<td>4. GATE</td>
<td>4. GATE</td>
</tr>
<tr>
<td>5. EMITTER, COMMON</td>
<td>6. BIAS 2</td>
<td>5. DRAIN</td>
<td>5. DRAIN</td>
</tr>
<tr>
<td>6. BASE, DIE #2</td>
<td>7. INPUT</td>
<td>6. DRAIN</td>
<td>6. DRAIN</td>
</tr>
<tr>
<td>7. BASE, DIE #1</td>
<td>8. GROUND</td>
<td>7. DRAIN</td>
<td>7. DRAIN</td>
</tr>
<tr>
<td>8. EMITTER, COMMON</td>
<td></td>
<td>8. DRAIN</td>
<td>8. DRAIN</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>STYLE 13</th>
<th>STYLE 14</th>
<th>STYLE 15</th>
<th>STYLE 16</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIN 1. N.C.</td>
<td>PIN 1. N-SOURCE</td>
<td>PIN 1. ANODE</td>
<td>PIN 1. EMITTER, DIE #1</td>
</tr>
<tr>
<td>2. SOURCE</td>
<td>3. P-SOURCE</td>
<td>2. ANODE</td>
<td>2. ANODE</td>
</tr>
<tr>
<td>3. SOURCE</td>
<td>4. P-GATE</td>
<td>3. ANODE</td>
<td>3. ANODE</td>
</tr>
<tr>
<td>4. GATE</td>
<td>5. P-DRAIN</td>
<td>4. ANODE</td>
<td>4. ANODE</td>
</tr>
<tr>
<td>5. DRAIN</td>
<td>6. P-DRAIN</td>
<td>5. CATHODE, COMMON</td>
<td>5. CATHODE, COMMON</td>
</tr>
<tr>
<td>7. DRAIN</td>
<td>8. N-DRAIN</td>
<td>7. CATHODE, COMMON</td>
<td>7. CATHODE, COMMON</td>
</tr>
<tr>
<td>8. DRAIN</td>
<td></td>
<td>8. CATHODE, COMMON</td>
<td>8. CATHODE, DIE #1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>STYLE 17</th>
<th>STYLE 18</th>
<th>STYLE 19</th>
<th>STYLE 20</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIN 1. VCC</td>
<td>PIN 1. ANODE</td>
<td>PIN 1. SOURCE</td>
<td>PIN 1. SOURCE (N)</td>
</tr>
<tr>
<td>2. V2OUT</td>
<td>2. ANODE</td>
<td>1. SOURCE</td>
<td>1. SOURCE</td>
</tr>
<tr>
<td>3. VOUT</td>
<td>3. SOURCE</td>
<td>2. GATE</td>
<td>2. GATE</td>
</tr>
<tr>
<td>4. TXE</td>
<td>4. GATE</td>
<td>3. SOURCE</td>
<td>3. SOURCE</td>
</tr>
<tr>
<td>5. RXE</td>
<td>5. DRAIN</td>
<td>4. GATE</td>
<td>4. GATE</td>
</tr>
<tr>
<td>6. VEE</td>
<td>6. MIRROR 2</td>
<td>5. DRAIN</td>
<td>5. DRAIN</td>
</tr>
<tr>
<td>7. GND</td>
<td>7. MIRROR 1</td>
<td>6. DRAIN</td>
<td>6. DRAIN</td>
</tr>
<tr>
<td>8. ACC</td>
<td>8. MIRROR 1</td>
<td>7. DRAIN</td>
<td>7. DRAIN</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8. DRAIN</td>
<td>8. DRAIN</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>STYLE 21</th>
<th>STYLE 22</th>
<th>STYLE 23</th>
<th>STYLE 24</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIN 1. CATHODE 1</td>
<td>PIN 1. I/O LINE 1</td>
<td>PIN 1. LINE 1 IN</td>
<td>PIN 1. BASE</td>
</tr>
<tr>
<td>2. CATHODE 2</td>
<td>3. COMMON CATHODE/VCC</td>
<td>2. COMMON ANODE/GND</td>
<td>2. EMITTER</td>
</tr>
<tr>
<td>3. CATHODE 3</td>
<td>4. COMMON CATHODE/VCC</td>
<td>3. COMMON ANODE/GND</td>
<td>3. COLLECTOR/ANODE</td>
</tr>
<tr>
<td>4. CATHODE 4</td>
<td>5. COMMON ANODE/GND</td>
<td>4. LINE 2</td>
<td>4. COLLECTOR/ANODE</td>
</tr>
<tr>
<td>5. CATHODE 5</td>
<td>6. I/O LINE 3</td>
<td>5. LINE 2 OUT</td>
<td>5. CATHODE</td>
</tr>
<tr>
<td>6. COMMON ANODE</td>
<td>7. COMMON ANODE</td>
<td>6. COMMON ANODE/GND</td>
<td>6. CATHODE</td>
</tr>
<tr>
<td>7. COMMON ANODE</td>
<td>8. COMMON ANODE/GND</td>
<td>7. COMMON ANODE/GND</td>
<td>7. COLLECTOR/ANODE</td>
</tr>
<tr>
<td>8. CATHODE 6</td>
<td></td>
<td>8. LINE 1 OUT</td>
<td>8. COLLECTOR/ANODE</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>STYLE 25</th>
<th>STYLE 26</th>
<th>STYLE 27</th>
<th>STYLE 28</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIN 1. VIN</td>
<td>PIN 1. GND</td>
<td>PIN 1. ILIMIT</td>
<td>PIN 1. SW_TO_GND</td>
</tr>
<tr>
<td>2. N/C</td>
<td>2. dV/dt</td>
<td>2. OVLO</td>
<td>2. DASIC_OFF</td>
</tr>
<tr>
<td>3. RXET</td>
<td>3. GATE</td>
<td>3. UVLO</td>
<td>3. DASIC_SW_DET</td>
</tr>
<tr>
<td>4. GND</td>
<td>4. ILIMIT</td>
<td>4. INPUT+</td>
<td>4. GND</td>
</tr>
<tr>
<td>5. IP</td>
<td>5. SOURCE</td>
<td>5. SOURCE</td>
<td>5. V_MON</td>
</tr>
<tr>
<td>7. OUT</td>
<td>7. SOURCE</td>
<td>7. SOURCE</td>
<td>7. VBUSK</td>
</tr>
<tr>
<td>8. GND</td>
<td>8. DRIN</td>
<td>8. BIAS</td>
<td>8. VIN</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>STYLE 29</th>
<th>STYLE 30</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>PIN 1. BASE, DIE #1</td>
<td>PIN 1. DRAIN</td>
<td></td>
</tr>
<tr>
<td>2. EMITTER, #1</td>
<td>2. DRAIN</td>
<td></td>
</tr>
<tr>
<td>3. BASE, #2</td>
<td>3. DRAIN</td>
<td></td>
</tr>
<tr>
<td>4. EMITTER, #2</td>
<td>4. SOURCE</td>
<td></td>
</tr>
<tr>
<td>5. COLLECTOR, #2</td>
<td>5. SOURCE</td>
<td></td>
</tr>
<tr>
<td>6. COLLECTOR, #2</td>
<td>6. SOURCE</td>
<td></td>
</tr>
<tr>
<td>7. COLLECTOR, #1</td>
<td>7. SOURCE</td>
<td></td>
</tr>
<tr>
<td>8. COLLECTOR, #1</td>
<td>8. GATE</td>
<td></td>
</tr>
</tbody>
</table>

**DESCRIPTION:** SOIC-8 NB

**DATE 16 FEB 2011**

Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.

© Semiconductor Components Industries, LLC, 2019

www.onsemi.com
onsemi, ON Semiconductor, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba “onsemi” or its affiliates and/or subsidiaries in the United States and/or other countries. onsemi owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of onsemi’s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. onsemi reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided “as−is” and onsemi makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using onsemi products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by onsemi. “Typical” parameters which may be provided in onsemi data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals” must be validated for each customer application by customer’s technical experts. onsemi does not convey any license under any of its intellectual property rights nor the rights of others. onsemi products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use onsemi products for any such unintended or unauthorized application, Buyer shall indemnify and hold onsemi and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that onsemi was negligent regarding the design or manufacture of the part. onsemi is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.