

# LM324S, LM2902S

## Single Supply Quad Operational Amplifiers

The LM324S and LM2902S are low-cost, quad operational amplifiers with true differential inputs. They have several distinct advantages over standard operational amplifier types in single supply applications. The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

### Features

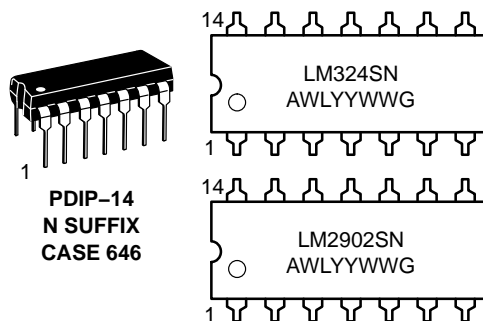
- Short Circuited Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 V to 32 V
- Four Amplifiers Per Package
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Industry Standard Pinouts
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



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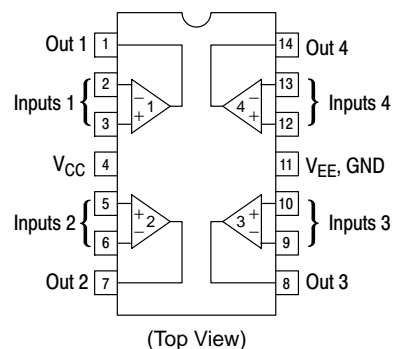
<http://onsemi.com>

### MARKING DIAGRAMS



LMxxxx = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y, YY = Year  
WW = Work Week  
G = Pb-Free Package

### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

## LM324S, LM2902S

### MAXIMUM RATINGS (T<sub>A</sub> = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	Single Supply	V <sub>CC</sub>	32
	Split Supplies	V <sub>CC</sub> , V <sub>EE</sub>	±16
Input Differential Voltage Range (Note 1)	V <sub>IDR</sub>	±32	Vdc
Input Common Mode Voltage Range (Note 2)	V <sub>ICR</sub>	-0.3 to 32	Vdc
Output Short Circuit Duration	t <sub>SC</sub>	Continuous	
Junction Temperature	T <sub>J</sub>	150	°C
Thermal Resistance, Junction-to-Air (Note 3)	Case 646	R <sub>θJA</sub>	118 °C/W
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C
Operating Ambient Temperature Range	T <sub>A</sub>		°C
		LM324S	0 to +70
		LM2902S	-40 to +105

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Split Power Supplies.
2. For supply voltages less than 32 V, the absolute maximum input voltage is equal to the supply voltage.
3. All R<sub>θJA</sub> measurements made on evaluation board with 1 oz. copper traces of minimum pad size. All device outputs were active.

# LM324S, LM2902S

## ELECTRICAL CHARACTERISTICS ( $V_{CC} = 5.0\text{ V}$ , $V_{EE} = \text{GND}$ , $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

Characteristics	Symbol	LM324S			LM2902S			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage $V_{CC} = 5.0\text{ V}$ to $30\text{ V}$ , $V_{ICR} = 0\text{ V}$ to $V_{CC} - 1.7\text{ V}$ , $V_O = 1.4\text{ V}$ , $R_S = 0\ \Omega$ $T_A = 25^\circ\text{C}$ $T_A = T_{\text{high}}$ (Note 4) $T_A = T_{\text{low}}$ (Note 4)	$V_{IO}$	-	2.0	7.0	-	2.0	7.0	mV
Average Temperature Coefficient of Input Offset Voltage $T_A = T_{\text{high}}$ to $T_{\text{low}}$ (Notes 4 and 6)	$\Delta V_{IO}/\Delta T$	-	7.0	-	-	7.0	-	$\mu\text{V}/^\circ\text{C}$
Input Offset Current $T_A = T_{\text{high}}$ to $T_{\text{low}}$ (Note 4)	$I_{IO}$	-	5.0	50	-	5.0	50	nA
Average Temperature Coefficient of Input Offset Current $T_A = T_{\text{high}}$ to $T_{\text{low}}$ (Notes 4 and 6)	$\Delta I_{IO}/\Delta T$	-	10	-	-	10	-	$\text{pA}/^\circ\text{C}$
Input Bias Current $T_A = T_{\text{high}}$ to $T_{\text{low}}$ (Note 4)	$I_{IB}$	-	-90	-250	-	-90	-250	nA
Input Common Mode Voltage Range (Note 5) $V_{CC} = 30\text{ V}$ $T_A = +25^\circ\text{C}$ $T_A = T_{\text{high}}$ to $T_{\text{low}}$ (Note 4)	$V_{ICR}$	0	-	28.3	0	-	28.3	V
Differential Input Voltage Range	$V_{IDR}$	-	-	$V_{CC}$	-	-	$V_{CC}$	V
Large Signal Open Loop Voltage Gain $R_L = 2.0\text{ k}\Omega$ , $V_{CC} = 15\text{ V}$ , for Large $V_O$ Swing $T_A = T_{\text{high}}$ to $T_{\text{low}}$ (Note 4)	$A_{VOL}$	25	100	-	25	100	-	V/mV
Channel Separation 10 kHz $\leq f \leq 20\text{ kHz}$ , Input Referenced	CS	-	-120	-	-	-120	-	dB
Common Mode Rejection, $R_S \leq 10\text{ k}\Omega$	CMR	65	70	-	50	70	-	dB
Power Supply Rejection	PSR	65	100	-	50	100	-	dB

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. LM324S:  $T_{\text{low}} = 0^\circ\text{C}$ ,  $T_{\text{high}} = +70^\circ\text{C}$

LM2902S:  $T_{\text{low}} = -40^\circ\text{C}$ ,  $T_{\text{high}} = +105^\circ\text{C}$

5. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common mode voltage range is  $V_{CC} - 1.7\text{ V}$ , but either or both inputs can go to +32 V without damage, independent of the magnitude of  $V_{CC}$ .

6. Guaranteed by design.

# LM324S, LM2902S

**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5.0\text{ V}$ ,  $V_{EE} = \text{GND}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

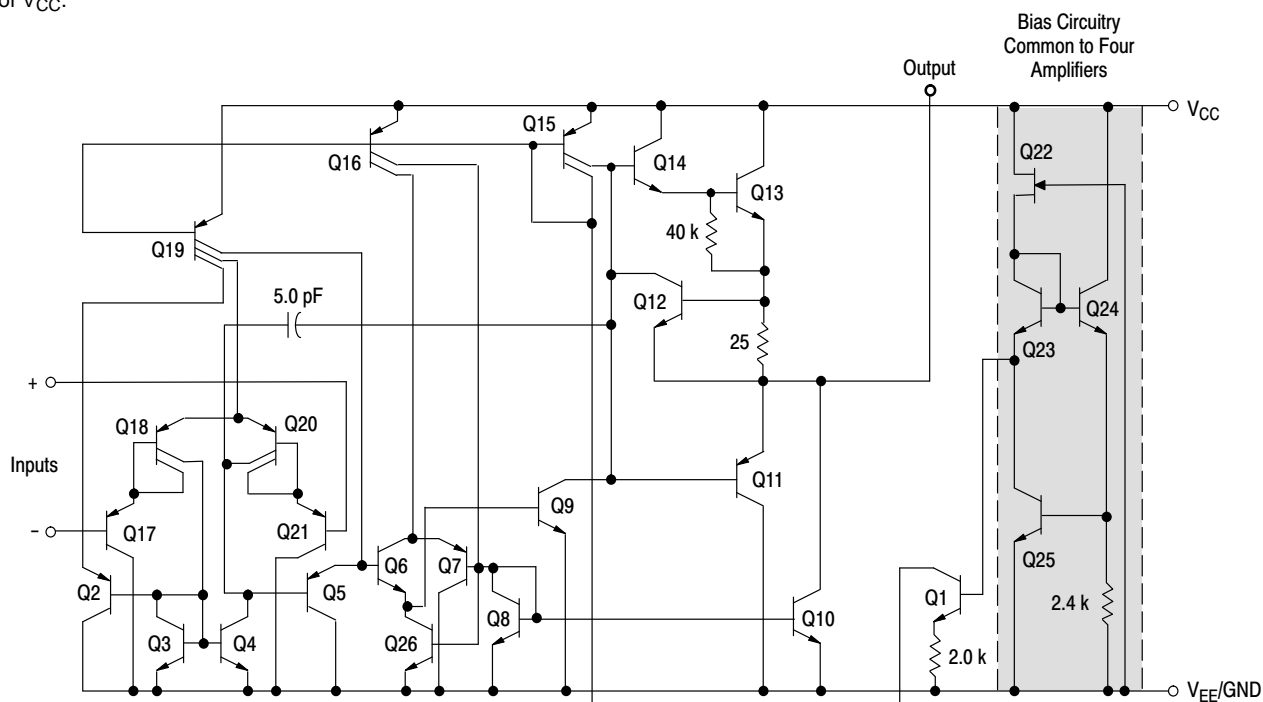
Characteristics	Symbol	LM324S			LM2902S			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage – High Limit $V_{CC} = 5.0\text{ V}$ , $R_L = 2.0\text{ k}\Omega$ , $T_A = 25^\circ\text{C}$ $V_{CC} = 30\text{ V}$ , $R_L = 2.0\text{ k}\Omega$ , ( $T_A = T_{\text{high}}$ to $T_{\text{low}}$ ) (Note 7) $V_{CC} = 30\text{ V}$ , $R_L = 10\text{ k}\Omega$ , ( $T_A = T_{\text{high}}$ to $T_{\text{low}}$ ) (Note 7)	$V_{OH}$	3.3	3.5	–	3.3	3.5	–	V
Output Voltage – Low Limit, $V_{CC} = 5.0\text{ V}$ , $R_L = 10\text{ k}\Omega$ , $T_A = T_{\text{high}}$ to $T_{\text{low}}$ (Note 7)	$V_{OL}$	–	5.0	20	–	5.0	100	mV
Output Source Current ( $V_{ID} = +1.0\text{ V}$ , $V_{CC} = 15\text{ V}$ ) $T_A = 25^\circ\text{C}$ $T_A = T_{\text{high}}$ to $T_{\text{low}}$ (Note 7)	$I_{O+}$	20	40	–	20	40	–	mA
Output Sink Current $V_{ID} = -1.0\text{ V}$ , $V_{CC} = 15\text{ V}$ , $T_A = 25^\circ\text{C}$ $T_A = T_{\text{high}}$ to $T_{\text{low}}$ (Note 7) $V_{ID} = -1.0\text{ V}$ , $V_O = 200\text{ mV}$ , $T_A = 25^\circ\text{C}$	$I_{O-}$	10	20	–	10	20	–	mA
Output Short Circuit to Ground (Note 8)	$I_{SC}$	–	40	60	–	40	60	mA
Power Supply Current ( $T_A = T_{\text{high}}$ to $T_{\text{low}}$ ) (Note 7) $V_{CC} = 30\text{ V}$ , $V_O = 0\text{ V}$ , $R_L = \infty$ $V_{CC} = 5.0\text{ V}$ , $V_O = 0\text{ V}$ , $R_L = \infty$	$I_{CC}$	–	–	3.0	–	–	3.0	mA
		–	–	1.2	–	–	1.2	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. LM324S:  $T_{\text{low}} = 0^\circ\text{C}$ ,  $T_{\text{high}} = +70^\circ\text{C}$

LM2902S:  $T_{\text{low}} = -40^\circ\text{C}$ ,  $T_{\text{high}} = +105^\circ\text{C}$

8. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common mode voltage range is  $V_{CC} - 1.7\text{ V}$ , but either or both inputs can go to  $+32\text{ V}$  without damage, independent of the magnitude of  $V_{CC}$ .



**Figure 1. Representative Circuit Diagram**  
(One-Fourth of Circuit Shown)

# LM324S, LM2902S

## CIRCUIT DESCRIPTION

The LM324S and LM2902S are made using four internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q20 and Q18 with input buffer transistors Q21 and Q17 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance, a smaller compensation capacitor (only 5.0 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q20

and Q18. Another feature of this input stage is that the input common mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

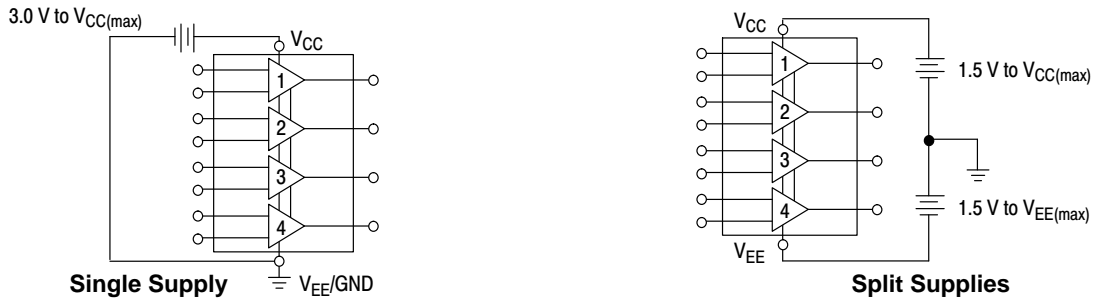


Figure 2.

# LM324S, LM2902S

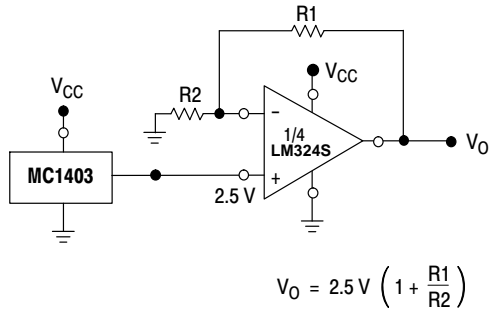


Figure 3. Voltage Reference

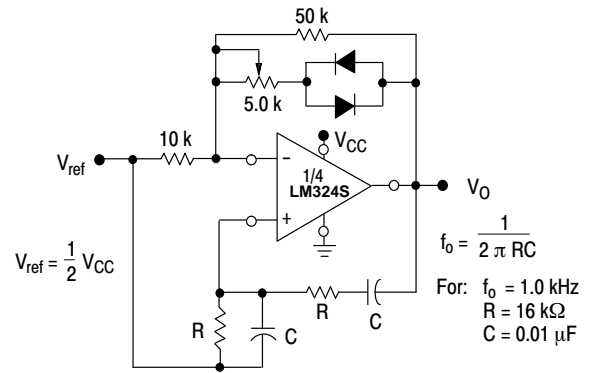


Figure 4. Wien Bridge Oscillator

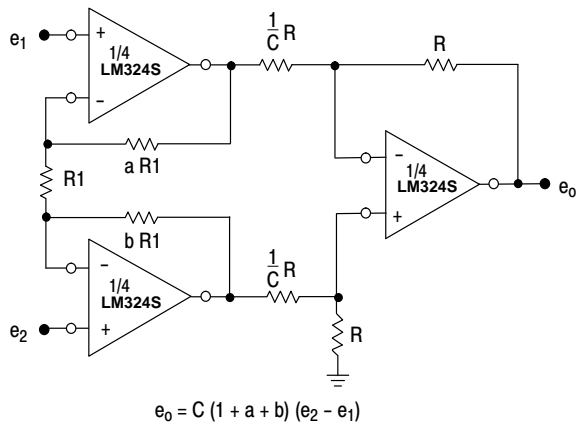


Figure 5. High Impedance Differential Amplifier

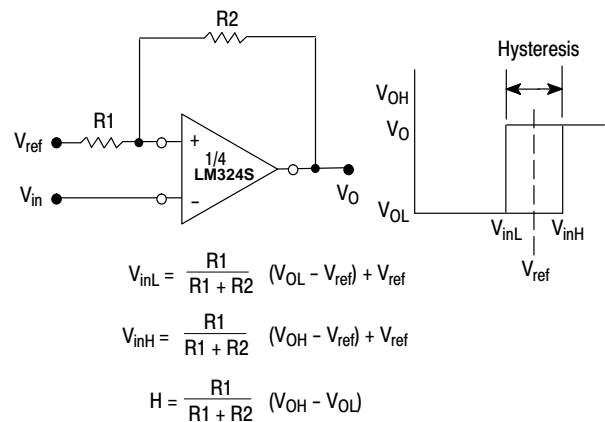


Figure 6. Comparator with Hysteresis

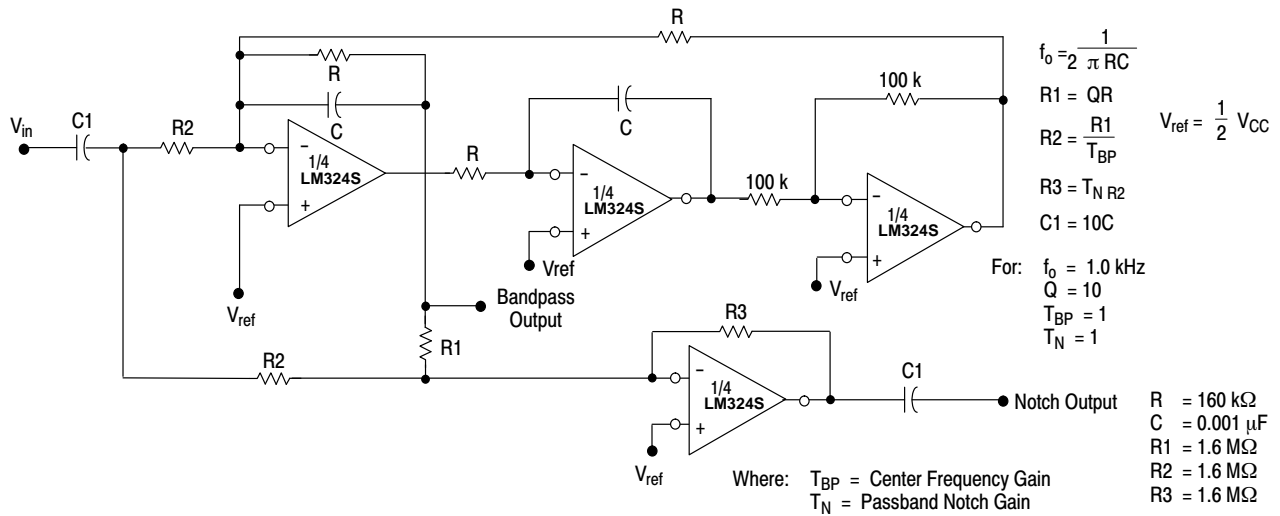
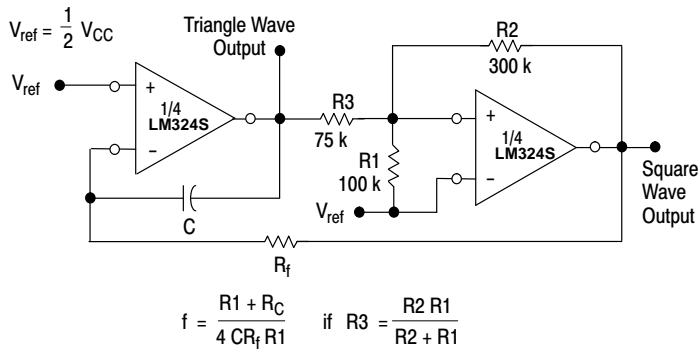
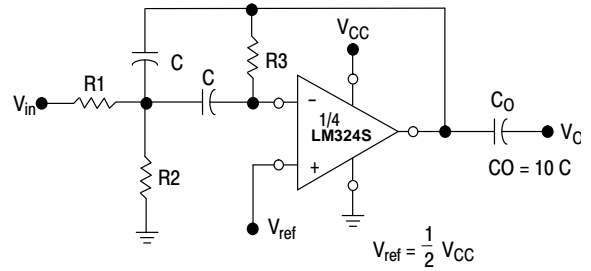


Figure 7. Bi-Quad Filter

## LM324S, LM2902S



**Figure 8. Function Generator**



**Figure 9. Multiple Feedback Bandpass Filter**

Given:  $f_o$  = center frequency  
 $A(f_o)$  = gain at center frequency

Choose value  $f_o, C$

$$\text{Then: } R3 = \frac{Q}{\pi f_o C}$$

$$R1 = \frac{R3}{2 A(f_o)}$$

$$R2 = \frac{R1 R3}{4Q^2 R1 - R3}$$

For less than 10% error from operational amplifier,  $\frac{Q_o f_o}{BW} < 0.1$

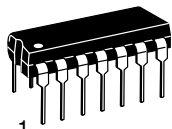
where  $f_o$  and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

### ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping†
LM324SNG	0°C to +70°C	PDIP-14 (Pb-Free)	25 Units / Rail
LM2902SNG	-40°C to +105°C	PDIP-14 (Pb-Free)	25 Units / Rail

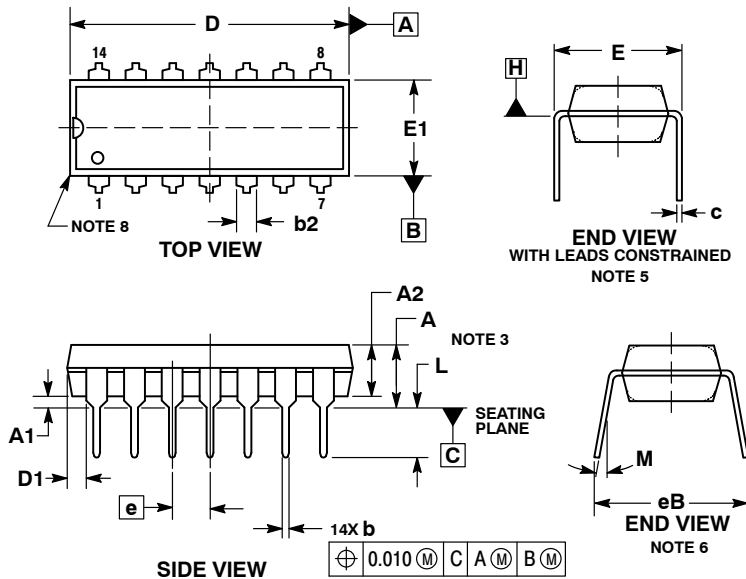
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



1  
SCALE 1:1

PDIP-14  
CASE 646-06  
ISSUE 5

DATE 22 APR 2015

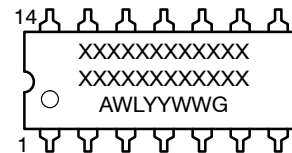


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.210	---	5.33
A1	0.015	---	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP	---	1.52 TYP	---
C	0.008	0.014	0.20	0.36
D	0.735	0.775	18.67	19.69
D1	0.005	---	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC	---	2.54 BSC	---
eB	---	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	---	10°	---	10°

GENERIC  
MARKING DIAGRAM\*



- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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**PDIP-14**  
**CASE 646-06**  
**ISSUE S**

DATE 22 APR 2015

STYLE 1:  
 PIN 1. COLLECTOR  
 2. BASE  
 3. EMITTER  
 4. NO  
 CONNECTION  
 5. EMITTER  
 6. BASE  
 7. COLLECTOR  
 8. COLLECTOR  
 9. BASE  
 10. EMITTER  
 11. NO  
 CONNECTION  
 12. EMITTER  
 13. BASE  
 14. COLLECTOR

STYLE 2:  
 CANCELLED

STYLE 3:  
 CANCELLED

STYLE 4:  
 PIN 1. DRAIN  
 2. SOURCE  
 3. GATE  
 4. NO  
 CONNECTION  
 5. GATE  
 6. SOURCE  
 7. DRAIN  
 8. DRAIN  
 9. SOURCE  
 10. GATE  
 11. NO  
 CONNECTION  
 12. GATE  
 13. SOURCE  
 14. DRAIN

STYLE 5:  
 PIN 1. GATE  
 2. DRAIN  
 3. SOURCE  
 4. NO CONNECTION  
 5. SOURCE  
 6. DRAIN  
 7. GATE  
 8. GATE  
 9. DRAIN  
 10. SOURCE  
 11. NO CONNECTION  
 12. SOURCE  
 13. DRAIN  
 14. GATE

STYLE 6:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. NO CONNECTION  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 7:  
 PIN 1. NO CONNECTION  
 2. ANODE  
 3. ANODE  
 4. NO CONNECTION  
 5. ANODE  
 6. NO CONNECTION  
 7. ANODE  
 8. ANODE  
 9. ANODE  
 10. NO CONNECTION  
 11. ANODE  
 12. ANODE  
 13. NO CONNECTION  
 14. COMMON  
 CATHODE

STYLE 8:  
 PIN 1. NO CONNECTION  
 2. CATHODE  
 3. CATHODE  
 4. NO CONNECTION  
 5. CATHODE  
 6. NO CONNECTION  
 7. CATHODE  
 8. CATHODE  
 9. CATHODE  
 10. NO CONNECTION  
 11. CATHODE  
 12. CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 9:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. COMMON ANODE  
 8. COMMON ANODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. NO CONNECTION  
 12. ANODE/CATHODE  
 13. ANODE/CATHODE  
 14. COMMON CATHODE

STYLE 10:  
 PIN 1. COMMON  
 CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. COMMON ANODE  
 8. COMMON  
 CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 11:  
 PIN 1. CATHODE  
 2. CATHODE  
 3. CATHODE  
 4. CATHODE  
 5. CATHODE  
 6. CATHODE  
 7. CATHODE  
 8. ANODE  
 9. ANODE  
 10. ANODE  
 11. ANODE  
 12. ANODE  
 13. ANODE  
 14. ANODE

STYLE 12:  
 PIN 1. COMMON CATHODE  
 2. COMMON ANODE  
 3. ANODE/CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. COMMON ANODE  
 7. COMMON CATHODE  
 8. ANODE/CATHODE  
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