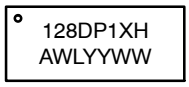
# OIS & Open-AF Control LSI

# LC898128DP

**WLCSP30**
**CASE 567WE**

## MARKING DIAGRAM




A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| LC898128DP1XHTBG | WLCSP30 (Pb−Free) | 4,000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.



### Overview

This is a system LSI integrating an on−chip 32bit DSP, a FLASH ROM and peripherals including analog circuits for OIS (Optical Image Stabilization) / Open−AF (Auto Focus) control, constant current drivers.

### Features

- On−chip 32bit DSP
  - Built−in Software for Digital Servo Filter
  - Built−in Software for Gyro Filter
- Memory
  - 40 kB Flash Memory
  - Program ROM
  - Program SRAM
  - Data SRAM
- Peripherals
  - AD Converter
  - DA Converter
  - 2−wire Serial I/F Circuit
    (The Communication Protocol is Compatible with $I^2C$)
  - Hall Bias Circuit
  - Hal Amp
  - OSC (Oscillator)
  - LDO (Low Drop−Out Regulator)
  - Temperature Sensor
  - Digital Gyro I/F (SPI)
  - Interrupt I/F
- Driver
  - OIS:
    Constant Current Linear Driver (x2ch, $I_{full}$ = 200 mA)
  - OP−AF (Bi−direction):
    Constant Current Linear Driver (x1ch, $I_{full}$ = 130 mA)
- Package
  - WLCSP30 (4.300 mm x 1.175 mm) Thickness Max. 0.35 mm, with Back Coat
  - Ball 3 x 10
  - Pitch 0.4 mm
  - Lead−Free
  - Halogen Free
- Power Supply Voltage
  - AD/DA/VGA/LDO/OSC/Flash/:
    AVDD30 = 2.7 V to 3.3 V
  - Driver: VM1,2 = 1.8 V to 3.3 V
  - 1.8 V I/O: IOVDD = 1.7 V to 3.3 V
  - Core Logic: Generated by On−chip LDO
    Connect 1 μF Capacitor to LDPO Pin

## BLOCK DIAGRAM

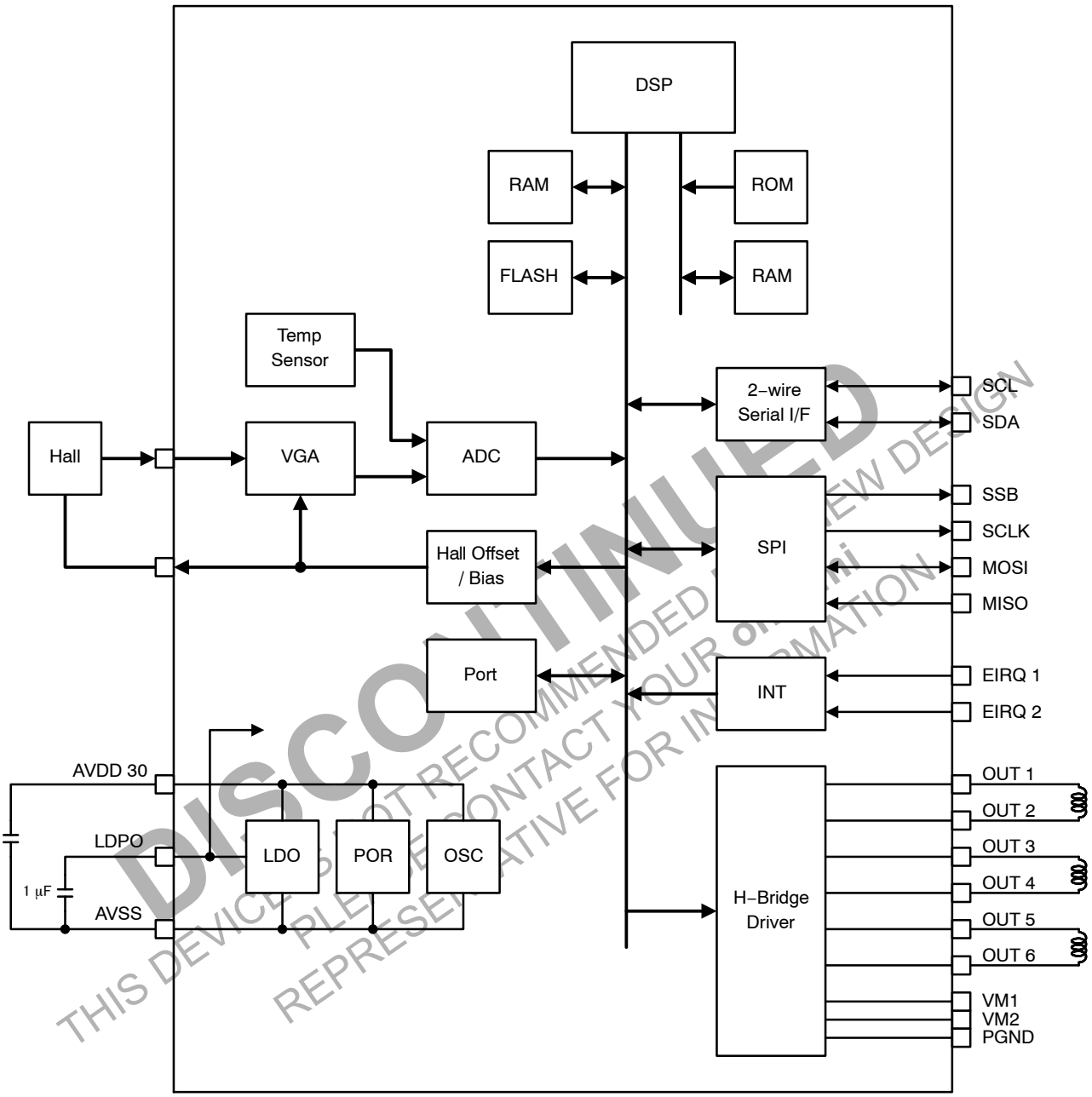





**Figure 1. Block Diagram**

## PIN LAYOUT

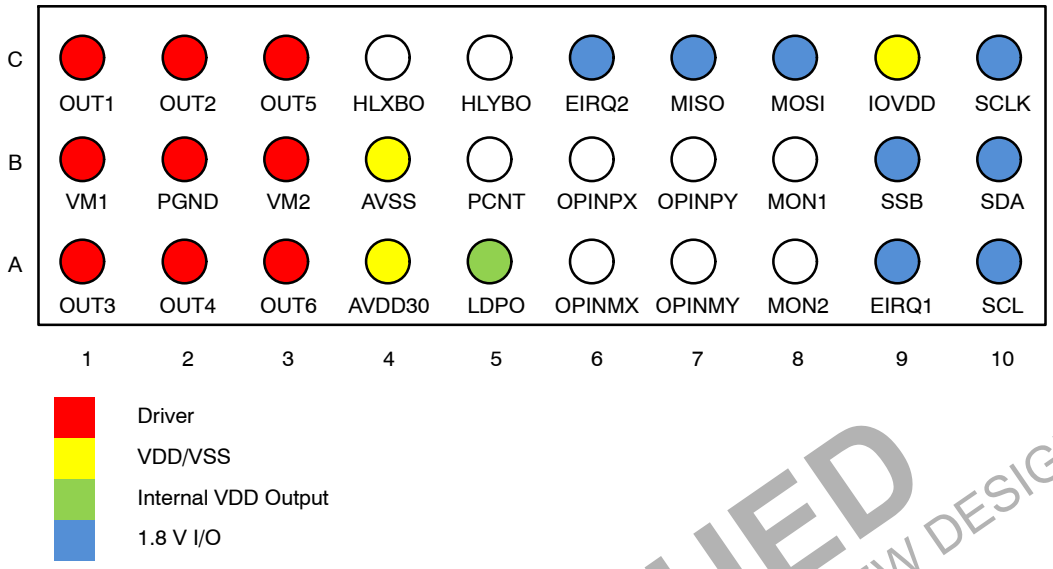



**Figure 2. Pin Layout (Bottom View)**



## PIN DESCRIPTION

**PIN DESCRIPTION**

| No. | Pin | I/O | I/O Pwr | Primary Function | Sub Functions | Init |
|---|---|---|---|---|---|---|
| 1 | MON1 | B | AVDD30 | Servo Monitor Analog In/Out | 2−wire serial Monitor Data | Z |
| 2 | MON2 | B | AVDD30 | Servo Monitor Analog In/Out | 2−wire serial Monitor Clock | Z |
| 3 | SCL | B | IOVDD | 2−wire serial HOST I/F Clock Slave | | Z |
| 4 | SDA | B | IOVDD | 2−wire serial HOST I/F Data Slave | | Z |
| 5 | IOVDD | P | | I/O Power (1.7 V to 3.3 V) | | − |
| 6 | SSB | B | IOVDD | Digital Gyro Data I/F Chip Select Out (3/4−wire Master) | Digital Gyro Data I/F Chip Select In (3/4−wire Slave) | Z |
| 7 | SCLK | B | IOVDD | Digital Gyro Data I/F Clock Out (3/4−wire Master) | Digital Gyro Data I/F Clock In (3/4−wire Slave)<br>2−wire serial Sensor Hub I/F Clock Slave | Z |
| 8 | MOSI | B | IOVDD | Digital Gyro Data I/F Data InOut (3−wire Master)<br>Digital Gyro Data I/F Data Out (4−wire Master) | Digital Gyro Data I/F Data InOut (3wire Slave)<br>Digital Gyro Data I/F Data In (4−wire Slave)<br>2−wire serial Sensor Hub I/F Data Slave | Z |
| 9 | MISO | B | IOVDD | Digital Gyro Data I/F Data In (4−wire Master)<br>Digital Gyro Data I/F Chip Select 2 Out (3−wire Master) | Digital Gyro Data I/F Data Out (4−wire Slave) | U |
| 10 | EIRQ1 | B | IOVDD | Interrupt Input 1 | | Z |
| 11 | EIRQ2 | B | IOVDD | Interrupt Input 2 | | Z |

**PIN DESCRIPTION** (continued)

| No. | Pin | I/O | I/O Pwr | Primary Function | Sub Functions | Init |
|---|---|---|---|---|---|---|
| 12 | PCNT | O | AVDD30 | No use | | Z |
| 13 | HLXBO | O | AVDD30 | OIS Hall X Bias Output | | Z |
| 14 | HLYBO | O | AVDD30 | OIS Hall Y Bias Output | | Z |
| 15 | OPINMX | I | AVDD30 | OIS Hall X Opamp Input Minus | | – |
| 16 | OPINPX | I | AVDD30 | OIS Hall X Opamp Input Plus | | – |
| 17 | OPINMY | I | AVDD30 | OIS Hall Y Opamp Input Minus | | – |
| 18 | OPINPY | I | AVDD30 | OIS Hall Y Opamp Input Plus | | – |
| 19 | OUT1 | O | VM1 | OIS Driver Output | | Z |
| 20 | OUT2 | O | VM1 | OIS Driver Output | | Z |
| 21 | OUT3 | O | VM1 | OIS Driver Output | | Z |
| 22 | OUT4 | O | VM1 | OIS Driver Output | | Z |
| 23 | OUT5 | O | VM2 | OP−AF Driver Output | | Z |
| 24 | OUT6 | O | VM2 | OP−AF Driver Output | | Z |
| 25 | AVDD30 | P | | Analog Power (2.7 V to 3.3 V) | | – |
| 26 | AVSS | P | | Analog GND | | – |
| 27 | VM1 | P | | OIS Driver Power (1.8 V to 3.3 V) | | – |
| 28 | VM2 | P | | OP−AF Driver Power (1.8 V to 3.3 V) | | – |
| 29 | PGND | P | | Driver GND | | – |
| 30 | LDPO | P | | Internal 1.38 V LDO Power Output | | – |

*Process when pins are not used

- PIN TYPE “O” – Ensure that it is set to OPEN.
- PIN TYPE “I” – OPEN is inhibited. Ensure that it is connected to the $V_{DD}$ or $V_{SS}$ even when it is unused. (Please contact **onsemi** for more information about selection of $V_{DD}$ or $V_{SS}$.)
- PIN TYPE “B” – If you are unsure about processing method on the pin description of pin layout table, please contact us.

Note that incorrect processing of unused pins may result in defects.

## ELECTRICAL CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS (AVSS = 0 V, PGND = 0 V)

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Power Supply Voltage | $V_{AD}30$ max | $T_A \le 25°C$ | −0.3 to 4.6 | V |
| | $V_M$ max | $T_A \le 25°C$ | −0.3 to 4.6 | V |
| | $V_{IO}$ max | $T_A \le 25°C$ | −0.3 to 4.6 | V |
| Input/Output Voltage | $V_{AI}30$, $V_{AO}30$ | $T_A \le 25°C$ | −0.3 to $V_{AD}30$ + 0.3 | V |
| | $V_{MI}30$, $V_{MO}30$ | $T_A \le 25°C$ | −0.3 to $V_M30$ + 0.3 | V |
| | $V_{II}$, $V_{IOO}$ | $T_A \le 25°C$ | −0.3 to $V_{IO}18$ + 0.3 | V |
| Storage Temperature | $T_{stg}$ | | −55 to 125 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### ALLOWABLE OPERATING RATINGS ($T_A$ = −30 to 85°C, AVSS = 0 V, PGND = 0 V)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **3.0 V POWER SUPPLY (AVDD30)** | | | | | |
| Power Supply Voltage | $V_{AD}30$ | 2.7 | 2.8 | 3.3 | V |
| Input Voltage Range | $V_{INA}$ | 0 | – | $V_{AD}30$ | V |
| **3.0 V POWER SUPPLY (VM1, VM2)** | | | | | |
| Power Supply Voltage | $V_M30$ | 1.8 (Note 1) | 2.8 | the lower of 3.3 and AVDD30 + 0.5 | V |
| Input Voltage Range | $V_{INM}$ | 0 | – | $V_M30$ | V |
| **1.8 V POWER SUPPLY (IOVDD)** | | | | | |
| Power Supply Voltage | $V_{IO}$ | 1.7 | 1.8 | 3.3 | V |
| Input Voltage Range | $V_{INI}$ | 0 | – | $V_{IO}$ | V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Constant current.



### DC CHARACTERISTICS: INPUT/OUTPUT

($T_A$ = −30 to 85°C, AVSS = 0 V, PGND = 0 V, AVDD30 = 2.7 to 3.3 V, IOVDD = 1.7 to 3.3 V)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit | Applicable Pins |
|---|---|---|---|---|---|---|---|
| High−level Input Voltage | $V_{IH}$ | CMOS Schmitt | 0.7 IOVDD | | | V | SCL, SDA, SSB, SCLK, MOSI, MISO, EIRQ1, EIRQ2 |
| Low−level Input Voltage | $V_{IL}$ | | | | 0.3 IOVDD | V | |
| High−level Input Voltage | $V_{IH}$ | CMOS Schmitt | 0.7 AVDD30 | | | V | MON1, MON2 |
| Low−level Input Voltage | $V_{IL}$ | | | | 0.3 AVDD30 | V | MON1, MON2 |
| High−level Output Voltage | $V_{OH}$ | $I_{OH}$ = −3 mA | IOVDD − 0.2 | | | V | SDA, SSB, SCLK, MOSI, MISO, EIRQ1, EIRQ2 |
| Low−level Output Voltage | $V_{OL}$ | $I_{OL}$ = 3 mA | | | 0.2 | V | SCL, SDA, SSB, SCLK, MOSI, MISO, EIRQ1, EIRQ2 |
| High−level Output Voltage | $V_{OH}$ | $I_{OH}$ = −2 mA | AVDD30 − 0.2 | | | V | MON1, MON2 |
| Low−level Output Voltage | $V_{OL}$ | $I_{OL}$ = 2 mA | | | 0.2 | V | MON1, MON2 |

**DC CHARACTERISTICS: INPUT/OUTPUT** (continued)
($T_A$ = −30 to 85°C, AVSS = 0 V, PGND = 0 V, AVDD30 = 2.7 to 3.3 V, IOVDD = 1.7 to 3.3 V)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit | Applicable Pins |
|---|---|---|---|---|---|---|---|
| Analog Input Voltage | $V_{AI}$ | | AVSS | | AVDD30 | V | MON1, MON2, OPINPX, OPINMX, OPINPY, OPINMY |
| Pull Up Resistor | $R_{up}$ | | 20 | | 250 | kΩ | SSB, SCLK, MOSI, MISO, EIRQ1, EIRQ2, MON1, MON2 |
| Pull Down Resistor | $R_{dn}$ | | 20 | | 250 | kΩ | |

**DRIVER OUTPUT**
($T_A$ = 25°C, $V_{SS}$ = 0 V, PGND = 0 V, AVDD30 = VM1,2 = 2.8 V)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Current, OUT1−OUT4 | $I_{full}$ | Full code | 190 | 200 | 210 | mA |
| Output Current, OUT5, OUT6 | | Full code<br>OP−AF (bi−direction) | 123.5 | 130 | 136.5 | mA |

**NON−VOLATILE MEMORY CHARACTERISTICS**

| Parameter | Symbol | Conditions | Value | Unit |
|---|---|---|---|---|
| Operating Temperature | $T_{opr1}$ | Read for FLASH | −30 to 85 | °C |
| | $T_{opr2}$ | Program & Erase for FLASH | −10 to 65 (Note 2) | °C |

2. All drivers must be in the standby state.

| Item | Symbol | Conditions | Min | Typ | Max | Unit | Applicable Circuit |
|---|---|---|---|---|---|---|---|
| Endurance | EN | | − | − | 1000 | Cycles | Flash Memory |
| Data Retention | RT | | 10 | − | − | Years | |
| Write Time | $t_{WT}$ | | − | − | 3 | ms | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## AC CHARACTERISTICS

### Power Supply Timing

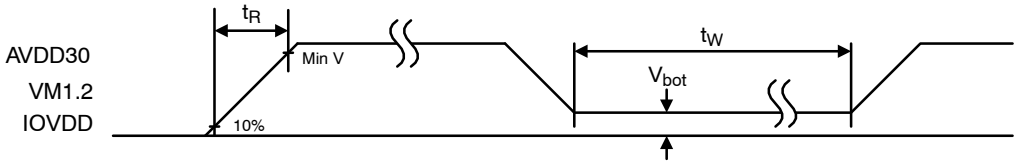



**Figure 3. $V_{DD}$ Supply Timing**

**Table 1.**

| Item | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Rise Time | $t_R$ | – | – | 3 | ms |
| Wait Time | $t_W$ | 100 | – | – | ms |
| Bottom Voltage | $V_{bot}$ | – | – | 0.2 | V |

Injection order between AVDD30, VM1,2 and IOVDD is below.

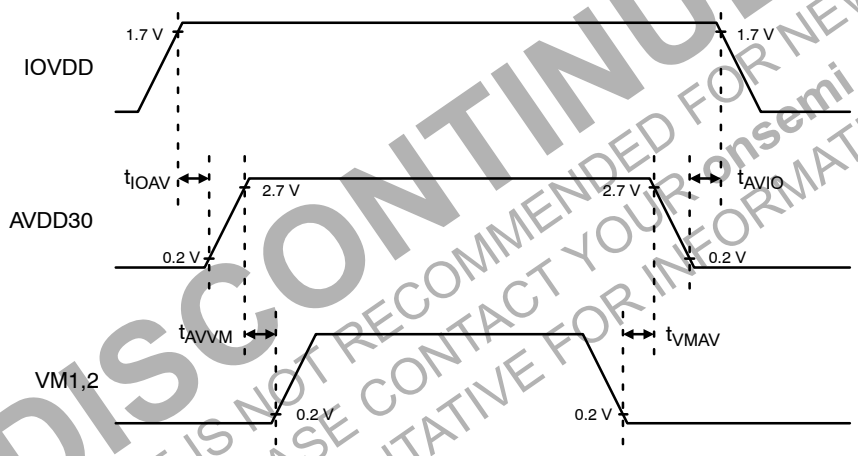



**Figure 4. Injection Order between AVDD30, VM1,2 and IOVDD**

**Table 2.**

| Item | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| IOVDD On to AVDD30 ON | $t_{IOAV}$ | 0 | – | – | ms |
| AVDD30 ON to VM1,2 ON | $t_{AVVM}$ | 0 | – | – | ms |
| VM1,2 OFF to AVDD30 OFF | $t_{VMAV}$ | 0 | – | – | ms |
| AVDD30 OFF to IOVDD OFF | $t_{AVIO}$ | 0 | – | * | ms |

*Please make IOPRSTB (D0_0064h, bit0) = 0 before turning OFF AVDD when AVDD is turned off with keeping IOVDD on.

NOTES:

- VM1, VM2 ≤ AVDD30 + 0.5 V
- Power ON/OFF of VM1 and VM2, is possible individually.

SDA, SCL, SSB, SCLK, MOSI, MISO, EIRQ1 and EIRQ2 tolerate 3 V input at the time of power off.

The data in the Flash memory may be rewritten unintentionally if you do not keep specifications.

And it is forbidden to power off during Flash memory access. The data in the Flash memory may be rewritten unintentionally.

OIS driver is recommended to set standby before VM1 power off.
AF driver is recommended to set standby before VM2 power off.

### 2−wire Serial Interface Timing

The 2−wire serial interface timing definition and electric characteristics are shown below. The communication protocol is compatible with $I^2C$. This circuit has clock stretch function.

Static Address: 7'b0100100

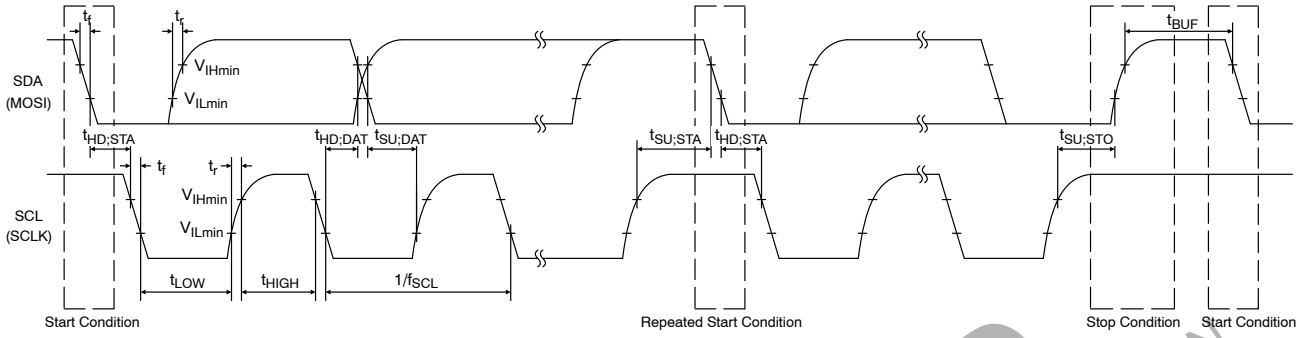



**Figure 5. 2−wire Serial Interface Timing**



**Table 3.**

| Item | Symbol | Standard−mode | | Fast−mode | | Fast−mode Plus | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| SCL Clock Frequency | $f_{SCL}$ | − | 100 | − | 400 | − | 1000 | kHz |
| START Condition Hold Time | $t_{HD;STA}$ | 4.0 | − | 0.6 | − | 0.26 | − | μs |
| SCL Clock Low Period | $t_{LOW}$ | 4.7 | − | 1.3 | − | 0.5 | − | μs |
| SCL Clock High Period | $t_{HIGH}$ | 4.0 | − | 0.6 | − | 0.26 | − | μs |
| Setup Time for Repetition START Condition | $t_{SU;STA}$ | 4.7 | − | 0.6 | − | 0.26 | − | μs |
| Data Hold Time | $t_{HD;DAT}$ | 0 (Note 3) | 3.45 | 0 (Note 3) | 0.9 | 0 (Note 3) | 0.45 | μs |
| Data Setup Time | $t_{SU;DAT}$ | 250 | − | 100 | − | 50 | − | ns |
| SDA, SCL Rising Time | $t_r$ | − | 1000 | − | 300 | − | 120 | ns |
| SDA, SCL Falling Time | $t_f$ | − | 300 | − | 300 | − | 120 | ns |
| STOP Condition Setup Time | $t_{SU;STO}$ | 4.0 | − | 0.6 | − | 0.26 | − | μs |
| Bus Free Time between STOP and START | $t_{BUF}$ | 4.7 | − | 1.3 | − | 0.5 | − | μs |

3. Although the $I^2C$ specification defines a condition that 300 ns of hold time is required internally, this LSI is designed for a condition with typ. 40 ns of hold time. If SDA (MOSI) signal is unstable around falling point of SCL (SCLK) signal, please implement an appropriate treatment on board, such as inserting a resister.

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT**: www.onsemi.com/support
**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales