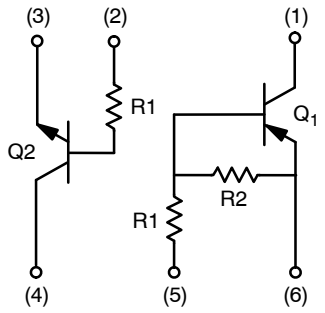
Dual Bias Resistor Transistor

NPN and PNP Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

IMD10AMT1G

- High Current: I_C = 500 mA max
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant



SC−74

MARKING DIAGRAM

D10 = Specific Device Code
M = Date Code
▪ = Pb−Free Package

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Value	Unit
Collector−Base Voltage	$V_{(BR)CBO}$	50	Vdc
Collector−Emitter Voltage	$V_{(BR)CEO}$	50	Vdc
Emitter−Base Voltage	$V_{(BR)EBO}$	5.0	Vdc
Collector Current − Continuous	I_C	500	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Power Dissipation*	P_D	285	mW
Junction Temperature	T_J	150	°C
Storage Temperature	T_{stg}	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*Total for both Transistors.

ORDERING INFORMATION

Device	Package	Shipping†
IMD10AMT1G	SC−74R (Pb−Free)	3000 / Tape & Reel
NSVIMD10AMT1G	SC−74R (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted, common for Q_1 and Q_2, – minus sign for Q_1(PNP) omitted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Base Breakdown Voltage (I_C = 50 μAdc, I_E = 0 A)	$V_{(BR)CBO}$	50	–	Vdc
Collector–Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0 A)	$V_{(BR)CEO}$	50	–	Vdc
Emitter–Base Breakdown Voltage (I_E = 50 μAdc, I_C = 0 A)	$V_{(BR)EBO}$	5.0	–	Vdc
Collector–Base Cutoff Current (V_{CB} = 50 Vdc, I_E = 0 A)	I_{CBO}	–	100	nA
Emitter–Base Cutoff Current Q1 (PNP) (V_{EB} = 6.0 Vdc, I_C = 0 A) Q2 (NPN)	I_{EBO}	– –	1.0 0.5	mA
Collector–Emitter Cutoff Current (V_{CE} = 25 Vdc, I_B = 0 A)	I_{CES}	–	100	nA
ON CHARACTERISTICS (Note 1)				
DC Current Gain (V_{CE} = 5.0 V, I_C = 100 mA) Q1(PNP) (V_{CE} = 5.0 V, I_C = 1.0 mA) Q2(NPN)	h_{FE}	 68 100	 – 600	
Collector–Emitter Saturation Voltage (I_C = 10 mA, I_B = 1.0 mA)	$V_{CE(sat)}$	–	0.3	Vdc
Output Voltage (on) (V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 kΩ)	V_{OL}	–	0.2	Vdc
Output Voltage (off) (V_{CC} = 5.0 V, V_B = 0.25 V, R_L = 1.0 kΩ)	V_{OH}	4.9	–	Vdc
Input Resistor Q1(PNP) Q2(NPN)	R1	 70 7.0	 130 13	 Ω kΩ
Resistor Ratio Q1(PNP) Q2(NPN)	R1/R2	 0.008 –	 0.012 –	

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle < 2.0%.

TYPICAL CHARACTERISTICS (NPN)

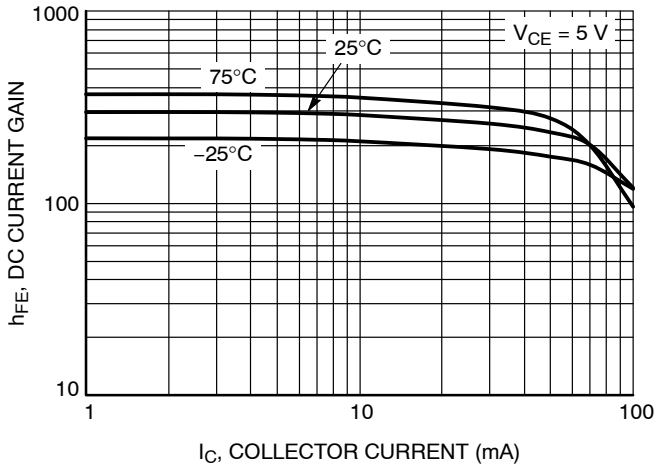


Figure 1. DC Current Gain

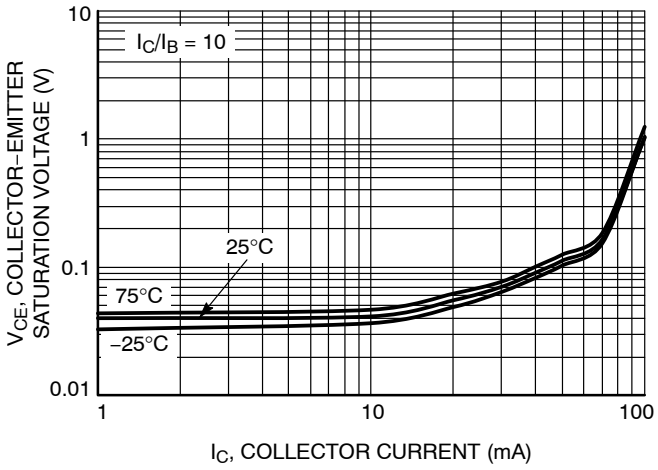


Figure 2. Collector−Emitter Saturation Voltage

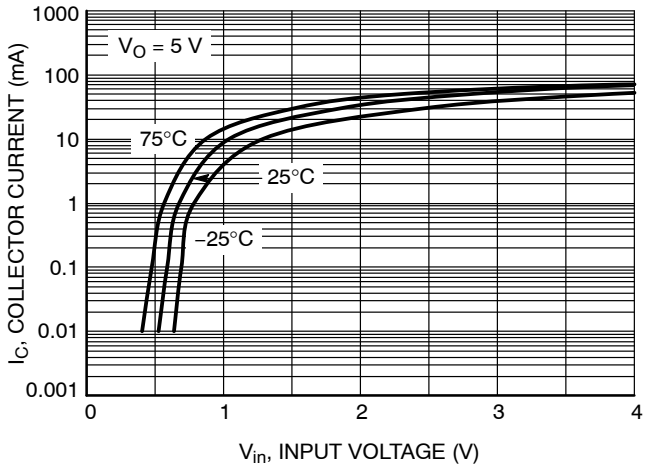


Figure 3. Output Current vs. Input Voltage

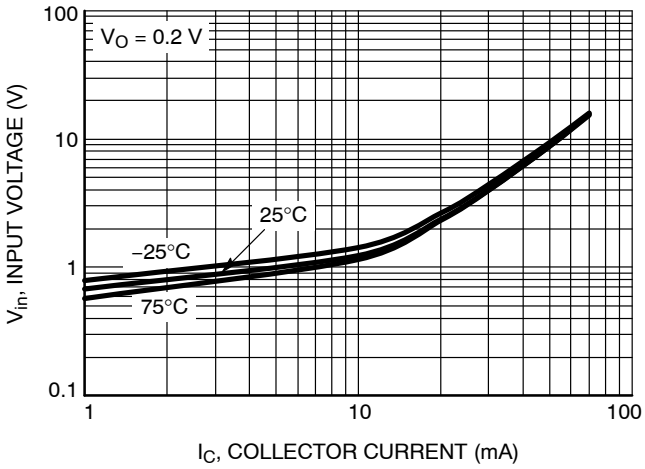


Figure 4. Input Voltage vs. Output Current

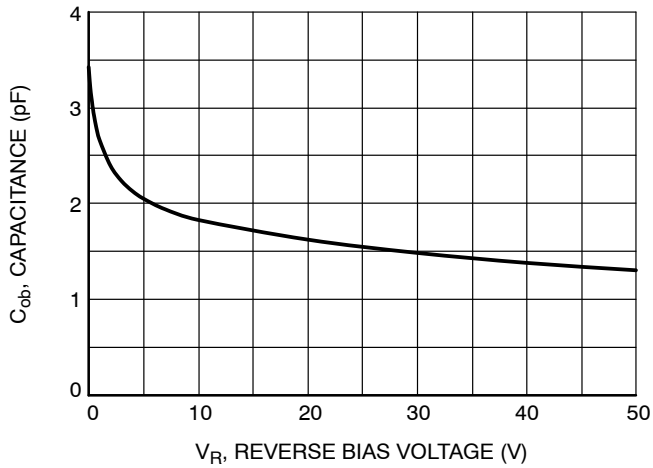


Figure 5. Output Capacitance

TYPICAL CHARACTERISTICS (PNP)

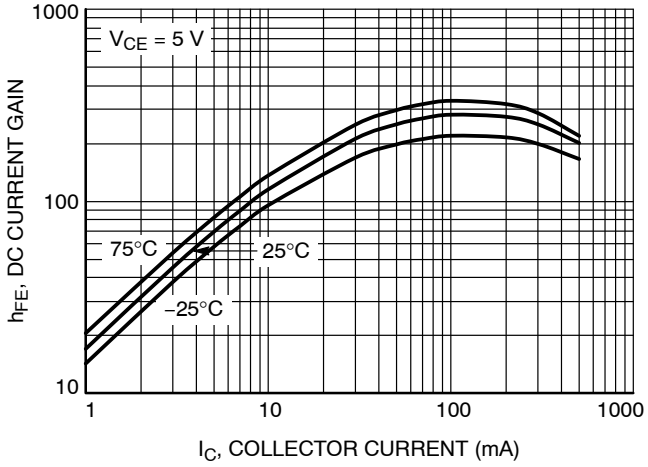


Figure 6. DC Current Gain

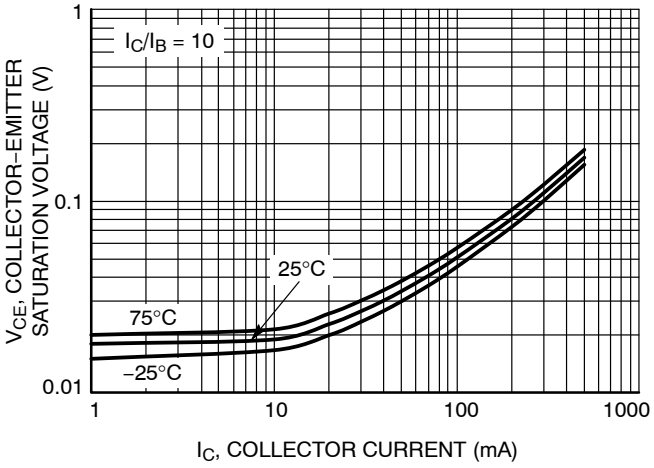


Figure 7. Collector−Emitter Saturation Voltage

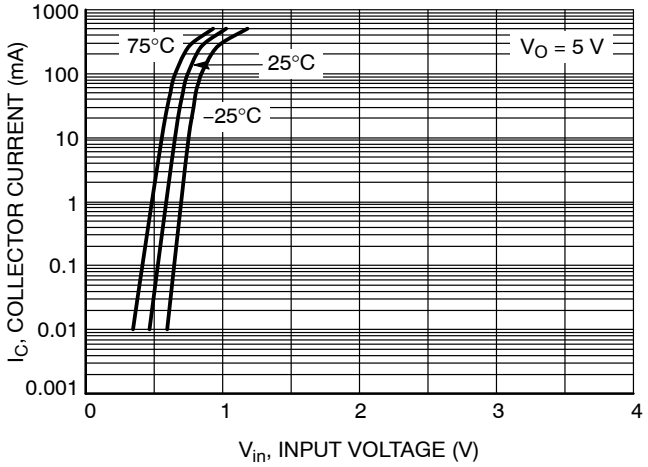


Figure 8. Output Current vs. Input Voltage

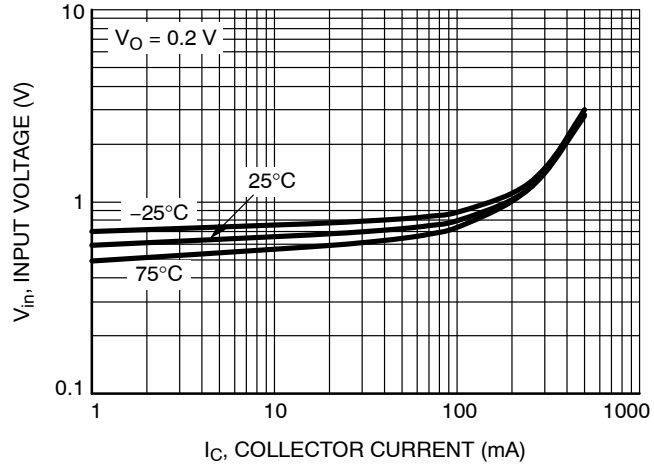


Figure 9. Input Voltage vs. Output Current

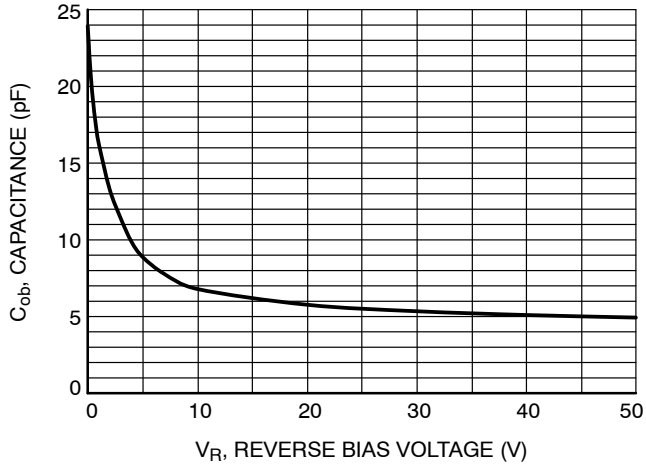
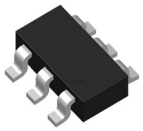
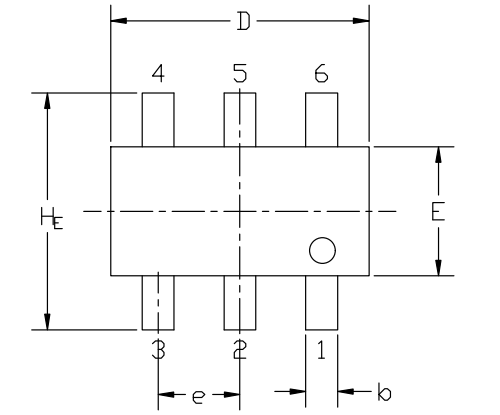


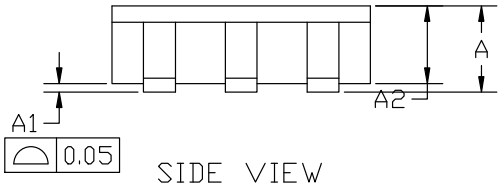
Figure 10. Output Capacitance

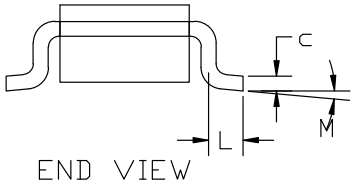


SC74−6 3.00x1.50x0.90, 0.95P
CASE 318AA
ISSUE C

DATE 22 AUG 2023



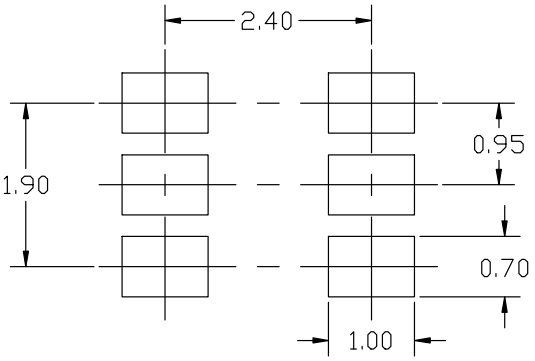




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

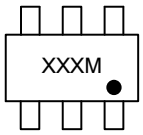
	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
A2	0.80	0.90	1.00
b	0.25	0.37	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
H_E	2.50	2.75	3.00
M	0°	–	10°



RECOMMENDED
MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 20:
PIN 1. COLLECTOR 1
2. BASE 2
3. EMITTER 2
4. COLLECTOR 2
5. BASE 1
6. EMITTER 1

STYLE 21:
PIN 1. COLLECTOR 1
2. EMITTER 2
3. BASE 2
4. COLLECTOR 2
5. EMITTER 1
6. BASE 1

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