

# **MOSFET – Power, N-Channel, UltraFET**

**75 V, 150 A, 0,016  $\Omega$**

## **HUFA75852G3-F085**

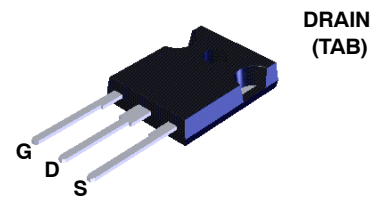
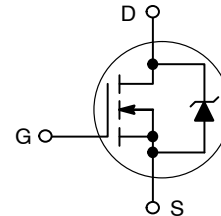
### **Features**

- Ultra Low On-Resistance
  - $R_{DS(ON)} = 0.016 \Omega$ ,  $V_{GS} = 10 V$
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- AEC-Q101 Qualified and PPAP Capable
- This Device is Pb-Free and is RoHS Compliant



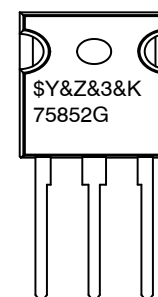
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**JEDEC TO-247  
CASE 340CK**

### **MARKING DIAGRAM**



\$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Data Code (Year & Week)
&K	= Lot
75852G	= Specific Device Code

### **ORDERING INFORMATION**

See detailed ordering and shipping information on page 2 of this data sheet.

# HUFA75852G3-F085

## ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25°C, Unless otherwise noted)

Symbol	Parameter		Value	Unit
V <sub>DSS</sub>	Drain to Source Voltage (Note 1)		150	V
V <sub>DGR</sub>	Gate to Gate Voltage (R <sub>GS</sub> = 20 kΩ) (Note 1)		150	V
V <sub>GS</sub>	Gate to Source Voltage		±20	V
I <sub>D</sub>	Drain Current Continuous (T <sub>C</sub> = 25°C, V <sub>GS</sub> = 10 V) (Figure 2)		75	A
	Drain Current Continuous (T <sub>C</sub> = 100°C, V <sub>GS</sub> = 10 V) (Figure 2)		75	A
I <sub>DM</sub>	Pulsed Drain Current		Figure 4	
UIS	Pulsed Avalanche Rating		Figures 6, 14, 15	
P <sub>D</sub>	Power Dissipation	(T <sub>C</sub> = 25°C)	500	W
		– Derate Above 25°C	3.33	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature		–55 to +175	°C
T <sub>L</sub>	Maximum Temperature for Soldering	Leads at 0.063 in (1.6 mm) from Case for 10 s	300	°C
T <sub>pkg</sub>		Package Body for 10 s	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Starting T<sub>J</sub> = 25°C to 150°C.

## PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Package	Brand
HUFA75852G3-F085	TO-247	75852G

# HUFA75852G3-F085

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### OFF STATE CHARACTERISTICS

$B_{V_{DS}}$	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0\ \text{V}$ (Figure 11)	150			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 140\ \text{V}$ , $V_{GS} = 0\ \text{V}$			1	$\mu\text{A}$
		$V_{DS} = 135\ \text{V}$ , $V_{GS} = 0\ \text{V}$ , $T_C = 150^\circ\text{C}$			250	
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}$			$\pm 100$	nA

### ON STATE CHARACTERISTICS

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\ \mu\text{A}$ (Figure 10)	2.0		4.0	V
$R_{DS(ON)}$	Drain to Source On Resistance	$I_D = 75\ \text{A}$ , $V_{GS} = 10\ \text{V}$ (Figure 9)		0.013	0.016	$\Omega$

### THERMAL CHARACTERISTICS

$R_{\theta JC}$	Thermal Resistance Junction to Case	TO-247			0.30	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient				30	$^\circ\text{C/W}$

### SWITCHING CHARACTERISTICS

$t_{on}$	Turn-On Time	$V_{DD} = 75\ \text{V}$ $I_D = 75\ \text{A}$ $V_{GS} = 10\ \text{V}$ $R_{GS} = 2.0\ \Omega$ (Figures 18, 19)			260	ns
$t_{d(on)}$	Turn-On Delay Time			22		ns
$t_r$	Rise Time			151		ns
$t_{d(off)}$	Turn-Off Delay Time			82		ns
$t_f$	Fall Time			107		ns
$t_{off}$	Turn-Off Time				285	ns

### GATE CHARGE CHARACTERISTICS

$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $20\ \text{V}$	$V_{DD} = 75\ \text{V}$ $I_D = 75\ \text{A}$ $I_{g(REF)} = 1.0\ \text{mA}$ (Figures 13,16,17)		400	480	nC
$Q_{g(10)}$	Total Gate Charge 10 V	$V_{GS} = 0\ \text{V}$ to $10\ \text{V}$			215	260	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0\ \text{V}$ to $2\ \text{V}$			15	17.5	nC
$Q_{gs}$	Gate to Source Gate Charge	$V_{DD} = 75\ \text{V}$ , $I_D = 75\ \text{A}$			25		nC
$Q_{gd}$	Gate to Drain "Miller" Charge	$I_{g(REF)} = 1.0\ \text{mA}$ , (Figures 13,16, 17)			66		nC

### CAPACITANCE CHARACTERISTICS

$C_{ISS}$	Input Capacitance	$V_{DS} = 25\ \text{V}$ , $V_{GS} = 0\ \text{V}$ , $f = 1\ \text{MHz}$ (Figure 12)		7690		pF
$C_{OSS}$	Output Capacitance			1650		pF
$C_{RSS}$	Reverse Transfer Capacitance			535		pF

### SOURCE TO DRAIN DIODE CHARACTERISTICS

$V_{SD}$	Source to Drain Diode Voltage	$I_{SD} = 75\ \text{A}$			1.25	V
		$I_{SD} = 35\ \text{A}$			1.00	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 75\ \text{A}$ , $dI_{SD}/dt = 100\ \text{A}/\mu\text{s}$			260	ns
$Q_{rr}$	Reverse Recovery Charge				1830	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

( $T_C = 25^\circ\text{C}$  unless otherwise noted)

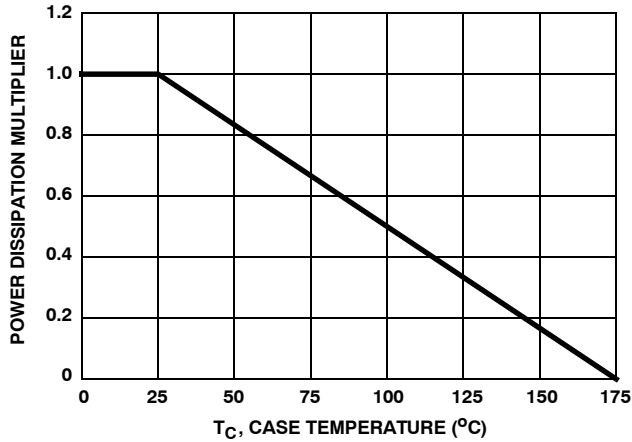


Figure 1. Normalized Power Dissipation vs. Case Temperature

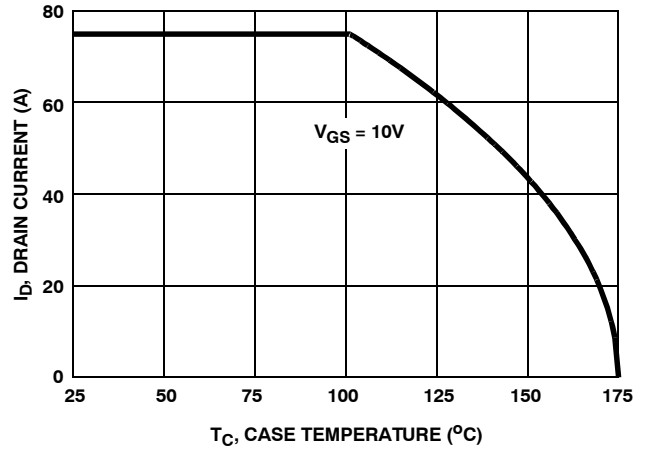


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

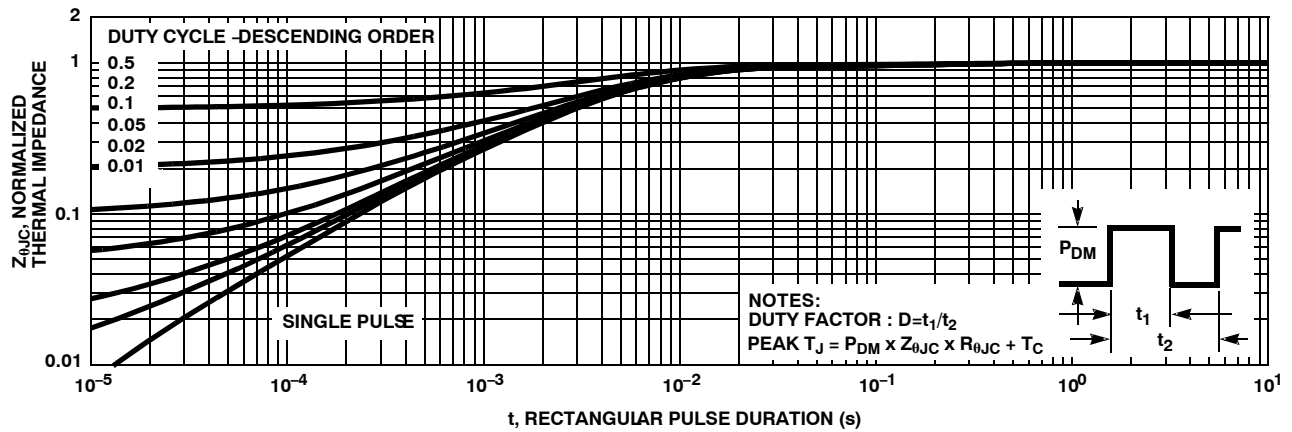


Figure 3. Normalized Maximum Transient Thermal Impedance

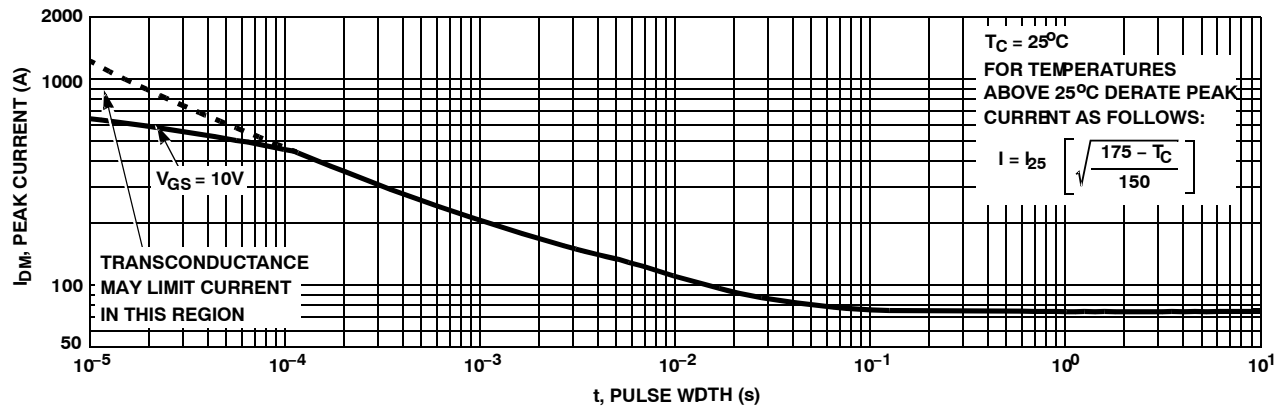


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (Continued)

$T_C = 25^\circ\text{C}$  unless otherwise noted

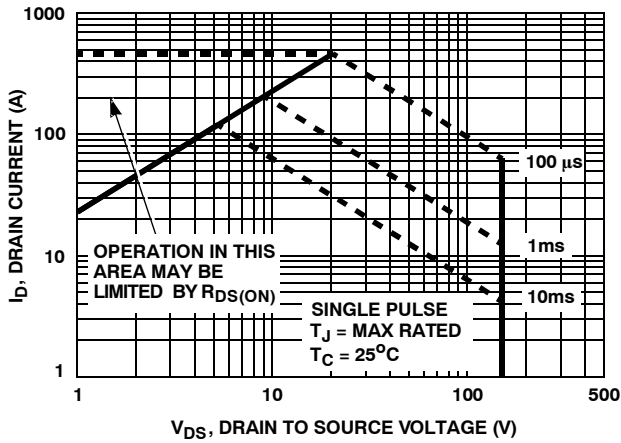


Figure 5. Forward Bias Safe Operating Area

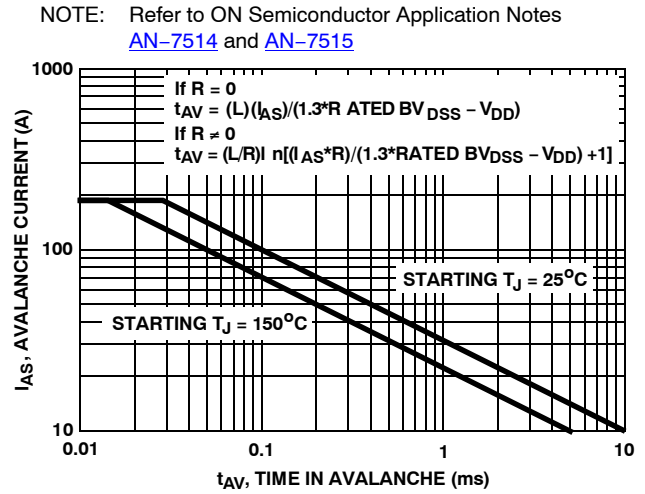


Figure 6. Unclamped Inductive Switching Capability

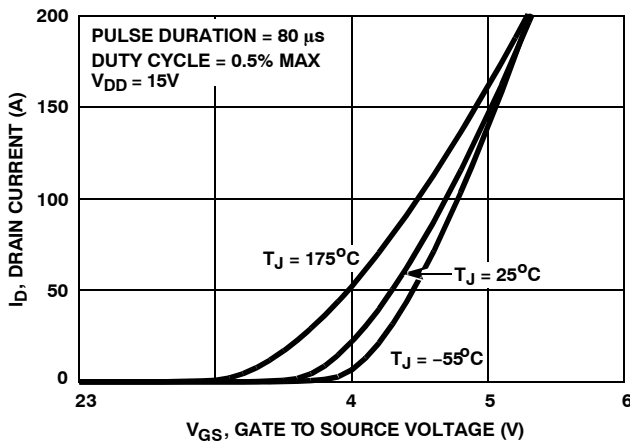


Figure 7. Transfer Characteristics

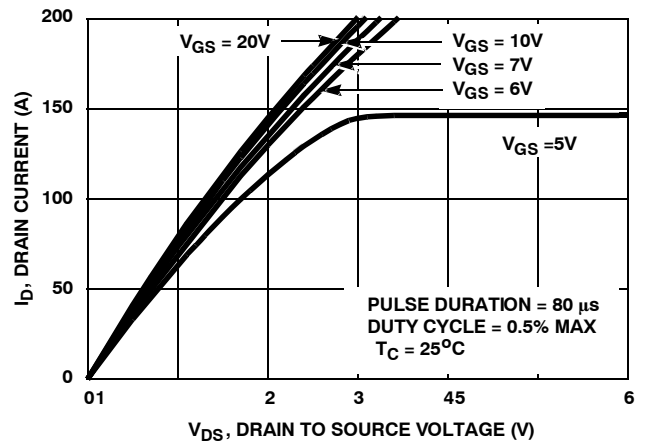


Figure 8. Saturation Characteristics

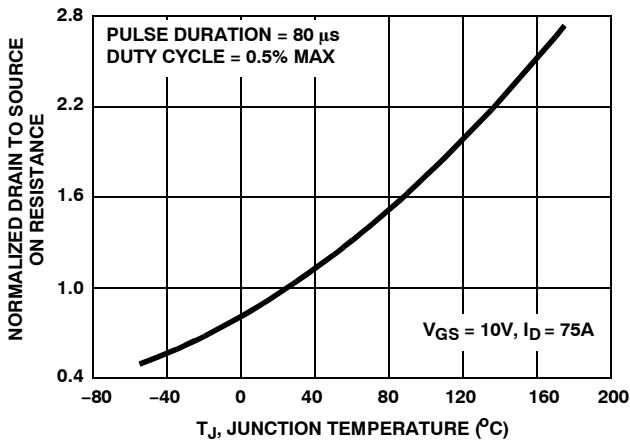


Figure 9. Normalized Drain to Source Resistance vs. Junction Temperature

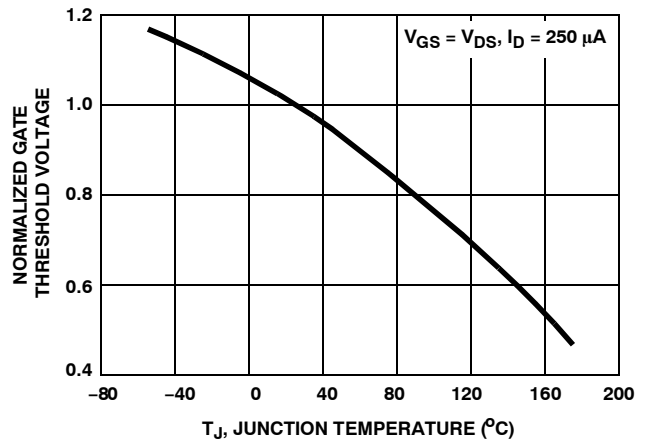


Figure 10. Normalized Gate Threshold Voltage vs. Junction Temperature

TYPICAL CHARACTERISTICS (Continued)

( $T_C = 25^\circ\text{C}$  unless otherwise noted)

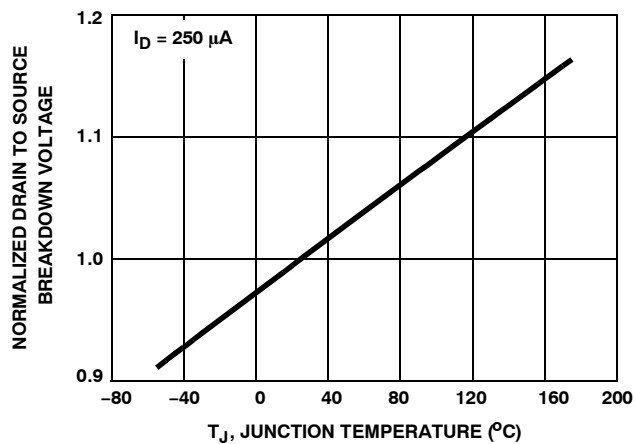


Figure 11. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

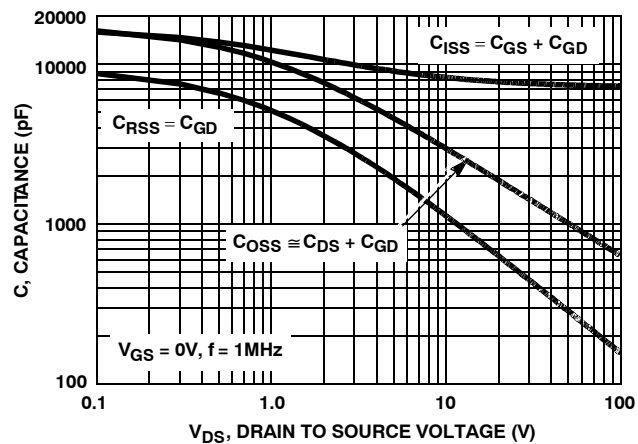


Figure 12. Capacitance vs. Drain to Source Voltage

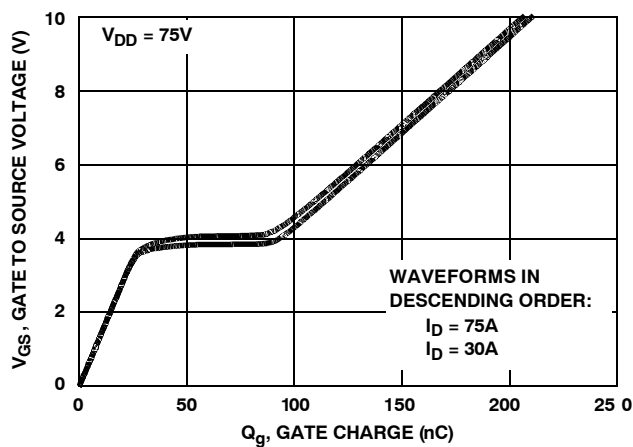


Figure 13. Gate Charge Waveforms for Constant Gate Current

TEST CIRCUITS AND WAVEFORMS

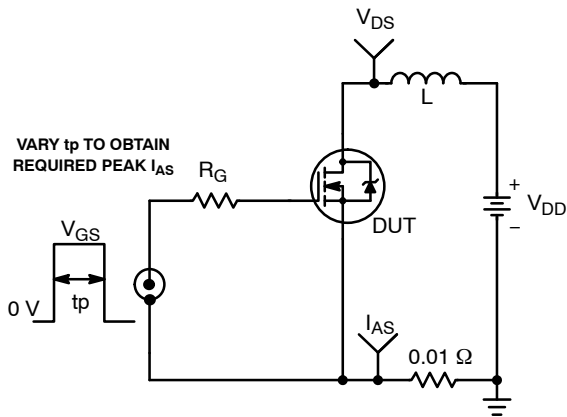


Figure 14. Unclamped Energy  
Test Circuit

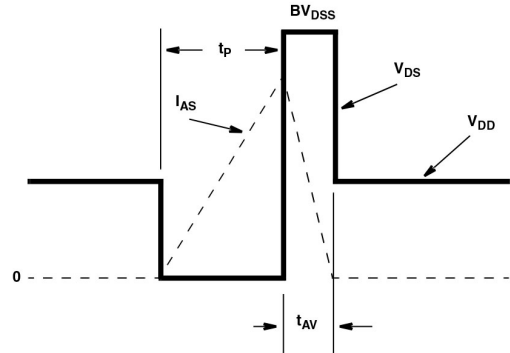


Figure 15. Unclamped Energy  
Waveforms

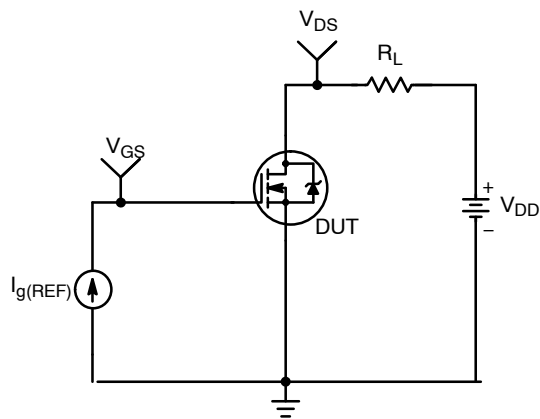


Figure 16. Gate Charge Test Circuit

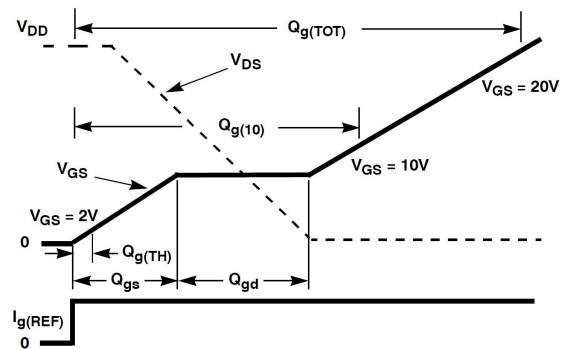


Figure 17. Gate Charge Waveforms

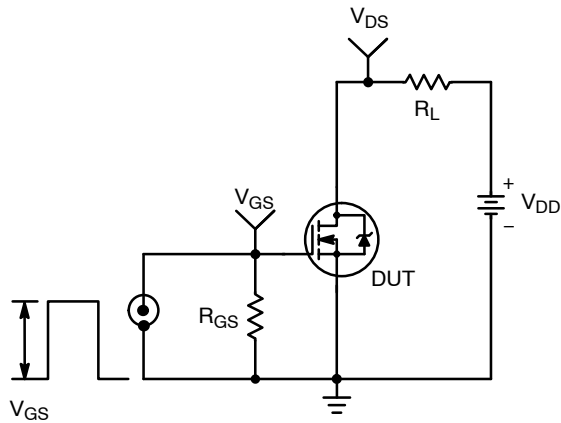


Figure 18. Switching Time Test Circuit

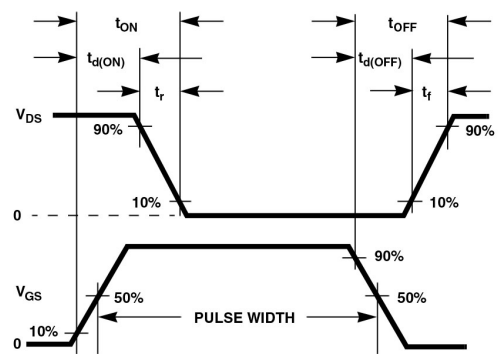
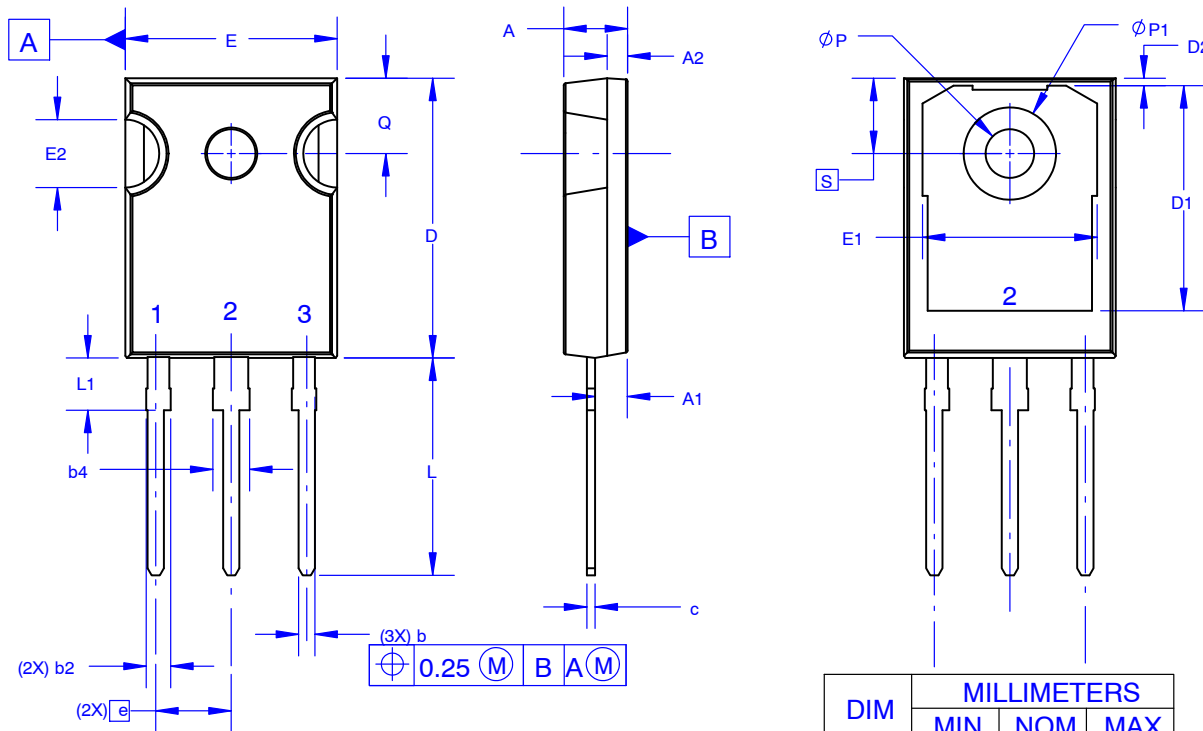


Figure 19. Switching Time Waveforms

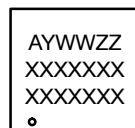
**TO-247-3LD SHORT LEAD**  
**CASE 340CK**  
**ISSUE A**

DATE 31 JAN 2019



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.  
B. ALL DIMENSIONS ARE IN MILLIMETERS.  
C. DRAWING CONFORMS TO ASME Y14.5 - 2009.  
D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.  
E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

**GENERIC**  
**MARKING DIAGRAM\***


XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
ZZ = Assembly Lot Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D	20.32	20.57	20.82
D1	13.08	~	~
D2	0.51	0.93	1.35
E	15.37	15.62	15.87
E1	12.81	~	~
E2	4.96	5.08	5.20
e	~	5.56	~
L	15.75	16.00	16.25
L1	3.69	3.81	3.93
$\phi P$	3.51	3.58	3.65
$\phi P1$	6.60	6.80	7.00
Q	5.34	5.46	5.58
S	5.34	5.46	5.58

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