onsemi

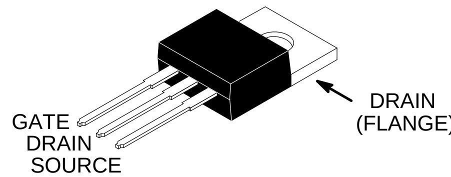
DATA SHEET
www.onsemi.com

MOSFET – Power, N-Channel, UltraFET

100 V, 75 A, 14 mΩ

HUF75645P3

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
100 V	14 mΩ @ 10 V	75 A



TO−220−3LD
CASE 340AT

Features

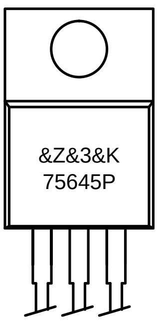
- Ultra Low On−Resistance
  - $R_{DS(ON)}$ = 0.014 Ω, V_{GS} = 10 V
- Simulation Models
  - Temperature Compensated PSPICE™ and Saber® Electrical Models
  - Spice and Saber Thermal Impedance Models
  - www.onsemi.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- This Device is Pb−Free, Halide Free and is RoHS Compliant

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, unless otherwise noted)

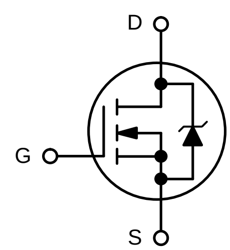
Symbol	Parameter		Ratings	Unit
V_{DSS}	Drain to Source Voltage (Note 1)		100	V
V_{DGR}	Drain to Gate Voltage (R_{GS} = 20 kΩ) (Note 1)		100	V
V_{GS}	Gate to Source Voltage		±20	V
I_D	Drain Current	Continuous (T_C = 25°C, V_{GS} = 10 V) (Figure 2)	75	A
		Continuous (T_C = 100°C, V_{GS} = 10 V) (Figure 2)	65	A
I_{DM}	Pulsed Drain Current		Figure 4	
UIS	Pulsed Avalanche Rating		Figures 6, 14, 15	
P_D	Power Dissipation		310	W
		Derate Above 25°C	2.07	W/°C
T_J, T_{STG}	Operating and Storage Temperature		−55 to 175	°C
T_L	Maximum Temperature for Soldering	Leads at 0.063 in (1.6 mm) from Case for 10 s	300	°C
T_{pkg}		Package Body for 10 s, See Techbrief TB334	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. T_J = 25°C to 150°C.

MARKING DIAGRAM



&Z = Assembly Plant Code
&3 = Data Code (Year & Week)
&K = Lot Code
75645P = Specific Device Code



N−Channel MOSFET

ORDERING INFORMATION

Device	Package	Shipping
HUF75645P3	TO−220−3LD	800 Units / Tube

June, 2024 − Rev. 4
Publication Order Number:
HUF75645P3/D

ELECTRICAL SPECIFICATIONS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
OFF STATE SPECIFICATIONS							
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V (Figure 11)		100	–	–	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 95 V, V_{GS} = 0 V		–	–	1	μA
		V_{DS} = 90 V, V_{GS} = 0 V, T_C = 150°C		–	–	250	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V		–	–	±100	nA
ON STATE SPECIFICATIONS							
$V_{GS(TH)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA (Figure 10)		2	–	4	V
$R_{DS(ON)}$	Drain to Source On Resistance	I_D = 75 A, V_{GS} = 10 V (Figure 9)		–	0.0115	0.014	Ω
THERMAL SPECIFICATIONS							
$R_{\theta JC}$	Thermal Resistance Junction to Case	TO−220		–	–	0.48	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient			–	–	62	°C/W
SWITCHING SPECIFICATIONS (V_{GS} = 10 V)							
t_{ON}	Turn−On Time	V_{DD} = 50 V, I_D = 75 A, V_{GS} = 10 V, R_{GS} = 2.5 Ω (Figures 18, 19)		–	–	197	ns
$t_{d(ON)}$	Turn−On Delay Time			–	14	–	ns
t_r	Rise Time			–	117	–	ns
$t_{d(OFF)}$	Turn−Off Delay Time			–	41	–	ns
t_f	Fall Time			–	97	–	ns
t_{OFF}	Turn−Off Time			–	–	207	ns
GATE CHARGE SPECIFICATIONS							
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 20 V	V_{DD} = 50 V, I_D = 75 A, $I_{g(REF)}$ = 1.0 mA (Figures 13, 16, 17)	–	198	238	nC
$Q_{g(10)}$	Gate Charge at 10 V	V_{GS} = 0 V to 10 V		–	106	127	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0 V to 2 V		–	6.8	8.2	nC
Q_{gs}	Gate to Source Gate Charge			–	14	–	nC
Q_{gd}	Gate to Drain "Miller" Charge			–	41	–	nC
CAPACITANCE SPECIFICATIONS							
C_{ISS}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz (Figure 12)		–	3790	–	pF
C_{OSS}	Output Capacitance			–	810	–	pF
C_{RSS}	Reverse Transfer Capacitance			–	230	–	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

SOURCE TO DRAIN DIODE SPECIFICATIONS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF STATE SPECIFICATIONS						
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 75 A	–	–	1.25	V
		I_{SD} = 35 A	–	–	1.00	V
t_{rr}	Reverse Recovery Time	I_{SD} = 75 A, dI_{SD}/dt = 100 A/μs	–	–	145	ns
Q_{RR}	Reverse Recovered Charge	I_{SD} = 75 A, dI_{SD}/dt = 100 A/μs	–	–	360	nC

TYPICAL PERFORMANCE CURVES

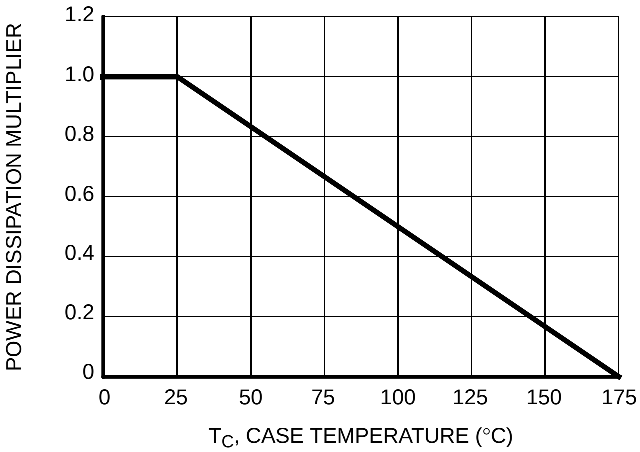


Figure 1. Normalized Power Dissipation vs. Case Temperature

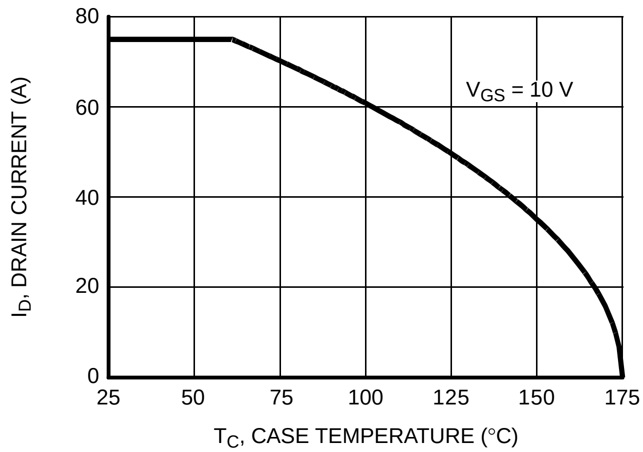


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

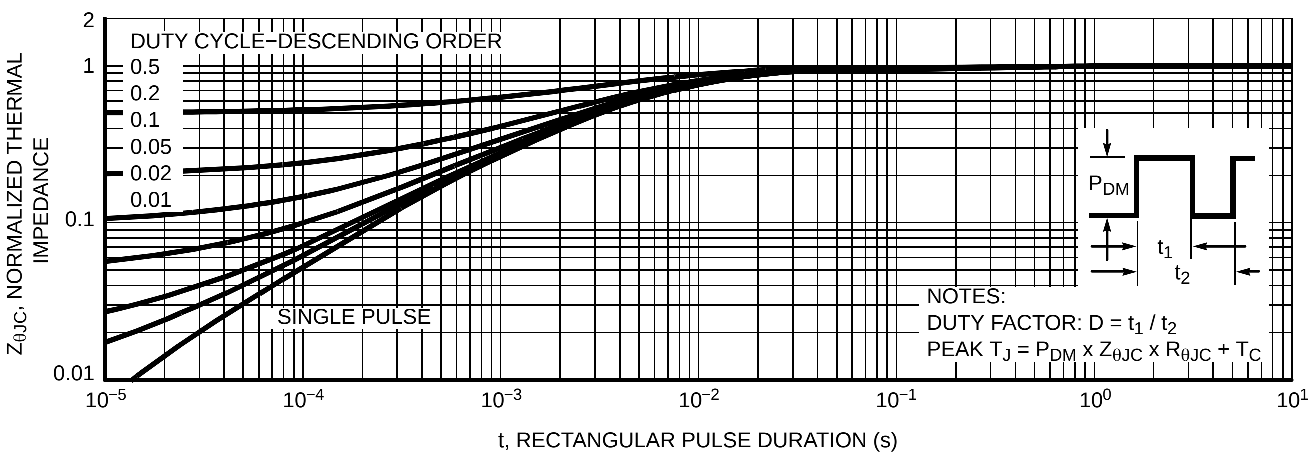


Figure 3. Normalized Maximum Transient Thermal Impedance

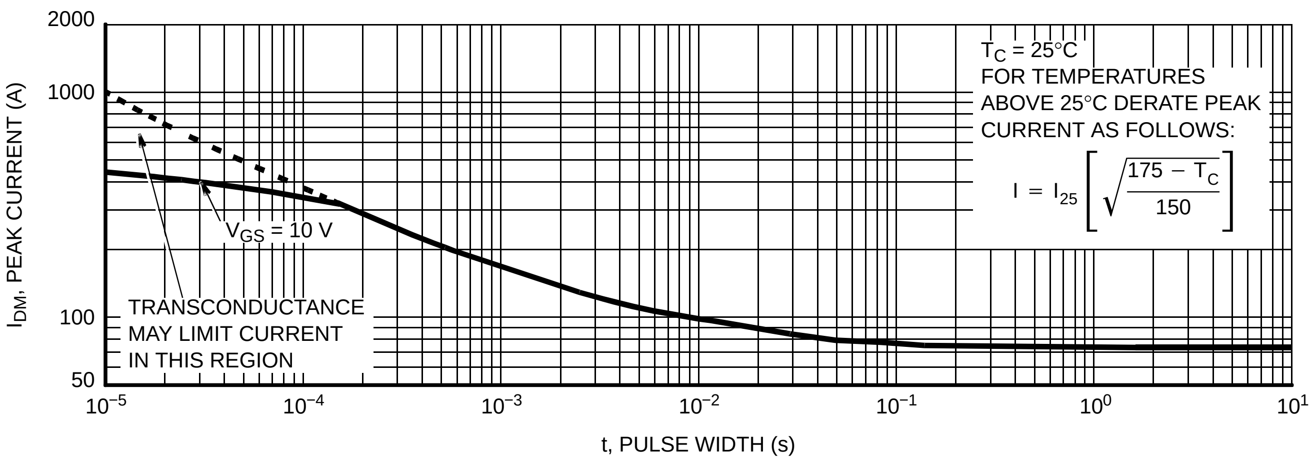


Figure 4. Peak Current Capability

TYPICAL PERFORMANCE CURVES (CONTINUED)

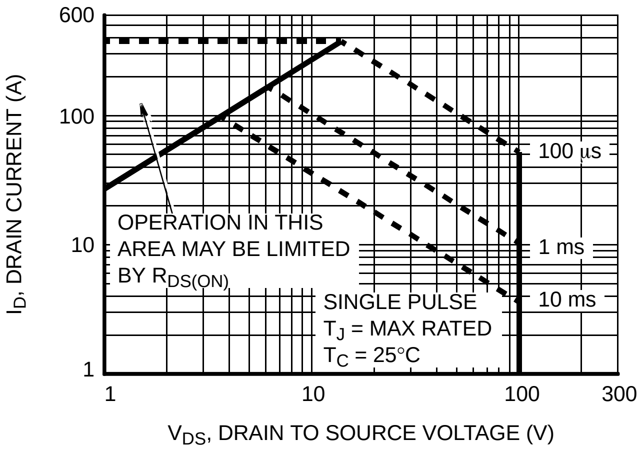
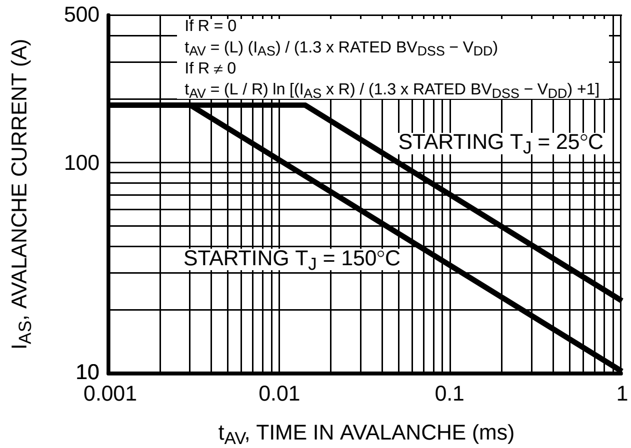


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to **onsemi** Application Notes AN9321 and AN9322.

Figure 6. Unclamped Inductive Switching Capability

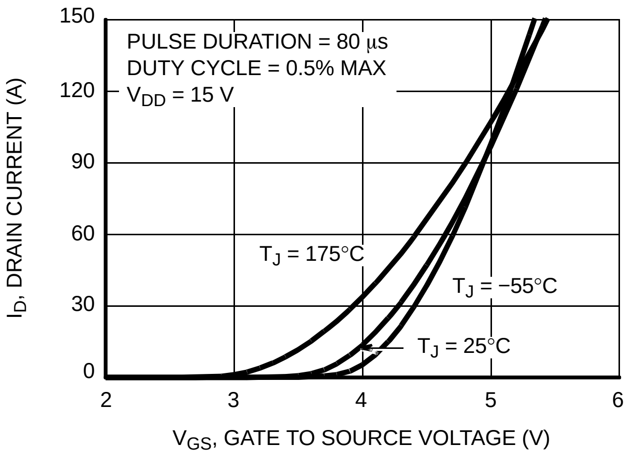


Figure 7. Transfer Characteristics

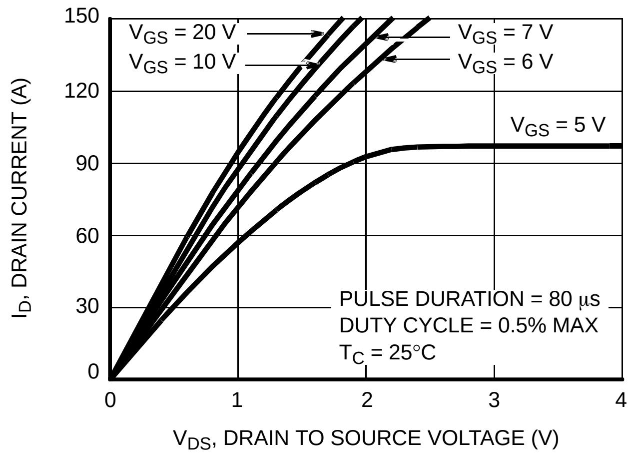


Figure 8. Saturation Characteristics

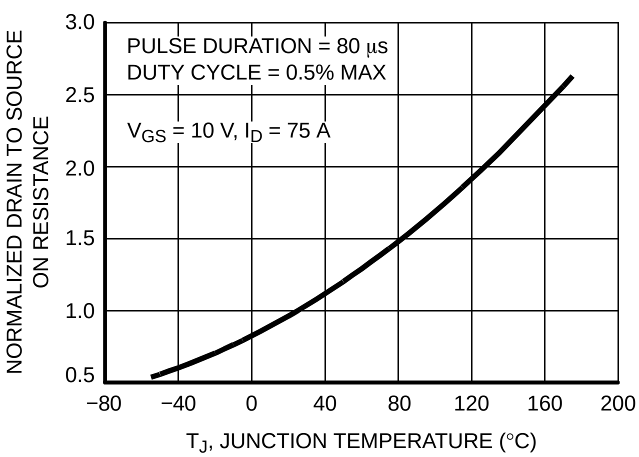


Figure 9. Normalized Drain to Source On Resistance vs. Junction Temperature

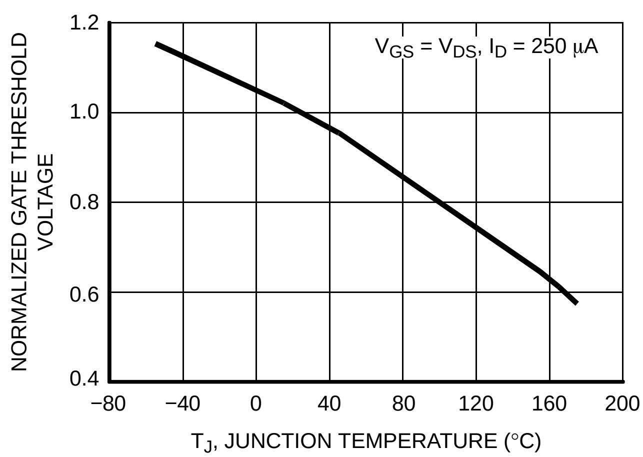


Figure 10. Normalized Gate Threshold Voltage vs. Junction Temperature

TYPICAL PERFORMANCE CURVES (CONTINUED)

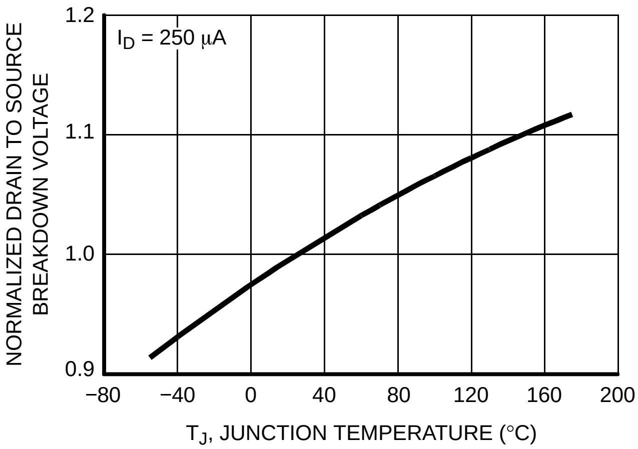


Figure 11. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

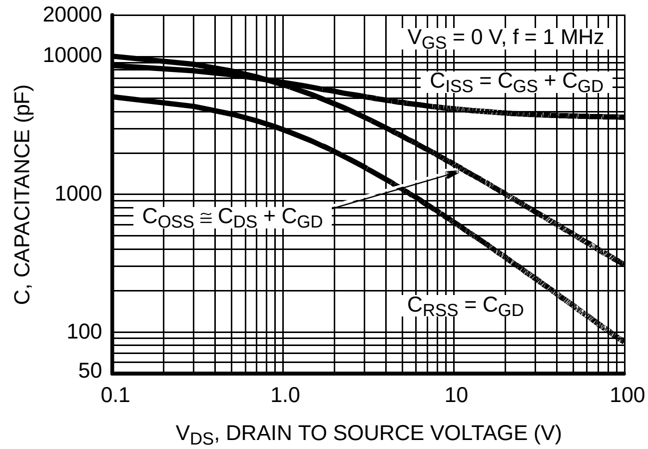
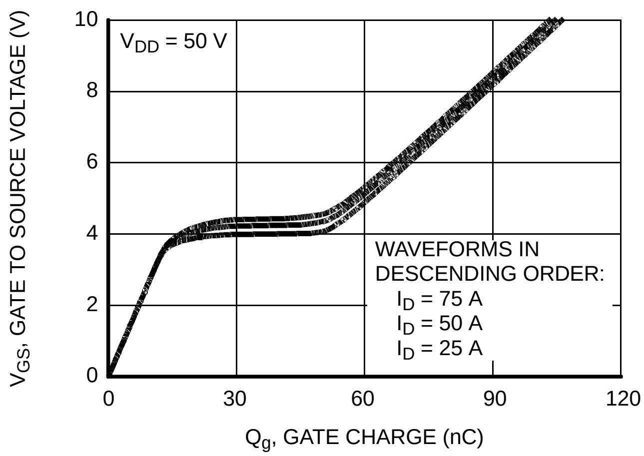


Figure 12. Capacitance vs. Drain to Source Voltage



NOTE: Refer to **onsemi** Application Notes AN7254 and AN7260.

Figure 13. Gate Charge Waveforms for Constant Gate Current

TEST CIRCUITS AND WAVEFORMS

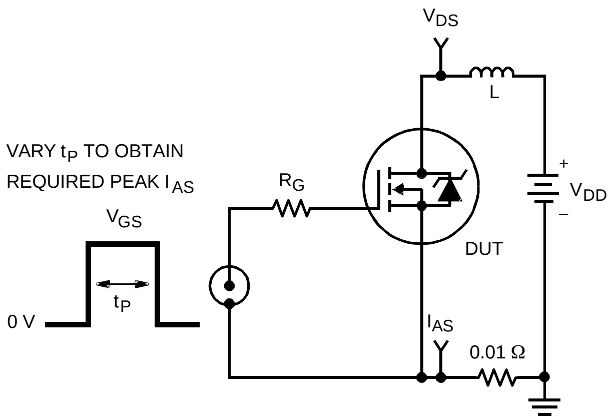


Figure 14. Unclamped Energy Test Circuit

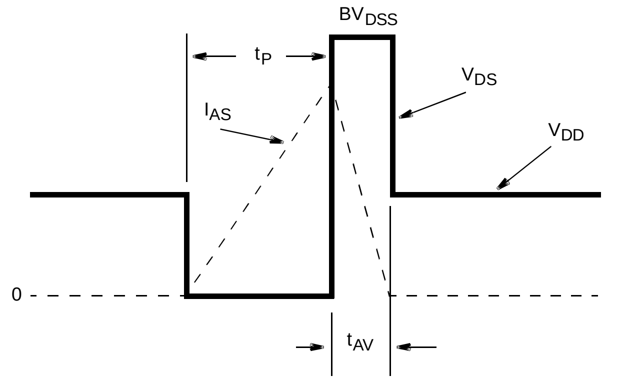


Figure 15. Unclamped Energy Waveforms

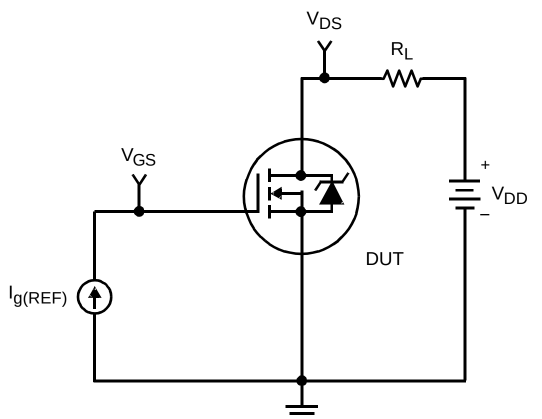


Figure 16. Gate Charge Test Circuit

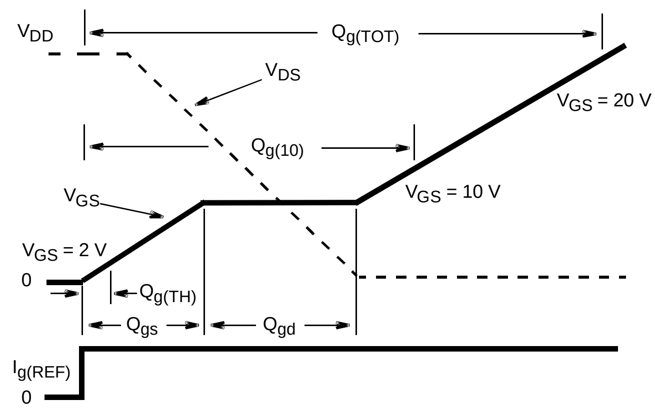


Figure 17. Gate Charge Waveforms

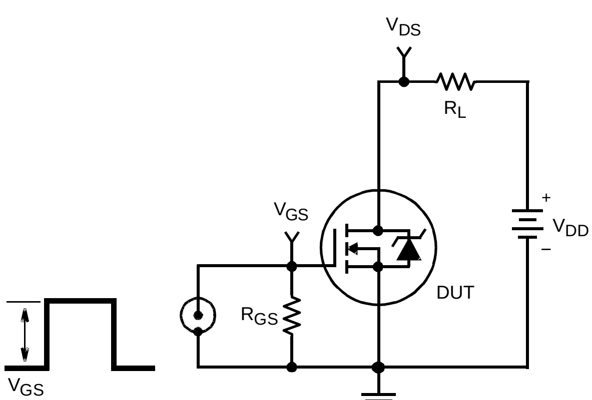


Figure 18. Switching Time Test Circuit

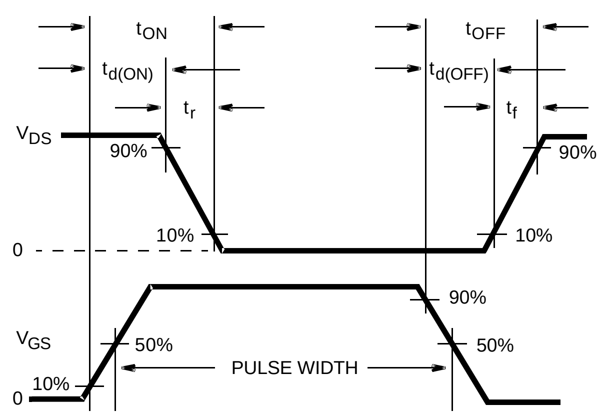


Figure 19. Switching Time Waveforms

PSPICE ELECTRICAL MODEL

```
.SUBCKT HUF75645 2 1 3 ;      rev 21 May 1999

CA 12 8 5.31e−9
CB 15 14 5.31e−9
CIN 6 8 3.56e−9

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 115.5
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1.0e−9
LGATE 1 9 5.1e−9
LSOURCE 3 7 4.4e−9

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 7.80e−3
RGATE 9 20 0.83
RLDRAIN 2 5 10
RLGATE 1 9 26
RLSOURCE 3 7 11
RSLC1 5 51 RSLCMOD 1e−6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 1.65e−3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e−6*205),3.5))}
```

.MODEL DBODYMOD D (IS = 3.00e−12 IKF = 19 RS = 1.78e−3 XTI = 5 TRS1 = 2.25e−3 TRS2 = 1.00e−5 CJO = 5.32e−9 TT = 7.4e−8 M = 0.68)
.MODEL DBREAKMOD D (RS = 2.15e− 1IKF = 1 TRS1 = 8e− 4TRS2 = 3e−6)
.MODEL DPLCAPMOD D (CJO = 5.55e− 9IS = 1e−3 0M = 0.98)
.MODEL MMEDMOD NMOS (VTO = 3.13 KP = 10 IS = 1e−30 N = 10 TOX = 1 L = 1u W = 1u RG = 0.83)
.MODEL MSTROMOD NMOS (VTO = 3.51 KP = 93 IS = 1e−30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 2.65 KP = 0.11 IS = 1e−30 N = 10 TOX = 1 L = 1u W = 1u RG = 8.33)
.MODEL RBREAKMOD RES (TC1 = 9.9e− 4TC2 = −1.3e−6)
.MODEL RDRAINMOD RES (TC1 = 9.40e−3 TC2 = 2.93e−5)
.MODEL RSLCMOD RES (TC1 = 2.63e−3 TC2 = 1.05e−6)
.MODEL RSOURCEMOD RES (TC1 = 1e−3 TC2 = 1e−6)
.MODEL RVTHRESMOD RES (TC1 = −2.57e−3 TC2 = −7.05e−6)
.MODEL RVTEMPMOD RES (TC1 = −2.87e− 3TC2 = −2.21e−6)

.MODEL S1AMOD VSWITCH (RON = 1e−5 ROFF = 0.1 VON = −6.2 VOFF= −2.4)
.MODEL S1BMOD VSWITCH (RON = 1e−5 ROFF = 0.1 VON = −2.4 VOFF= −6.2)
.MODEL S2AMOD VSWITCH (RON = 1e−5 ROFF = 0.1 VON = −1.8 VOFF= 0.5)
.MODEL S2BMOD VSWITCH (RON = 1e−5 ROFF = 0.1 VON = 0.5 VOFF= −1.8)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub−Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

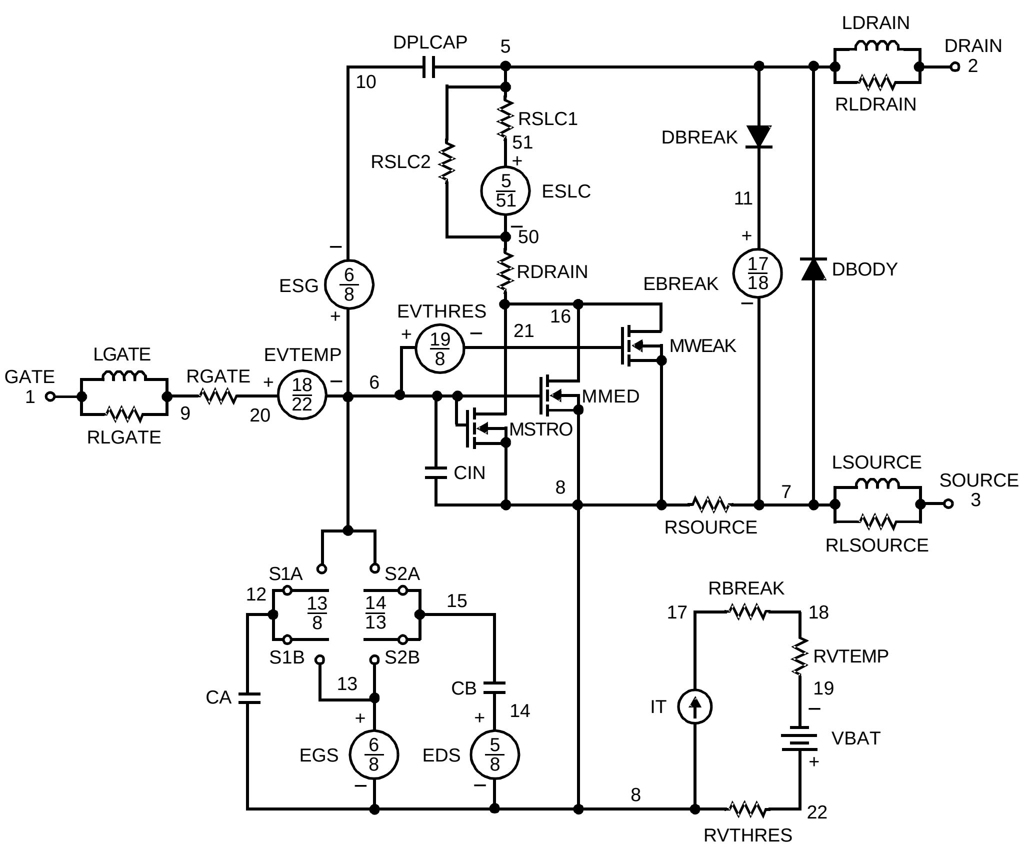


Figure 20.

SABER ELECTRICAL MODEL

REV 21 May 1999

```
template ta75645 n2,n1,n3
electrical n2,n1,n3
{
var i iscl
d..model dbodymod = (is = 3.00e−12, cjo = 5.32e−9, tt = 7.4e−8, xti = 5, m = 0.68)
d..model dbreakmod = ()
d..model dplcapmod = (cjo = 5.55e−9, is = 1e−30, vj=1.0, m = 0.8)
m..model mmedmod = (type=_n, vto = 3.13, kp = 10, is = 1e−30, tox = 1)
m..model mstrongmod = (type=_n, vto = 3.51, kp = 93, is = 1e−30, tox = 1)
m..model mweakmod = (type=_n, vto = 2.65, kp = 0.11, is = 1e−30, tox = 1)
sw_vcsp..model s1amod = (ron = 1e−5, roff = 0.1, von = −6.2, voff = −2.4)
sw_vcsp..model s1bmod = (ron =1e−5, roff = 0.1, von = −2.4, voff = −6.2)
sw_vcsp..model s2amod = (ron = 1e−5, roff = 0.1, von = −1.8, voff = 0.5)
sw_vcsp..model s2bmod = (ron = 1e−5, roff = 0.1, von = 0.5, voff = −1.8)

c.ca n12 n8 = 5.31e−9
c.cb n15 n14 = 5.31e−9
c.cin n6 n8 = 3.56e−9

d.dbody n7 n71 = model=dbodymod
d.dbreak n72 n11 = model=dbreakmod
d.dplcap n10 n5 = model=dplcapmod

i.it n8 n17 = 1

l.ldrain n2 n5 = 1e−9
l.lgate n1 n9 = 5.1e−9
l.lsource n3 n7 = 4.4e−9

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18 = 1, tc1 = 9.9e−4, tc2 = −1.3e−6
res.rdbody n71 n5 = 1.78e−3, tc1 = 2.25e−3, tc2 = 1.e−5
res.rdbreak n72 n5 = 2.15e−1, tc1 = 8e−4, tc2 = 3e−6
res.rdrain n50 n16 = 7.8e−3, tc1 = 9.4e−3, tc2 = 2.93e−5
res.rgate n9 n20 = 0.83
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 26
res.rlsource n3 n7 = 11
res.rslc1 n5 n51 = 1e−6, tc1 = 2.63e−3, tc2 = 1.05e−6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 1.65e−3, tc1 = 1e−3, tc2 = 1e−6
res.rvtemp n18 n19 = 1, tc1 = −2.87e−3, tc2 = −2.21e−6
res.rvthres n22 n8 = 1, tc1 = −2.57e−3, tc2 = −7.05e−6

spe.ebreak n11 n7 n17 n18 = 115.5
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1
```

```
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1

equations {
i (n51−>n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e−9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/205))** 3.5))
}
}
```

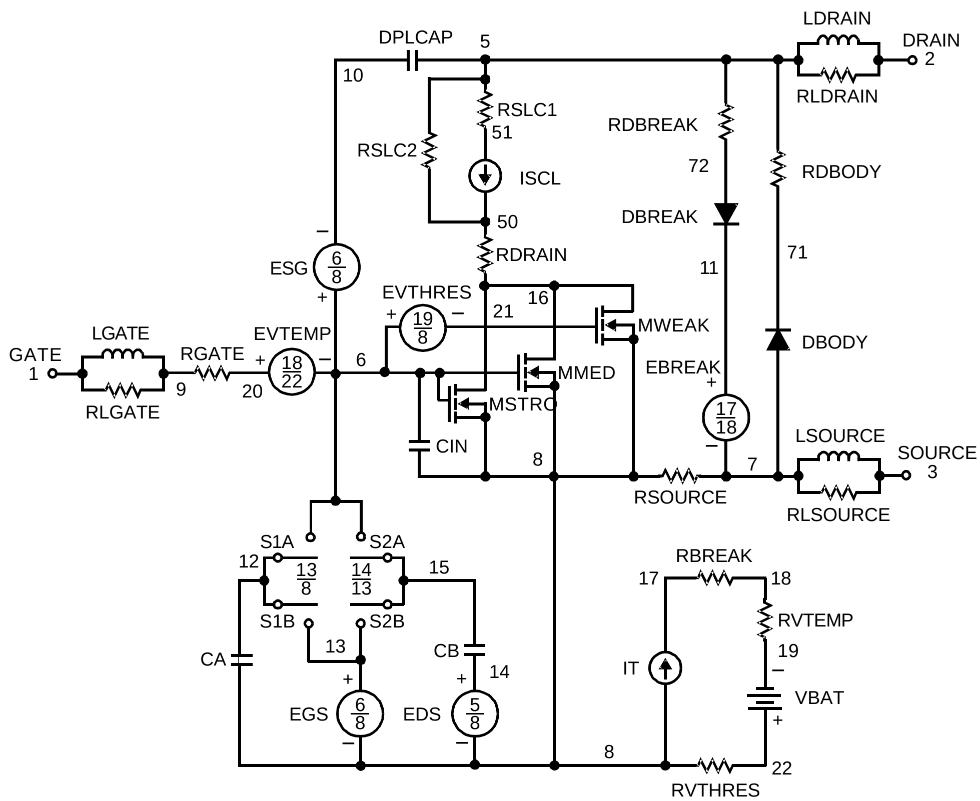


Figure 21.

SPICE THERMAL MODEL

REV 28 July 1999

HUF75645T

CTHERM1 th 6 8.80e−3
CTHERM2 6 5 2.50e−2
CTHERM3 5 4 2.70e−2
CTHERM4 4 3 3.70e−2
CTHERM5 3 2 4.40e−2
CTHERM6 2 tl 3.40e−1

RTHERM1 th 6 1.20e−2
RTHERM2 6 5 3.00e−2
RTHERM3 5 4 4.30e−2
RTHERM4 4 3 8.80e−2
RTHERM5 3 2 9.90e−2
RTHERM6 2 tl 1.10e−1

SABER THERMAL MODEL

SABER thermal model HUF75645T

template thermal_model th tl
thermal_c th, tl

{
ctherm.ctherm1 th 6 = 8.80e−3
ctherm.ctherm2 6 5 = 2.50e−2
ctherm.ctherm3 5 4 = 2.70e−2
ctherm.ctherm4 4 3 = 3.70e−2
ctherm.ctherm5 3 2 = 4.40e−2
ctherm.ctherm6 2 tl = 3.40e−1

rtherm.rtherm1 th 6 = 1.20e−2
rtherm.rtherm2 6 5 = 3.00e−2
rtherm.rtherm3 5 4 = 4.30e−2
rtherm.rtherm4 4 3 = 8.80e−2
rtherm.rtherm5 3 2 = 9.90e−2
rtherm.rtherm6 2 tl = 1.10e−1
}

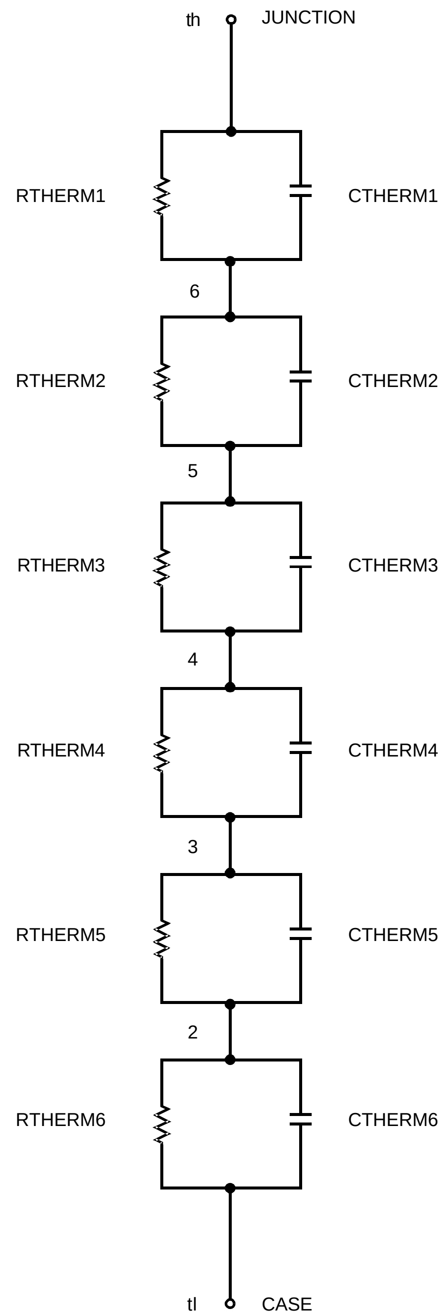
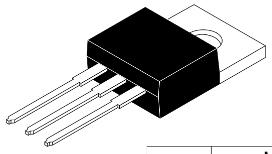


Figure 22.

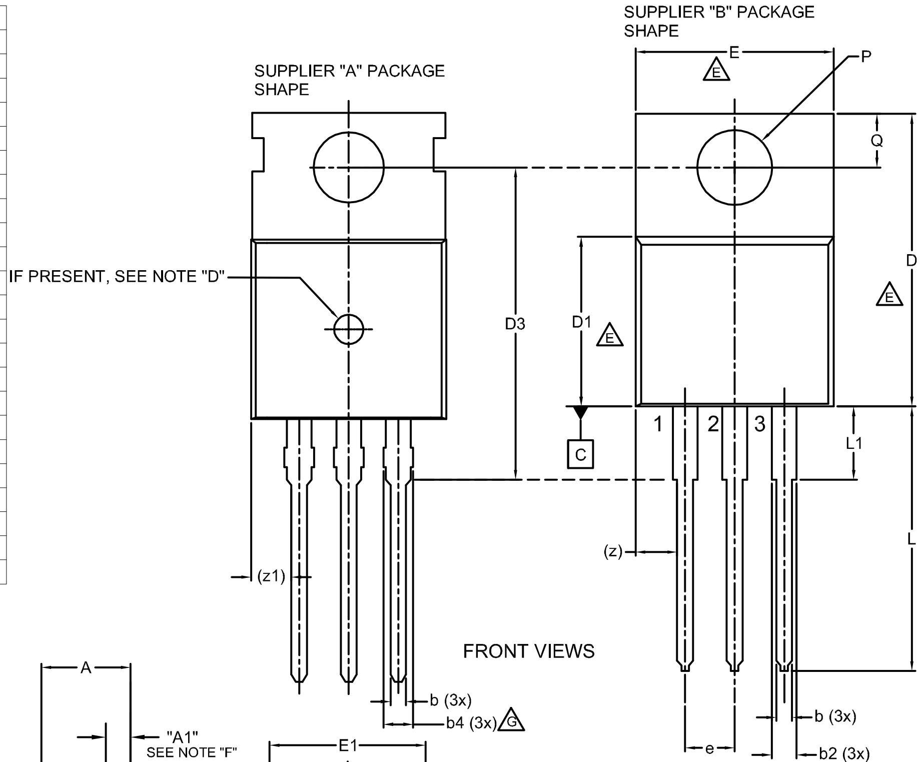
PSPICE is a trademark of MicroSim Corporation.
Saber is a registered trademark of Sabremark Limited Partnership.



TO−220−3LD
CASE 340AT
ISSUE B

DATE 08 AUG 2022

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	4.00	--	4.70
A1	SEE NOTE "F"		
A2	2.10	--	2.85
b	0.55	--	1.00
b2	1.10	--	1.62
b4	1.42	--	1.62
c	0.36	--	0.60
D	13.90	--	16.30
D1	8.13	--	9.40
D2	11.50	--	14.30
D3	15.42	--	16.51
E	9.65	--	10.67
E1	7.59	--	8.65
e	2.40	--	2.67
H1	6.06	--	6.69
L	12.70	--	14.04
L1	2.70	--	4.10
P	3.50	--	4.00
Q	2.50	--	3.40
z	2.13 REF		
z1	2.06 REF		
Θ	3°	--	5°

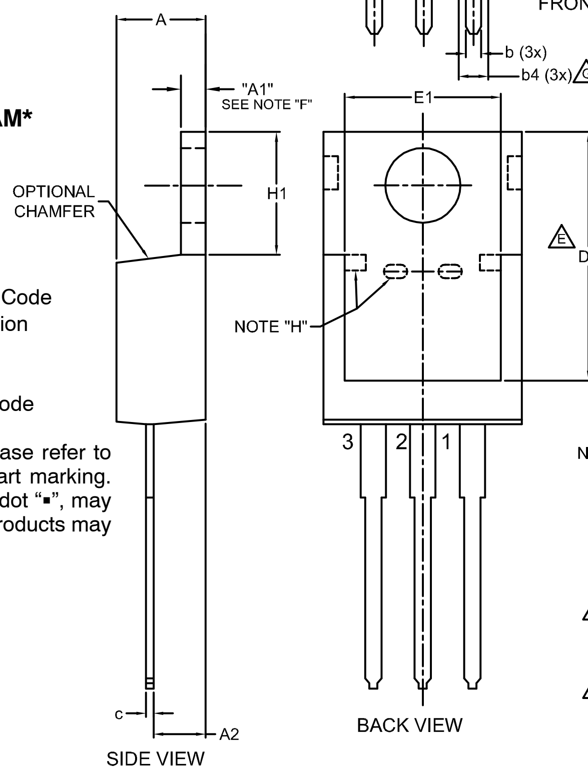


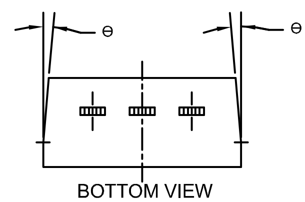
GENERIC MARKING DIAGRAM*

XXXXX
XXXXX
AYWWZZ

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.





NOTES:
A) REFERENCE JEDEC, TO-220, VARIATION AB
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
E) DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS AS BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.10 - 1.45
G) PRESENCE IS SUPPLIER DEPENDENT
H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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