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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor’s system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.
# FTL7522

Low $I_{CCT}$ Reset Timer with Fixed Delay and Reset Pulse

## Features
- Fixed Reset Delay: 7.5 Seconds
- Expanded $V_{IH}$ Input Range Allows Direct Interface to Lower Voltage Chips, (No Translator Needed)
- Low $I_{CCT}$ Feature Saves Power when Interfacing with Low-Voltage Chips
- One Input Reset Pin
- Open-Drain Output Pin with Fixed 400ms Pulse
- 1.8V to 5.0V Operation ($T_A=-40°C$ to $+85°C$)
- 1.7V to 5.0V Operation ($T_A=-25°C$ to $+85°C$)
- 1.65V to 5.0V Operation ($T_A=0°C$ to $+85°C$)
- $<1\mu A$ $I_{CCQ}$ Consumption
- Zero-Second Test Mode Enable

## Applications
- Cell Phones
- Portable Media Players
- Tablets
- Mobile Devices
- Consumer Medical

## Description

The FTL7522 is a timer for resetting a mobile device where long reset times are needed. The long delay helps avoid unintended resets caused by accidental key presses. It has a fixed delay of 7.5 ±20% seconds. The DSR pin enables Test Mode operation by immediately forcing $/RST1$ LOW for factory testing.

The FTL7522 has one input for single-button resetting capability. The device has a single open-drain output with 0.5mA pull-down drive.

FTL7522 draws minimal $I_{CC}$ current when inactive and functions over a power supply range of 1.65V to 5.0V.

The FTL7522 low-$I_{CCT}$ feature enables direct interface with lower-voltage chipsets without needing external translation, while maintaining low power consumption.

## Figure 1. Block Diagram

![Block Diagram](image)

## Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Operating Temperature Range</th>
<th>Top Mark</th>
<th>Package</th>
<th>Packing Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>FTL7522L6X</td>
<td>-40°C to +85°C</td>
<td>PC</td>
<td>6-Lead, MicroPak™ 1.0 x 1.45mm, JEDEC MO-252</td>
<td>5000 Units on Tape and Reel</td>
</tr>
</tbody>
</table>
Pin Configuration

Figure 2. Pad Assignments (Top-Through View)

Pin Definitions

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>/RST1</td>
<td>Open-Drain Output, Active LOW</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>/SR0</td>
<td>Reset Input, Active LOW</td>
</tr>
<tr>
<td>4</td>
<td>VCC</td>
<td>Power Supply</td>
</tr>
<tr>
<td>5</td>
<td>DSR</td>
<td>Delay Selection Input. Tie to GND(^{(1)}) during normal operation.</td>
</tr>
<tr>
<td>6</td>
<td>TEST</td>
<td>Used for device testing; should be tied to GND during normal operation.</td>
</tr>
</tbody>
</table>

Description:

- **Normal Operation**: Open-Drain Output, Active LOW
- **0-Second Factory-Test Mode**: Delay Selection Input. Pull HIGH to enable the 0-second delay for factory test.

**Note:**

1. The DSR pin must always be tied to either GND or VCC; it must not float.
Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Supply Voltage</td>
<td></td>
<td>-0.5</td>
<td>7.0</td>
<td>V</td>
</tr>
<tr>
<td>VIN</td>
<td>DC Input Voltage</td>
<td>/SR0, DSR</td>
<td>-0.5</td>
<td>7.0</td>
<td>V</td>
</tr>
<tr>
<td>VOUT</td>
<td>Output Voltage(^{(2)})</td>
<td>/RST1</td>
<td>-0.5</td>
<td>7.0</td>
<td>V</td>
</tr>
<tr>
<td>IK</td>
<td>DC Input Diode Current</td>
<td>VIN &lt; 0V</td>
<td>-50 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IOK</td>
<td>DC Output Diode Current</td>
<td>VOUT &lt; 0V</td>
<td>-50 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IOL</td>
<td>DC Output Sink Current</td>
<td></td>
<td>+50 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ICC</td>
<td>DC VCC or Ground Current per Supply Pin</td>
<td></td>
<td>±100 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TSTG</td>
<td>Storage Temperature Range</td>
<td></td>
<td>-65°C to +150°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TJ</td>
<td>Junction Temperature Under Bias</td>
<td></td>
<td>+150°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TL</td>
<td>Junction Lead Temperature, Soldering 10 Seconds</td>
<td></td>
<td>+260°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PD</td>
<td>Power Dissipation</td>
<td></td>
<td>5 mW</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ESD</td>
<td>Electrostatic Discharge Capability</td>
<td>Human Body Model, JESD22-A114</td>
<td>4 kV</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Charged Device Model, JESD22-C101</td>
<td>2 kV</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note:
2. All output current Absolute Maximum Ratings must be observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Supply Voltage(^{(3)})</td>
<td>-40°C to +85°C</td>
<td>1.8</td>
<td>5.0</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-25°C to +85°C</td>
<td>1.7</td>
<td>5.0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0°C to +85°C</td>
<td>1.65</td>
<td>5.00</td>
<td></td>
</tr>
<tr>
<td>tRFC</td>
<td>VCC Recovery Time After Power Down</td>
<td>VCC=0V After Power Down, Rising to 0.5V</td>
<td>5</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>VIN</td>
<td>Input Voltage(^{(3)})</td>
<td>/SR0</td>
<td>0</td>
<td>5</td>
<td>V</td>
</tr>
<tr>
<td>VOUT</td>
<td>Output Voltage</td>
<td>/RST1</td>
<td>0</td>
<td>5</td>
<td>V</td>
</tr>
<tr>
<td>IOL</td>
<td>DC Output Sink Current</td>
<td>/RST1, VCC=1.8V to 5.0V</td>
<td>+0.5 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TA</td>
<td>Free-Air Operating Temperature</td>
<td></td>
<td>-40°C to +85°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>θJA</td>
<td>Thermal Resistance</td>
<td></td>
<td>350°C/W</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note:
3. VCC should never be allowed to float while input pins are driven.
### DC Electrical Characteristics

Unless otherwise specified; conditions of $T_A=-40$ to $85^\circ C$ with $V_{CC}=1.8 - 5.0V$, OR $T_A=-25$ to $85^\circ C$ with $V_{CC}=1.7 - 5V$, OR $T_A=0$ to $85^\circ C$ with $V_{CC}=1.65 - 5V$ produce the performance characteristics below.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Input High Voltage (/SR0, DSR)</td>
<td>$4.2V &lt; V_{CC} &lt;= 5.0V$</td>
<td>1.8V</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$1.8V &lt;= V_{CC} &lt;= 4.2V$</td>
<td>1.2V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input Low Voltage (/SR0, DSR)</td>
<td></td>
<td>0.45V</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low Level Output Voltage</td>
<td>RST, $I_{OL}=500\mu A$</td>
<td>0.3V</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{IN}$</td>
<td>Input Leakage Current (/SR0, DSR)</td>
<td>$0V \leq V_{IN} \leq 5.0V$</td>
<td>\pm 1.0 \mu A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>Quiescent Supply Current (Timer Inactive)</td>
<td>/SR0, DSR=$V_{CC}$</td>
<td>1 \mu A</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>/SR0=1.8V, DSR=GND, $V_{CC}=5V$</td>
<td>14 \mu A</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>/SR0=1.2V, DSR=GND, $V_{CC}=4V$</td>
<td>11 \mu A</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Dynamic Supply Current (Timer Active)</td>
<td>/SR0, DSR=GND</td>
<td>100 \mu A</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### AC Electrical Characteristics

Unless otherwise specified; conditions of $T_A=-40$ to $80^\circ C$ with $V_{CC}=1.8 - 5.0V$, OR $T_A=-25$ to $85^\circ C$ with $V_{CC}=1.7 - 5V$, OR $T_A=0$ to $85^\circ C$ with $V_{CC}=1.65 - 5V$ produce the performance characteristics below.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PHL1}$</td>
<td>Timer Delay, /SR0 to RST (DSR=0)</td>
<td>$C_L=5pF$, $R_L=5K\Omega$, See Figure 6</td>
<td>6.0</td>
<td>7.5</td>
<td>9.0</td>
<td>s</td>
</tr>
<tr>
<td>$t_{REC}$</td>
<td>Reset Timeout Delay</td>
<td></td>
<td>320</td>
<td>400</td>
<td>480</td>
<td>ms</td>
</tr>
</tbody>
</table>

### Capacitance Specifications

$T_A=+25^\circ C$.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Typical</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{IN}$</td>
<td>Input Capacitance</td>
<td>$V_{CC}=GND$</td>
<td>4.0</td>
<td>pF</td>
</tr>
<tr>
<td>$C_{OUT}$</td>
<td>Output Capacitance</td>
<td>$V_{CC}=5.0V$</td>
<td>5.0</td>
<td>pF</td>
</tr>
</tbody>
</table>
Functional Description

Device default operation time \( N \) is 7.5s. If the DSR pin is pulled HIGH prior to \( V_{CC} \) ramp, the FTL7522 enters Test Mode and the reset output, /RST1, is immediately pulled LOW for factory testing. The DSR pin MUST be forced to GND during normal operation. The DSR pin should never be driven HIGH or left to float during normal operation. The DSR pin state should never be changed during device operation; it must be biased prior to supplying the \( V_{CC} \) supply. If there is a need to use the DSR=VCC Test Mode, the /SR0 must be HIGH when the DSR pin is moved from LOW to HIGH to enter Zero-Second Factory-Test Mode. To return to the standard 7.5-second reset time, the same procedure must be followed with DSR=GND. The DSR pin should never be allowed to change state while the /SR0 pin is LOW.

Operation Modes

A low input signal on /SR0 starts the oscillator. There are two scenarios for counting: short duration and long duration. In the short-duration scenario, output /RST1 is not affected. In the long-duration scenario, the output /RST1 goes LOW after /SR0 has been held LOW for at least 7.5 seconds. The /RST1 output returns to its original HIGH state 400ms after time \( t_{REC} \) has expired, regardless of the state of /SR0. The /RST1 output is an open-drain driver. When the count time exceeds 7.5 seconds, the /RST1 output pulls LOW.

Short Duration \((tW < 7.5s)\)

When the /SR0 input goes LOW, the internal timer starts counting. If the /SR0 input goes HIGH before 7.5s has elapsed, the timer stops counting and resets; no changes occur on the outputs.

Long Duration \((tW > 7.5s)\)

When the /SR0 input goes LOW, the internal timer starts counting. If the /SR0 input stays LOW for at least 7.5s, the RST output is enabled and pulled LOW. The output RST is held LOW for \( t_{REC} \), 400ms, as soon as the reset time of 7.5s is met, regardless of the state of the /SR0 pin. When the /SR0 input has returned HIGH and \( t_{REC} \) has expired, the internal timer resets and awaits the next RESET event.

0-Second Test Mode

/RST1 goes LOW immediately after /SR0 goes LOW.

Figure 3. Reset Timing Waveforms
Application Diagram

Figure 4. Recommended Application Diagram

AC Test Circuit and Waveforms

Figure 5. AC Test Circuit

Figure 6. Waveforms for /RST1 Output
Physical Dimensions

2X 0.05 C 1.45

B

2X 0.05 C

(0.254)

1.00

A

TOP VIEW

PIN 1 IDENTIFIER

0.05

0.00

DETAIL A

0.25 6X

0.15 6X

0.55MAX

0.05 C

BOTTOM VIEW

(0.05) 6X

(0.5) 6X

0.5

0.35 5X

0.25 5X

0.40 6X

0.30 5X

0.40 30 4X

0.075 X 45° CHAMFER

DETAIL A PIN 1 TERMINAL

0.10 6X

0.00 6X

0.45

0.35

0.40

0.30

Notes:
1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994
4. FILENAME AND REVISION: MAC06AREV4
5. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

Figure 7. 6-Lead MicroPak™ 1.0 x 1.45mm, JEDEC MO-252

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FTL7522 — Low ICR Reset Timer with Fixed Delay and Reset Pulse

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PRODUCT STATUS DEFINITIONS

<table>
<thead>
<tr>
<th>Datasheet Identification</th>
<th>Product Status</th>
<th>Definition</th>
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<tbody>
<tr>
<td>Advance Information</td>
<td>Formative / In Design</td>
<td>Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.</td>
</tr>
<tr>
<td>Preliminary</td>
<td>First Production</td>
<td>Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.</td>
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<tr>
<td>No Identification Needed</td>
<td>Full Production</td>
<td>Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.</td>
</tr>
<tr>
<td>Obsolete</td>
<td>Not In Production</td>
<td>Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.</td>
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</tbody>
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