

FTCO3V455A2

3-Phase Inverter Automotive Power Module

General Description

The FTCO3V455A2 is a 40 V low $R_{ds(on)}$ automotive qualified power module featuring a 3-phase MOSFET inverter optimized for 12 V battery systems. It includes a precision shunt resistor for current sensing an NTC for temperature sensing and an RC snubber circuit.

The module utilizes ON Semiconductor's trench MOSFET technology and it is designed to provide a very compact and high performance variable speed motor drive for applications like electric power steering, electro-hydraulic power steering, electric water pumps, electric oil pumps. The power module is 100% lead free, RoHS and UL compliant.

Features

- 40 V – 150 A 3-phase Trench MOSFET Inverter Bridge
- 1% Precision Shunt Current Sensing
- Temperature Sensing
- DBC Substrate
- 100% Lead Free and RoHS Compliant 2000/53/C Directive
- UL94V-0 Compliant
- Isolation Rating of 2500 V rms/min
- Mounting Through Screws
- Automotive Qualified

Benefits

- Low Junction-sink Thermal Resistance
- Low Inverter Electrical Resistance
- High Current Handling
- Compact Motor Design
- Highly Integrated Compact Design
- Better EMC and Electrical Isolation
- Easy and Reliable Installation
- Improved Overall System Reliability

Applications

- Electric and Electro-Hydraulic Power Steering
- Electric Water Pump
- Electric Oil Pump
- Electric Fan

Flammability Information

- All Materials Present in the Power Module Meet UL Flammability Rating Class 94 V-0 or Higher.

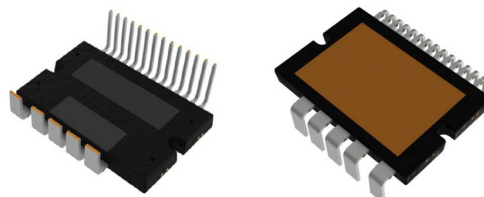
Solder

- Solder Used is a Lead Free SnAgCu Alloy.



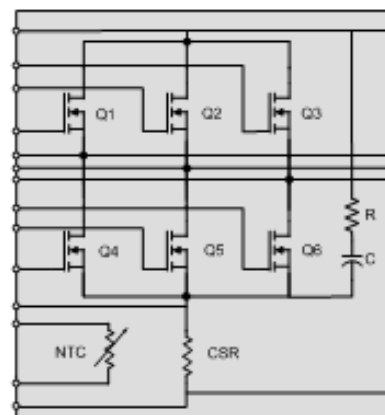
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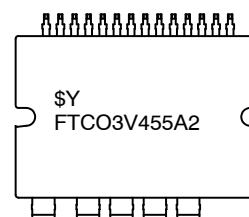


MOD-19
CASE MODCC

ELECTRICAL CONNECTION



MARKING DIAGRAM



\$Y = ON Semiconductor
FTCO3V455A2 = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

FTCO3V455A2

MAXIMUM RATINGS (T_J = 25°C, Unless Otherwise Specified)

Symbol	Parameter	Rating	Unit
V _{DS} (Q1~Q6)	Drain to Source Voltage	40	V
V _{GS} (Q1~Q6)	Gate to Source Voltage	±20	V
I _D (Q1~Q6)	Drain Current Continuous(T _C = 25°C, V _{GS} = 10V) (Note 1)	150	A
E _{AS} (Q1~Q6)	Single Pulse Avalanche Energy (Note 2)	947	mJ
P _D	Power dissipation	115	W
T _J	Maximum Junction Temperature	175	°C
T _{STG}	Storage Temperature	125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE

Symbol	Parameter	Min.	Typ.	Max.	Unit
R _{thjc} Thermal Resis- tance Junction to case, Single Inverter FET, PKG center (Note 3)	Q1 Thermal Resistance J –C	–	1.3	1.7	°C/W
	Q2 Thermal Resistance J –C	–	1.3	1.7	°C/W
	Q3 Thermal Resistance J –C	–	1.3	1.7	°C/W
	Q4 Thermal Resistance J –C	–	1.2	1.6	°C/W
	Q5 Thermal Resistance J –C	–	1.2	1.6	°C/W
	Q6 Thermal Resistance J –C	–	1.2	1.6	°C/W
T _J	Maximum Junction Temperature	–		175	°C
T _S	Operating Sink Temperature	–40		120	°C
T _{STG}	Storage Temperature	–40		125	°C

1. Max value to not exceed T_J = 175°C based on R_{thjc} thermal limitation. Defined by design, not subject to production testing.
2. Starting T_J = 25°C, V_{ds} = 20 V, I_{as} = 64 A, L = 480 μH.
3. These values are based on Thermal simulations and PV level measurements.
These values assume a single MOSFET is on, and the test condition for referenced temperature is “Package Center”.
This means that the DT is measured between the T_J of each MOSFET and the bottom surface temperature immediately under the thermal media in the center of the package.

FTCO3V455A2

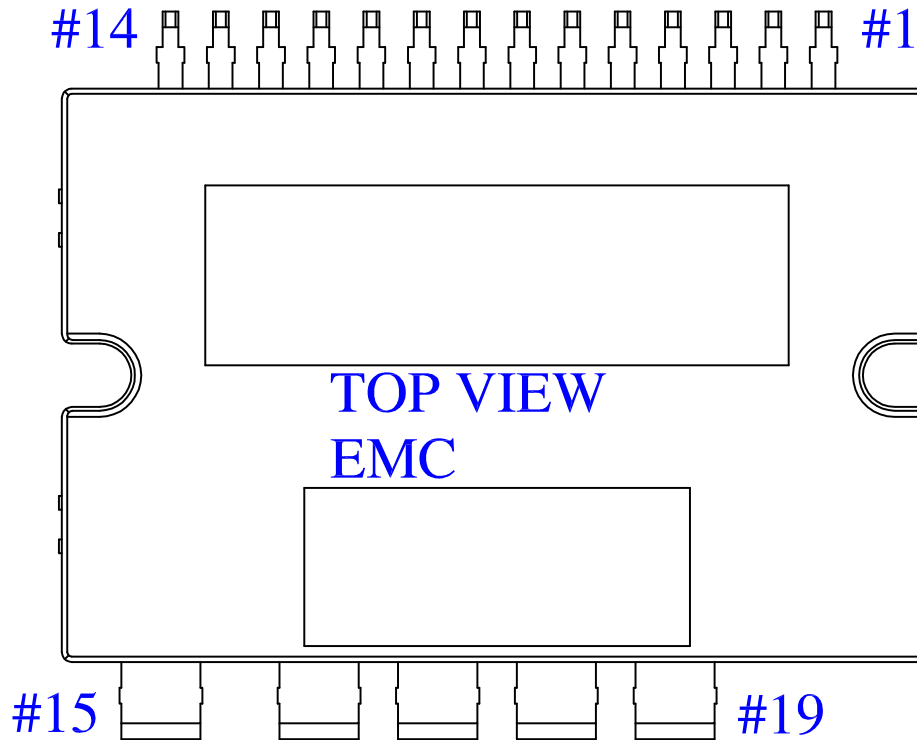


Figure 1. Pin Configuration

PIN DESCRIPTION

Pin Number	Pin Name	Pin Descriptions
1	TEMP 1	NTC Thermistor Terminal 1
2	TEMP 2	NTC Thermistor Terminal 2
3	PHASE W SENSE	Source of HS W and Drain of LS W
4	GATE HS W	Gate of HS phase W MOSFET
5	GATE LS W	Gate of LS phase W MOSFET
6	PHASE V SENSE	Source of HS V and Drain of LS V
7	GATE HS V	Gate of HS phase V MOSFET
8	GATE LS V	Gate of LS phase V MOSFET
9	PHASE U SENSE	Source of HS U and Drain of LS U
10	GATE HS U	Gate of HS phase U MOSFET
11	VBAT SENSE	Drain of HS U, V and W MOSFET
12	GATE LS U	Gate of LS phase U MOSFET
13	SHUNT P	Source of LS U, V W MOSFETS / Shunt +
14	SHUNT N	Negative shunt terminal (shunt -)
15	VBAT	Positive battery terminal
16	GND	Negative battery terminal
17	PHASE U	Motor phase U
18	PHASE V	Motor phase V
19	PHASE W	Motor phase W

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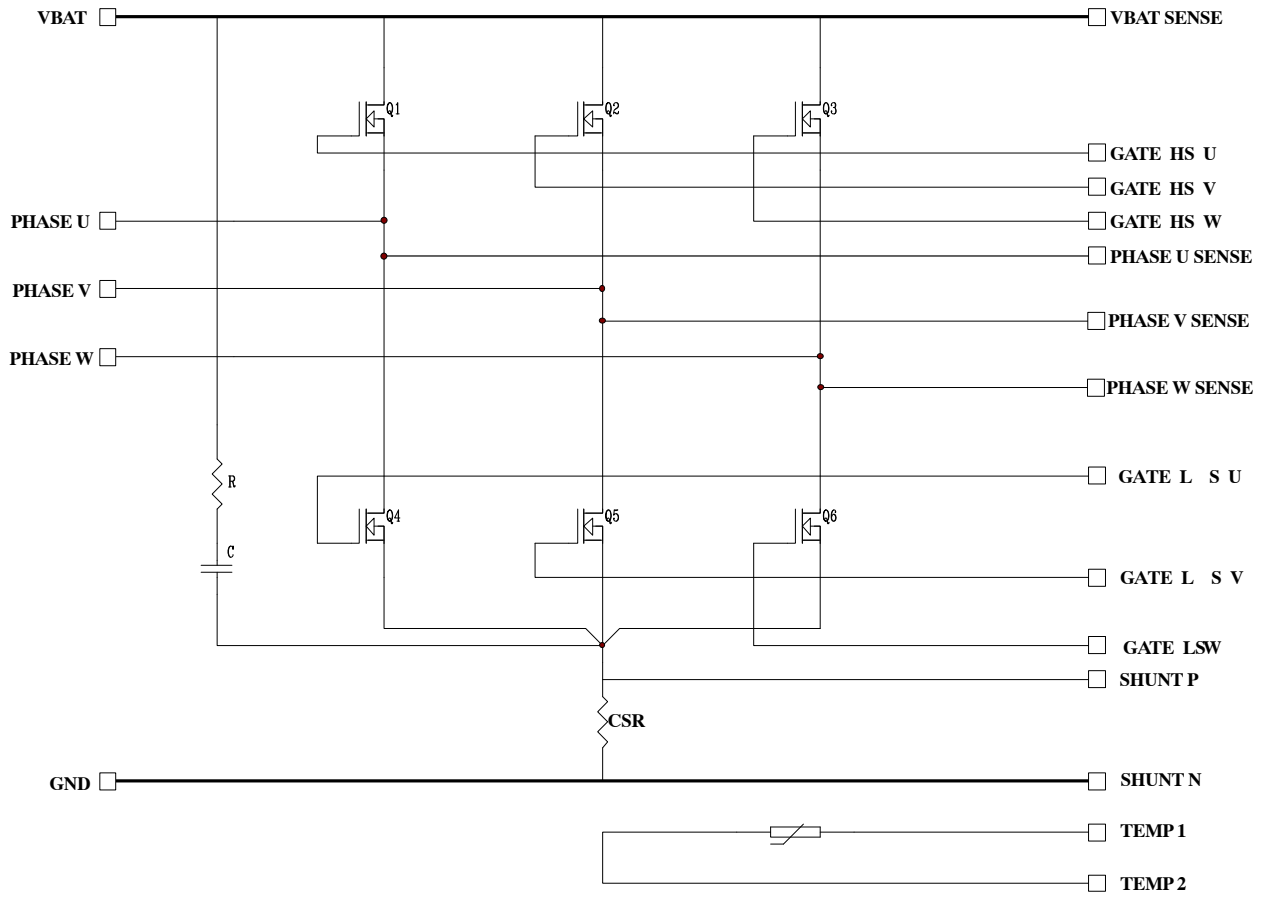


Figure 2. Internal Equivalent Circuit

FTCO3V455A2

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
BV _{DSS}	D-S Breakdown Voltage (Inverter MOSFETs)	V _{GS} =0, I _D =250uA	40	-	-	V
V _{GS}	Gate to Source Voltage (Inverter MOSFETs)		-20	-	20	V
V _{TH}	Threshold Voltage (Inverter MOSFETs)	V _{GS} =V _{DS} , I _D =250uA, T _J =25 °C	2.0	2.8	4.0	V
V _{SD}	MOSFET Body Diode Forward Voltage	V _{GS} =0V, I _S =80A, T _J =25 °C		0.8	1.28	V
R _{DS(ON)Q1}	Inverter High Side MOSFETs Q1 (See Note 4)	V _{GS} =10V, I _D =80A, T _J =25 °C	-	1.15	1.66	mΩ
R _{DS(ON)Q2}	Inverter High Side MOSFETs Q2 (See Note 4)	V _{GS} =10V, I _D =80A, T _J =25 °C	-	1.22	1.73	mΩ
R _{DS(ON)Q3}	Inverter High Side MOSFETs Q3 (See Note 4)	V _{GS} =10V, I _D =80A, T _J =25 °C	-	1.31	1.82	mΩ
R _{DS(ON)Q4}	Inverter Low Side MOSFETs Q4 (See Note 4)	V _{GS} =10V, I _D =80A, T _J =25 °C	-	1.36	1.87	mΩ
R _{DS(ON)Q5}	Inverter Low Side MOSFETs Q5 (See Note 4)	V _{GS} =10V, I _D =80A, T _J =25 °C	-	1.57	2.08	mΩ
R _{DS(ON)Q6}	Inverter Low Side MOSFETs Q6 (See Note 4)	V _{GS} =10V, I _D =80A, T _J =25 °C	-	1.86	2.32	mΩ
I _{DSS}	Inverter MOSFETs (UH,UL,VH,VL,WH,WL)	V _{GS} =0V, V _{DS} =32V, T _J =25 °C	-	-	1.0	μA
I _{GSS}	Inverter MOSFETs Gate to Source Leakage Current	V _{GS} =±20V	-	-	±100	nA
Total loop resistance VLINK(+) - V0 (-)		V _{GS} =10V, I _D =80A, T _J =25 °C	-	4.69	5.5	mΩ

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz	-	15000	-	pF
C _{oss}	Output Capacitance		-	1250	-	pF
C _{rss}	Reverse Transfer Capacitance		-	685	-	pF
R _G	Gate Resistance	V _{GS} = 0.5 V, f = 1 MHz	-	1.1	-	Ω
Q _{g(TOT)}	Total Gate Charge at 10 V	V _{GS} = 0 to 10 V, V _{DD} = 20 V, I _D = 35 A, I _g = 1 mA	-	215	280	nC
Q _{g(TH)}	Threshold Gate Charge	V _{GS} = 0 to 2 V, V _{DD} = 20 V, I _D = 35 A, I _g = 1 mA	-	29	38	nC
Q _{gs}	Gate to Source Gate Charge	V _{DD} = 20 V, I _D = 35 A, I _g = 1 mA	-	60	-	nC
Q _{gs2}	Gate Charge Threshold to Plateau		-	32	-	nC
Q _{gd}	Gate to Drain "Miller" Charge		-	49	-	nC

TEMPERATURE SENSE (NTC Thermistor)

Symbol	Test Conditions	Test Time	Min	Typ	Max	Unit
Voltage	Current = 1 mA, Temperature = 25 °C	T = 0.5 ms	7.5	-	12	V

CURRENT SENSE RESISTOR

Symbol	Test Conditions	Test Time	Min	Typ	Max	Unit
Resistance	Current Sense resistor current = 80 A	T = 0.5 ms	0.46	-	0.53	mΩ

TYPICAL CHARACTERISTICS

(Generated using MOSFETs assembled in a TO263 package, for reference purposes only.)

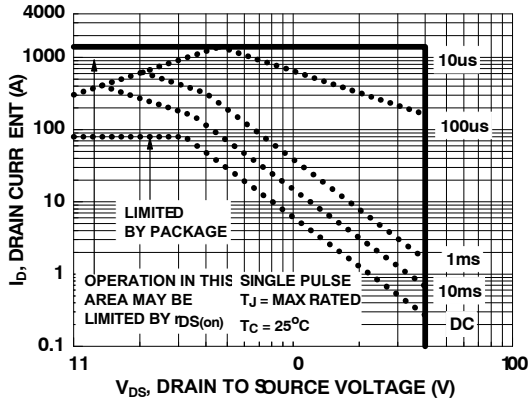
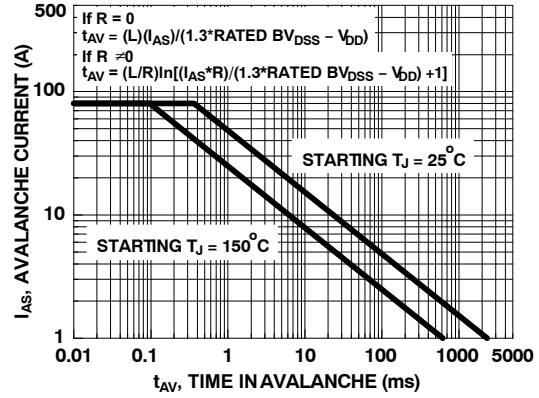


Figure 3. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515
 Figure 4. Unclamped Inductive Switching Capability

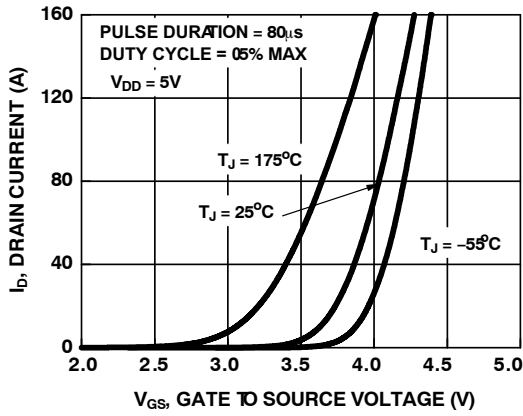


Figure 5. Transfer Characteristics

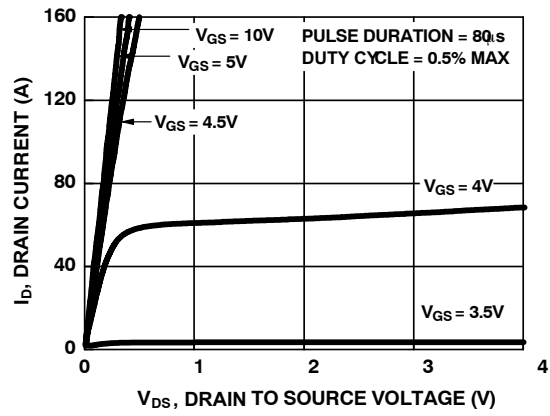


Figure 6. Saturation Characteristics

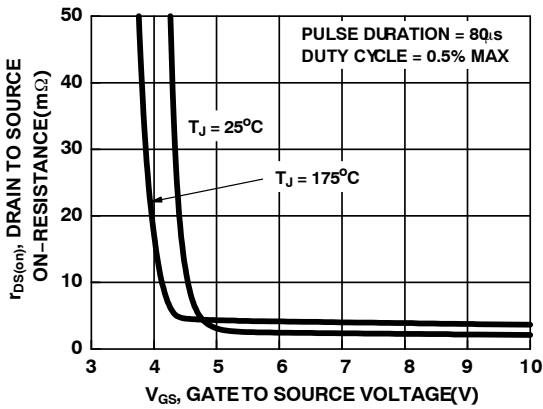


Figure 7. Drain to Source On-Resistance Variation vs Gate to Source Voltage

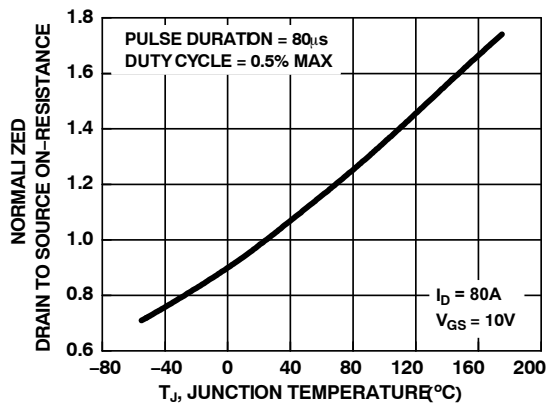


Figure 8. Normalized Drain to Source On Resistance vs Junction Temperature

FTCO3V455A2

TYPICAL CHARACTERISTICS

(Generated using MOSFETs assembled in a TO263 package, for reference purposes only.)

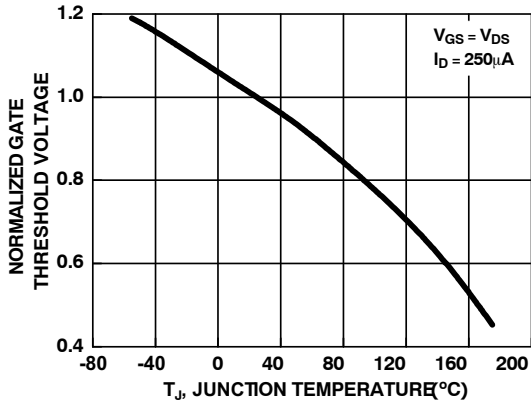


Figure 9. Normalized Gate Threshold Voltage vs Junction Temperature

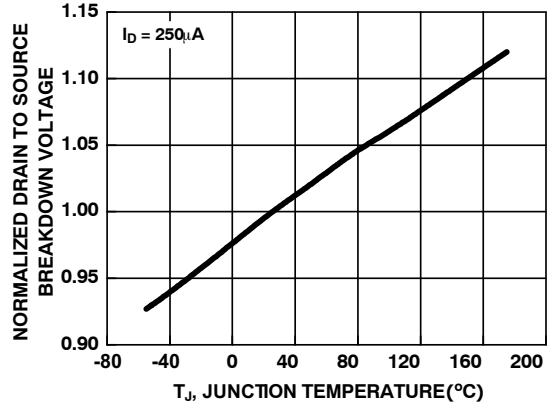


Figure 10. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

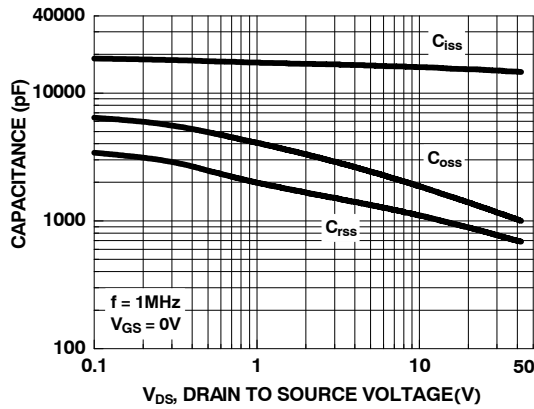


Figure 11. Capacitance vs Drain to Source Voltage

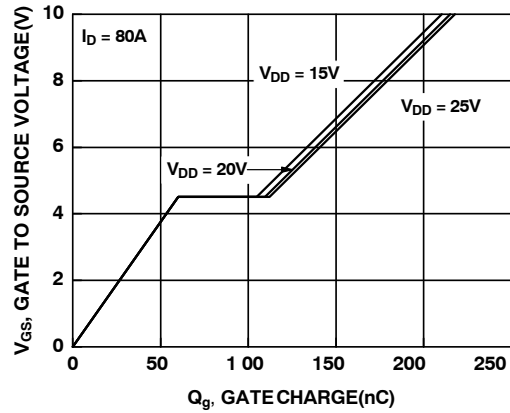
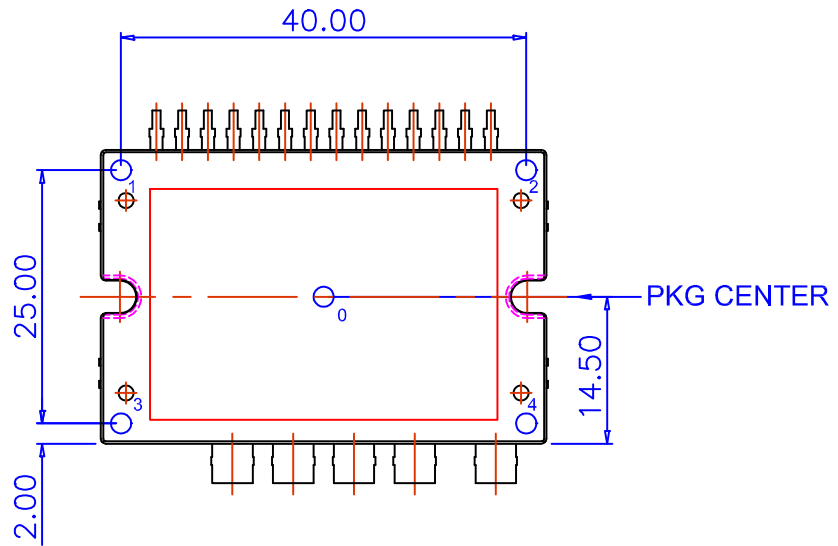


Figure 12. Gate Charge vs Gate to Source Voltage

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition	Limits			Unit
		Min	Typ	Max	
Device Flatness	Note Fig. 15	0	-	+150	µm
Mounting Torque	Mounting Screw: - M3, Recommended 0.7 N.m	0.6	0.7	0.8	N.m
Weight		-	20	-	g

FTCO3V455A2



FLATNESS : MAX. 150um

-. MEASURING AT INDICATING POINTS
1, 2, 3, AND 4 (BASED ON "0")

ORDERING INFORMATION

Device Marking	Packing Type	Quantity
FTCO3V455A2	Tube	11

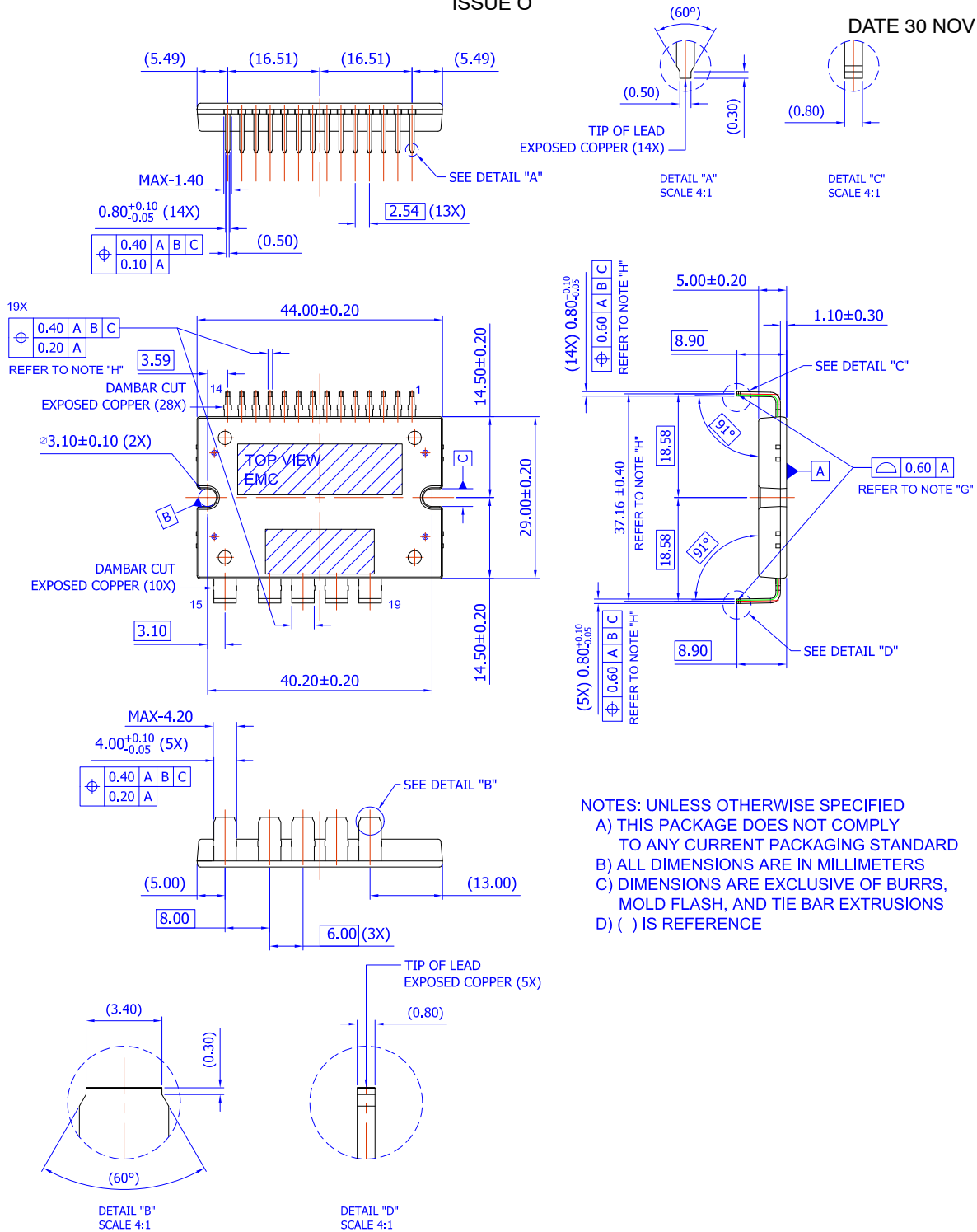
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19LD APM PDD STD CASE MODCC ISSUE O

DATE 30 NOV 2016



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