16-Bit to 32-Bit Multiplexer/ Demultiplexer Bus Switch with -2 V Undershoot Protection

FSTU32160

ON Semiconductor®

www.onsemi.com

TSSOP56 14x6.1
CASE 948BR

General Description

The ON Semiconductor Switch FSTU32160 is a 16−bit to 32−bit highspeed CMOS TTL−compatible multiplexer/demultiplexer bus switch. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device can be used in applications where two buses need to be addressed simultaneously. The FSTU32160 is designed so that the A Port demultiplexes into B_1 or B_2 or both. The A and B Ports have “undershoot hardened” circuit protection to support an extended range to 2.0 V below ground. The integrated Undershoot Hardened Circuit senses undershoot at the I/O’s, and responds by preventing voltage differentials from developing and turning on the switch.

Two select (S_1, S_2) inputs provide switch enable control. When S_1, S_2 are HIGH, the device precharges the B Port to a selectable bias voltage (Bias V) to minimize live insertion noise.

Features

- Undershoot hardened to −2 V (A and B Ports)
- Slower Output Enable Times prevent Signal Disruption
- 4 Ω Switch Connection between Two Ports
- Minimal Propagation Delay through the Switch
- Low I_{CC}
- Zero Bounce in Flow−through Mode
- Control Inputs Compatible with TTL Level
- See Application Note AN−5008 for Details
- This Device is Pb−Free and is RoHS Compliant

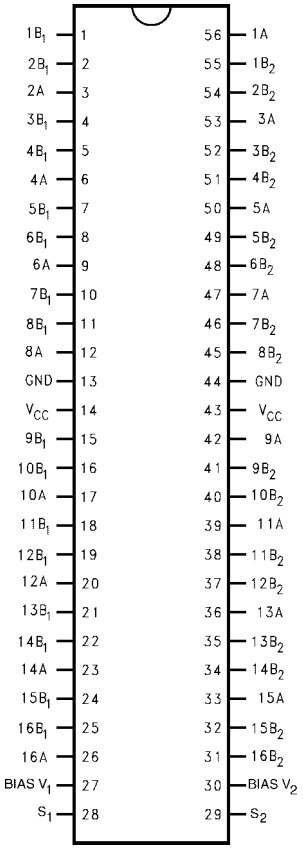
PIN DESCRIPTIONS

Pin Name	Description
S_1, S_2	Select Inputs
A	Bus A
B_1, B_2	Bus B

TRUTH TABLE

Inputs		
S_1	S_2	Function
L	H	x A = x B_1
H	L	x A = x B_2
L	L	x A = x B_1 and x B_2
H	H	x B_1, x B_2 = BiasV

CONNECTION DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

© Semiconductor Components Industries, LLC, 2019

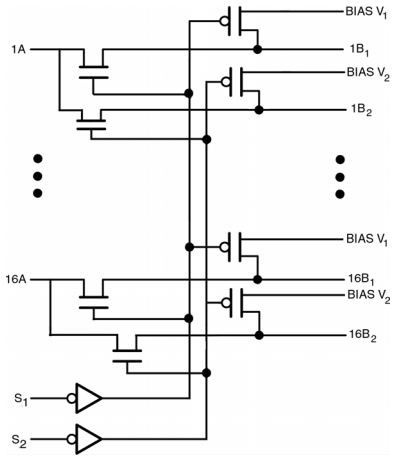


Figure 1. Logic Diagram

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Units
Supply Voltage	V_{CC}		−0.5 to 7.0	V
DC Switch Voltage	V_S	Note 1	−2.0 to 7.0	V
BiasV Voltage Range			−0.5 to 7.0	V
DC Input Control Pin Voltage	V_{IN}	Note 2	−0.5 to 7.0	V
DC Input Diode Current	I_{IK}	V_{IN} < 0 V	−50	mA
DC Output Current	I_{OUT}		128	mA
DC V_{CC}/GND Current	I_{CC}/I_{GND}		±100	mA
Storage Temperature Range	T_{STG}		−65 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. V_S is the voltage observed/applied at either the A or B Ports across the switch.
2. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

RECOMMENDED OPERATING CONDITIONS (Note 3)

Parameter	Symbol	Conditions	Rating	Units
Power Supply Operating	V_{CC}		4.0 to 5.5	V
Precharge Supply	BiasV		1.5 to V_{CC}	V
Input Voltage	V_{IN}		0 to 5.5	V
Output Voltage	V_{OUT}		0 to 5.5	V
Input Rise and Fall Time	t_r/t_f	Switch Control Input	0 to 5	ns/V
		Switch I/O	0 to DC	
Free Air Operating Temperature	T_A		−40 to 85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
3. Unused control inputs must be held HIGH or LOW. They may not float.

ORDERING INFORMATION

Part Number	Package	Shipping†
FSTU32160MTDX	TSSOP56 14x6.1, JEDEC MO−153, 6.1 mm Wide (Pb−Free)	1000 units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	T_A = −40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 4)	Max		
V_{IK}	Clamp Diode Voltage	4.5			−1.2	V	I_{IN} = −18 mA
V_{IH}	HIGH Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	μA	0 ≤ V_{IN} ≤ 5.5 V
		0			10	μA	V_{IN} = 5.5 V
I_O	Output Current	4.5	0.25			mA	BiasV = 2.4 V, S_X = 2.0 V B_X = 0
I_{OZH}, I_{OZL}	OFF−STATE Leakage Current	5.5			±1.0	μA	0 ≤ A, ≤ V_{CC}, V $BiasV_1$ = $BiasV_2$ = 5.5 V
I_{OZH}, I_{OZL}	OFF−STATE Leakage Current	5.5			±1.0	μA	0 ≤ B, ≤ V_{CC}, V $BiasV_1$ = $BiasV_2$ = FLOATING
R_{ON}	Switch On Resistance (Note 5)	4.5		4	7	Ω	V_{IN} = 0 V, I_{IN} = 64 mA
		4.5		4	7	Ω	V_{IN} = 0 V, I_{IN} = 30 mA
		4.5		8	14	Ω	V_{IN} = 2.4 V, I_{IN} = 15 mA
		4.0		11	20	Ω	V_{IN} = 2.4 V, I_{IN} = 15 mA
I_{CC}	Quiescent Supply Current	5.5			3	μA	V_{IN} = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4 V Other inputs at V_{CC} or GND
I_{BIAS}	Bias Pin Leakage Current	5.5			±1.0	μA	S_1, S_2 = 0 V B_X = 0 V, $BiasV_X$ = 5.5 V
V_{IKU}	Voltage Undershoot	5.5			−2.0	V	0.0 mA ≥ I_{IN} ≥ −50 mA S_1, S_2 = 5.5 V

4. Typical values are at V_{CC} = 5.0 V and T_A = +25°C
5. Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	T_A = −40 °C to +85 °C, C_L = 50 pF, RU = RD = 500 Ω				Units	Conditions	Figure No.
		V_{CC} = 4.5 − 5.5 V		V_{CC} = 4.0 V				
		Min	Max	Min	Max			
t_{PHL}, t_{PLH}	A or B, to B or A (Note 6)		0.25		0.25	ns	V_I = OPEN	Figures 4, 5
t_{PZH}	Output Enable Time, S to A, B	7.0	30.0		35.0	ns	V_I = OPEN for t_{PZH} BiasV = GND	Figures 4, 5
t_{PZL}	Output Enable Time, S to A, B	7.0	30.0		35.0	ns	V_I = 7 V for t_{PZL} BiasV = 3 V	Figures 4, 5
t_{PHZ}	Output Disable Time, S to A, B	1.0	6.9		7.3	ns	V_I = OPEN for t_{PHZ} BiasV = GND	Figures 4, 5
t_{PLZ}	Output Disable Time, S to A, B	1.0	7.7		7.7	ns	V_I = 7 V for t_{PLZ} BiasV = 3 V	Figures 4, 5

6. This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

CAPACITANCE (Note 7)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control pin Input Capacitance	4		pF	V_{CC} = 5.0 V
$C_{I/O\ OFF}$	Input/Output Capacitance “OFF State”	8		pF	V_{CC} = 5.0 V, Switch OFF

7. T_A = +25°C, f = 1 MHz, Capacitance is characterized but not tested.

UNDERSHOOT CHARACTERISTIC (Note 8)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OUTU}	Output Voltage During Undershoot	2.5	V_{OH} − 0.3		V	Figure 2

8. This test is intended to characterize the device’s protective capabilities by maintaining output signal integrity during an input transient voltage undershoot event.

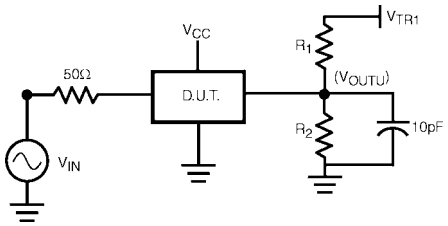


Figure 2.

DEVICE TEST CONDITIONS

Parameter	Value	Units
V_{IN}	see Waveform	V
$R_1 = R_2$	100K	Ω
V_{TRI}	11.0	V
V_{CC}	5.5	V

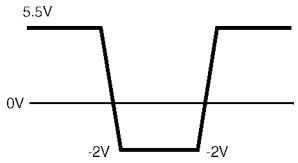
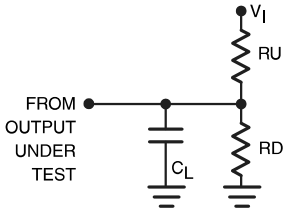


Figure 3. Transient Input Voltage (V_{IN}) Waveform

AC Loading and Waveforms



Notes:

Input driven by 50 Ω source terminated in 50 Ω.

C_L includes load and stray capacitance, C_L = 50 pF

Input PRR = 1.0 MHz, t_W = 500 ns

Figure 4. AC Test Circuit

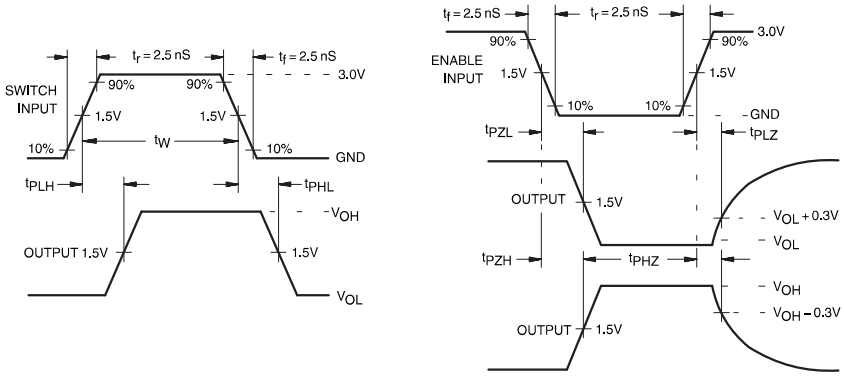
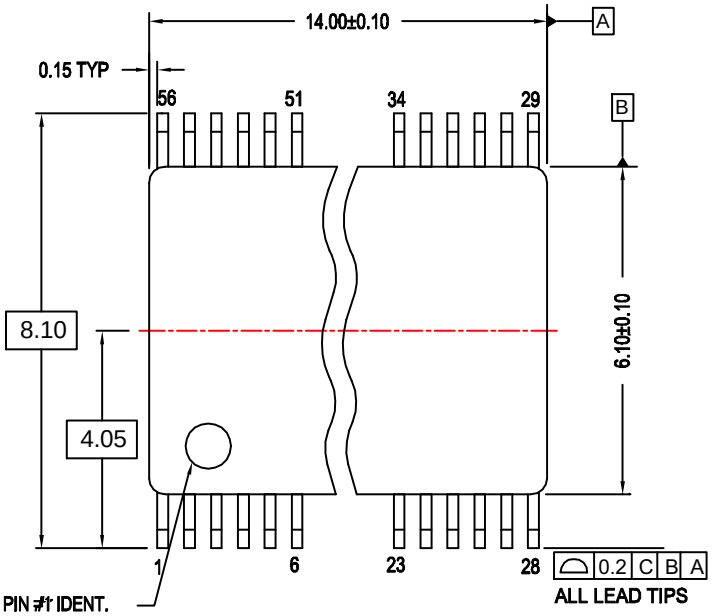
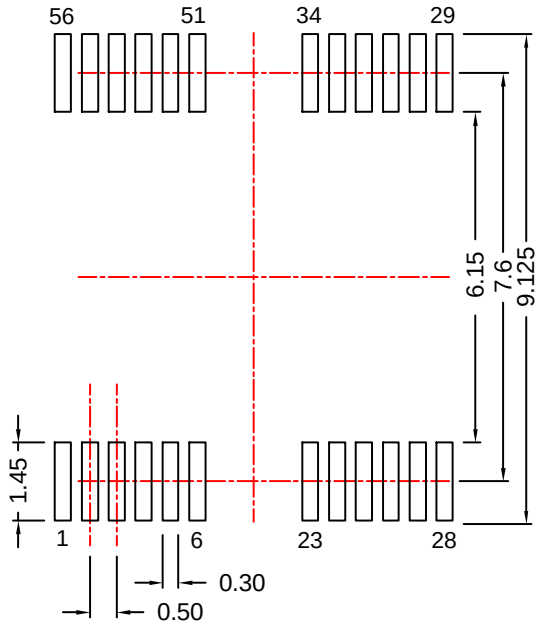


Figure 5. AC Waveforms

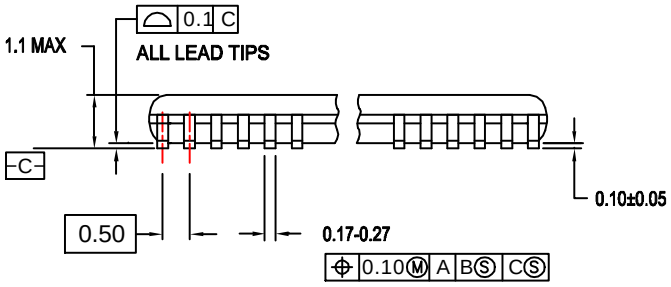
TSSOP56 14x6.1
CASE 948BR
ISSUE O

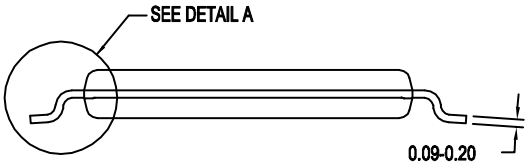
DATE 30 SEP 2016

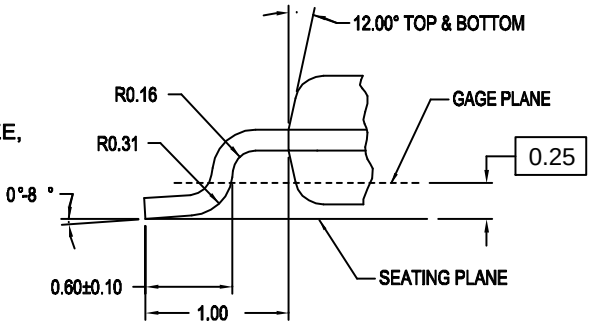




LAND PATTERN RECOMMENDATION
REFERENCE TSSOP50P810X120-56N







DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION EE, REF NOTE 6, DATE 10/97.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

DOCUMENT NUMBER:	**98AON13776G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**TSSOP56 14X6.1**	**PAGE 1 OF 1**

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales