# Green Mode Power Switch

# FSDH321, FSDL321



### Description

Each product in the FSDx321 (x for H, L) family consists of an integrated Pulse Width Modulator (PWM) and SENSEFET, and is specifically designed for high performance offline Switch Mode Power Supplies (SMPS) with minimal external components. Both devices are integrated high voltage power switching regulators which combine an avalanche rugged SENSEFET® with a current mode PWM control block. The integrated PWM controller features include: a fixed oscillator with frequency modulation for reduced EMI, Under Voltage Lock Out (UVLO) protection, Leading Edge Blanking (LEB), an optimized gate turn−on/turn−off driver, Thermal Shut Down (TSD) protection, Abnormal Over Current Protection (AOCP) and temperature compensated precision current sources for loop compensation and fault protection circuitry. When compared to a discrete MOSFET and controller or RCC switching converter solution, the FSDx321 devices reduce total component count, design size, weight while increasing efficiency, productivity and system reliability. Both devices provide a basic platform that is well suited for the design of cost−effective flyback converters.

### Features

- Internal Avalanche Rugged SENSEFET
- Consumes only 0.65 W at 240 VAC & 0.3 W Load with Advanced Burst−Mode Operation
- Frequency Modulation for EMI Reduction
- Precision Fixed Operating Frequency
- Internal Start−up Circuit
- Pulse−by−Pulse Current Limiting
- Abnormal Over Current Protection (AOCP)
- Over Voltage Protection (OVP)
- Over Load Protection (OLP)
- Internal Thermal Shutdown Function (TSD)
- Auto−Restart Mode
- Under Voltage Lockout (UVLO)
- Low Operating Current (max. 3 mA)
- Adjustable Peak Current Limit
- Built−in Soft Start

### Applications

- SMPS for STB, Low Cost DVD Player
- Auxiliary Power for PC
- Adapter & Charger

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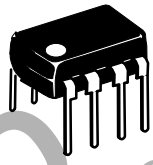
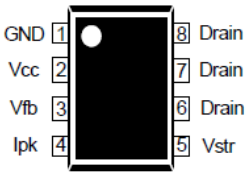


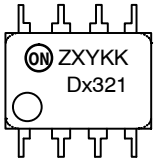
**PDIP8**
**(9.42x6.38, 2.54P)**
**CASE 646CM**

### PIN CONFIGURATION




(Top View)

### MARKING DIAGRAM




| | |
|---|---|
| Z | = Assembly Code |
| XY | = 2−digit Code (Year & Week) |
| KK | = 2−digit Die−Run Code |
| Dx321 (x=H/L) | = Specific Device Code |

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

## ORDERING INFORMATION

| Product Number | Package | Marking Code | $BV_{DSS}$ | $f_{OSC}$ | $R_{DS(ON)}$ | Shipping |
|---|---|---|---|---|---|---|
| FSDH321 | 8DIP | DH321 | 650 V | 100 KHz | 14 Ω | 3000 / Tube |
| FSDL321 | 8DIP | DL321 | 650 V | 50 KHz | 14 Ω | 3000 / Tube |

**Table 1. OUTPUT POWER TABLE**

| Product | 230VAC±15% (Note 3) | | 85−265VAC | |
|---|---|---|---|---|
| | Adapter (Note 1) | Open Frame (Note 2) | Adapter (Note 1) | Open Frame (Note 2) |
| FSDL321 | 11 W | 17 W | 8 W | 12 W |
| FSDH321 | 11 W | 17 W | 8 W | 12 W |

1. Typical continuous power in a non−ventilated enclosed adapter with sufficient drain pattern as a heat sinker, at 50°C ambient.
2. Maximum practical continuous power in an open frame design with sufficient drain pattern as a heat sinker, at 50°C ambient.
3. 230 VAC or 100/115 VAC with doubler.

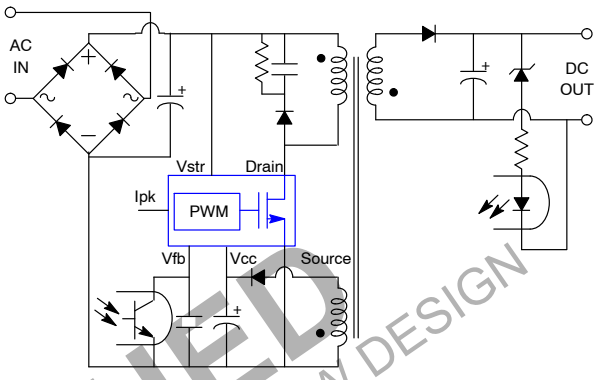



**Figure 1. Typical Flyback Application**



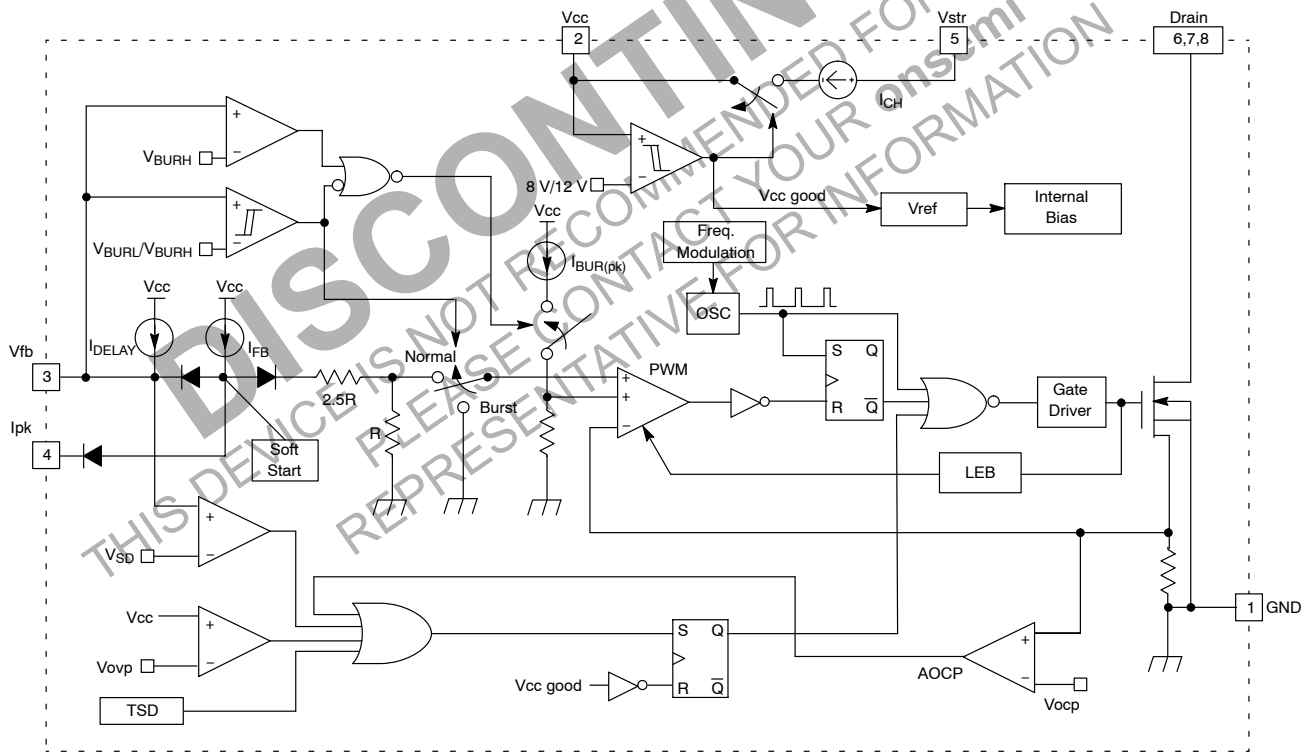



**Figure 2. Functional Block Diagram of FSDx321**

**Table 2. PIN DEFINITIONS**

| Pin Number | Pin Name | Pin Function Description |
|---|---|---|
| 1 | GND | SENSEFET source terminal on primary side and internal control ground. |
| 2 | Vcc | Positive supply voltage input. Although connected to an auxiliary transformer winding, current is supplied from pin 5 (Vstr) via an internal switch during startup (see Internal Block Diagram section). It is not until Vcc reaches the UVLO upper threshold (12 V) that the internal start−up switch opens and device power is supplied via the auxiliary transformer winding. |
| 3 | Vfb | The feedback voltage pin is the non−inverting input to the PWM comparator. It has a 0.9 mA current source connected internally while a capacitor and optocoupler are typically connected externally. A feedback voltage of 6 V triggers over load protection (OLP). There is a time delay while charging external capacitor Cfb from 3 V to 6 V using an internal 5 μA current source. This time delay prevents false triggering under transient conditions, but still allows the protection mechanism to operate under true overload conditions. |
| 4 | Ipk | This pin adjusts the peak current limit of the SENSEFET. The feedback 0.9 mA current source is diverted to the parallel combination of an internal 2.8 kΩ resistor and any external resistor to GND on this pin to determine the peak current limit. If this pin is tied to Vcc or left floating, the typical peak current limit will be 0.7 A. |
| 5 | Vstr | This pin connects directly to the rectified AC line voltage source. At start up the internal switch supplies internal bias and charges an external storage capacitor placed between the Vcc pin and ground. Once the Vcc reaches 12 V, the internal switch is opened. |
| 6, 7, 8 | Drain | The drain pins are designed to connect directly to the primary lead of the transformer and are capable of switching a maximum of 650 V. Minimizing the length of the trace connecting these pins to the transformer will decrease leakage inductance. |

**ABSOLUTE MAXIMUM RATINGS** (Ta = 25°C, unless otherwise specified)

| Symbol | Parameter | Ratings | Unit |
|---|---|---|---|
| $V_{DRAIN}$ | Drain Pin Voltage | 650 | V |
| $V_{STR}$ | Vstr Pin Voltage | 650 | V |
| $V_{DG}$ | Drain−Gate Voltage | 650 | V |
| $V_{GS}$ | Gate−Source Voltage | ±20 | V |
| $I_{DM}$ | Drain Current Pulsed (Note 4) | 1.5 | A |
| $I_D$ | Continuous Drain Current ($T_C$ = 25°C) | 0.7 | A |
| | Continuous Drain Current ($T_C$ = 100°C) | 0.32 | |
| $E_{AS}$ | Single Pulsed Avalanche Energy (Note 5) | 10 | mJ |
| $V_{CC}$ | Supply Voltage | 20 | V |
| $V_{FB}$ | Feedback Voltage Range | −0.3 to $V_{CC}$ | V |
| $P_D$ | Total Power Dissipation | 1.40 | W |
| $T_J$ | Operating Junction Temperature | Internally limited | °C |
| $T_A$ | Operating Ambient Temperature | −25 to 85 | °C |
| $T_{STG}$ | Storage Temperature | −55 to 150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. Repetitive rating: Pulse width is limited by maximum junction temperature
5. L = 24 mH, $T_J$ = 25°C

**THERMAL CHARACTERISTICS** (Ta = 25°C, unless otherwise specified)

| Symbol | Parameter | Ratings | Unit |
|---|---|---|---|
| **8DIP** | | | |
| $\theta_{JA}$ | Junction−to−Ambient Thermal (Note 6) | 88.84 | °C/W |
| $\theta_{JC}$ | Junction−to−Case Thermal (Note 7) | 13.94 | °C/W |

NOTE: All items are tested with the standards JESD 51−2 and 51−10 (DIP).

6. Free standing with no heatsink; without copper clad
   Measurement condition: Just before junction temperature $T_J$ enters into OTP
7. Measured on the DRAIN pin close to plastic interface

**ELECTRICAL CHARACTERISTICS** (Ta = 25°C unless otherwise noted)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **SENSEFET SECTION** | | | | | | |
| $I_{DSS}$ | Zero−Gate Voltage Drain Current | $V_{DS}$ = 650 V, $V_{GS}$ = 0 V | – | – | 25 | μA |
| | | $V_{DS}$ = 520 V, $V_{GS}$ = 0 V, $T_C$ = 125°C | – | – | 200 | μA |
| $R_{DS(ON)}$ | Drain−Source On−State Resistance | $V_{GS}$ = 10 V, $I_D$ = 0.5 A | – | 14 | 19 | Ω |
| $g_{fs}$ | Forward Trans−Conductance (Note 8) | $V_{DS}$ = 50 V, $I_D$ = 0.5 A | 1.0 | 1.3 | – | S |
| $C_{ISS}$ | Input Capacitance | $V_{GS}$ = 0 V, $V_{DS}$ = 25 V, f = 1 MHz | – | 162 | – | pF |
| $C_{OSS}$ | Output Capacitance | | – | 18 | – | |
| $C_{RSS}$ | Reverse Transfer Capacitance | | – | 3.8 | – | |
| $t_{d(on)}$ | Turn−On Delay Time | $V_{DS}$ = 325 V, $I_D$ = 1.0 A | – | 9.5 | – | ns |
| $t_r$ | Rise Time | | – | 19 | – | |
| $t_{d(off)}$ | Turn−Off Delay Time | | – | 33 | – | |
| $t_f$ | Fall Time | | – | 42 | – | |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 10 V, $I_D$ = 1.0 A, $V_{DS}$ = 325 V | – | 7.0 | – | nC |
| $Q_{gs}$ | Gate−Source Charge | | – | 3.1 | – | |
| $Q_{gd}$ | Gate−Drain (Miller) Charge | | – | 0.4 | – | |
| **CONTROL SECTION** | | | | | | |
| $f_{OSC}$ | Switching Frequency | **FSDH321** | 90 | 100 | 110 | KHz |
| $\Delta f_{MOD}$ | Switching Frequency Modulation | | ±2.5 | ±3.0 | ±3.5 | |
| $f_{OSC}$ | Switching Frequency | **FSDL321** | 45 | 50 | 55 | KHz |
| $\Delta f_{MOD}$ | Switching Frequency Modulation | | ±1.0 | ±1.5 | ±2.0 | |
| $\Delta f_{OSC}$ | Switching Frequency Variation (Note 9) | −25°C ≤ Ta ≤ 85°C | – | ±5 | ±10 | % |
| $D_{MAX}$ | Maximum Duty Cycle | **FSDH321** | 62 | 67 | 72 | % |
| | | **FSDL321** | 71 | 77 | 83 | |
| $V_{START}$ | UVLO Threshold Voltage | $V_{FB}$ = GND | 11 | 12 | 13 | V |
| $V_{STOP}$ | | $V_{FB}$ = GND | 7 | 8 | 9 | |
| $I_{FB}$ | Feedback Source Current | $V_{FB}$ = GND | 0.7 | 0.9 | 1.1 | mA |
| $t_{S/S}$ | Internal Soft Start Time | $V_{FB}$ = 4 V | 10 | 15 | 20 | ms |
| **BURST MODE SECTION** | | | | | | |
| $V_{BURH}$ | Burst Mode Voltage | $T_J$ = 25°C | 0.4 | 0.5 | 0.6 | V |
| $V_{BURL}$ | | $T_J$ = 25°C | 0.25 | 0.35 | 0.45 | V |
| $V_{BUR(HYST)}$ | | Hysteresis | – | 150 | – | mV |
| **PROTECTION SECTION** | | | | | | |
| $I_{LIM}$ | Peak Current Limit | $T_J$ = 25°C, $\Delta i/\Delta t$ = 250 mA/μs | 0.6 | 0.7 | 0.8 | A |
| $t_{CLD}$ | Current Limit Delay Time (Note 10) | $T_J$ = 25°C | – | 600 | – | ns |
| $T_{SD}$ | Thermal Shutdown Temperature (Note 10) | | 125 | 140 | – | °C |
| $V_{SD}$ | Shutdown Feedback Voltage | | 5.5 | 6.0 | 6.5 | V |
| $V_{OVP}$ | Over Voltage Protection | | 18 | 19 | 20 | V |
| $I_{DELAY}$ | Shutdown Delay Current | $V_{FB}$ = 4 V | 3.5 | 5.0 | 6.5 | μA |
| $t_{LEB}$ | Leading Edge Blanking Time | | 200 | – | – | ns |

**ELECTRICAL CHARACTERISTICS** (Ta = 25°C unless otherwise noted) (continued)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **TOTAL DEVICE SECTION** | | | | | | |
| $I_{OP}$ | Operating Supply Current (control part only) | $V_{CC}$ = 14 V, $V_{FB}$ = 0 V | 1 | 3 | 5 | mA |
| $I_{CH}$ | Start−Up Charging Current | $V_{CC}$ = 0 V | 0.7 | 0.85 | 1.0 | mA |
| $V_{STR}$ | Vstr Supply Voltage | $V_{CC}$ = 0 V | 35 | − | − | V |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Pulse test: Pulse width ≤ 300us, duty ≤ 2%
9. These parameters, although guaranteed, are tested in EDS (wafer test) process
10. These parameters, although guaranteed, are not 100% tested in production

**Table 3. COMPARISON BETWEEN FSDM311 AND FSDx321**

| Function | FSDM311 | FSDx321 | FSDx321 Advantages |
|---|---|---|---|
| Soft−Start | 15 ms | 15 ms | (same for both devices)<br>• Gradually increasing current limit during soft−start further reduces peak current and voltage stresses<br>• Eliminates external components used for soft−start in most applications<br>• Reduces or eliminates output overshoot |
| External Current Limit | not applicable | Programmable of default current limit | • Smaller transformer<br>• Allows power limiting (constant over−load power)<br>• Allows use of larger device for lower losses and higher efficiency |
| Frequency Modulation | not applicable | ±3.0 KHz @ 100 KHz<br>±1.5 KHz @ 50 KHz | • Reduces conducted EMI |
| Burst Mode Operation | Built into controller | Built into controller | (same for both devices)<br>• Improves light load efficiency<br>• Reduces power consumption at no−load<br>• Transformer audible noise reduction |
| Drain Creepage at Package | 7.62 mm | 7.62 mm | (same for both devices)<br>• Greater immunity to arcing provoked by dust, debris and other contaminants |

## Typical Performance Characteristics (Control Part)

(These characteristic graphs are normalized at Ta = 25°C)

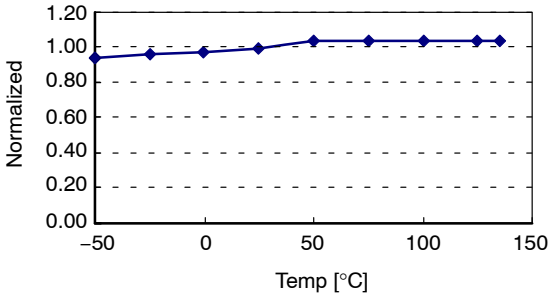



**Figure 3. Operating Frequency (Fosc) vs. Ta**

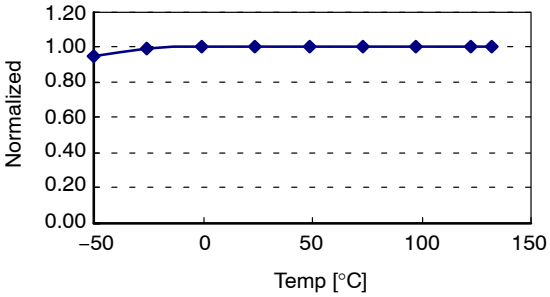



**Figure 4. Frequency Modulation ($\Delta F_{MOD}$) vs. Ta**

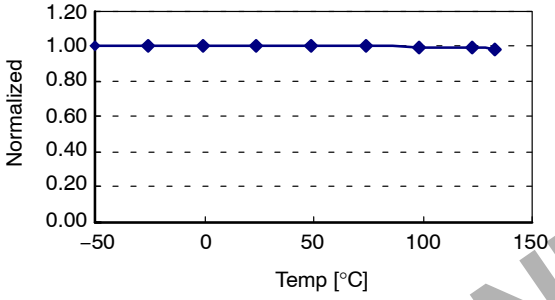



**Figure 5. Maximum Duty Cycle ($D_{MAX}$) vs. Ta**

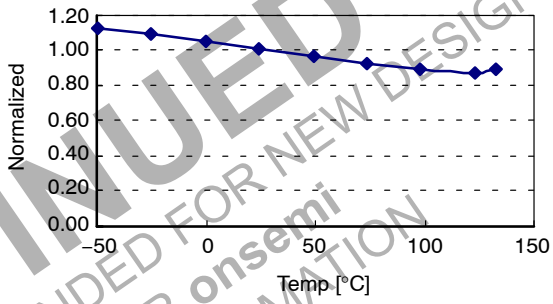



**Figure 6. Operating Supply Current ($I_{OP}$) vs. Ta**

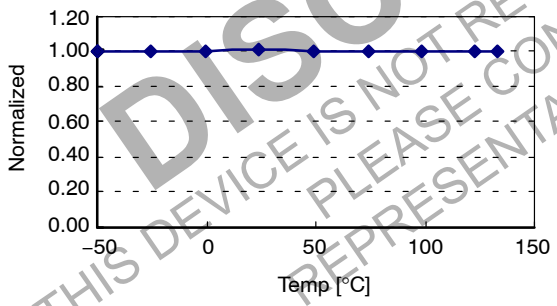



**Figure 7. Start Threshold Voltage ($V_{START}$) vs. Ta**

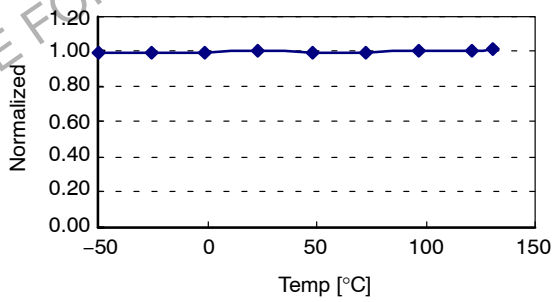



**Figure 8. Stop Threshold Voltage ($V_{STOP}$) vs. Ta**

## Typical Performance Characteristics (Control Part) (continued)

(These characteristic graphs are normalized at Ta = 25°C)

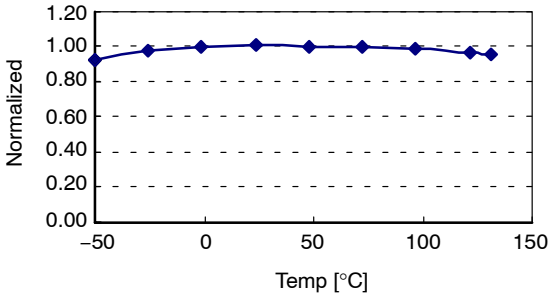



**Figure 9. Feedback Source Current ($I_{FB}$) vs. Ta**

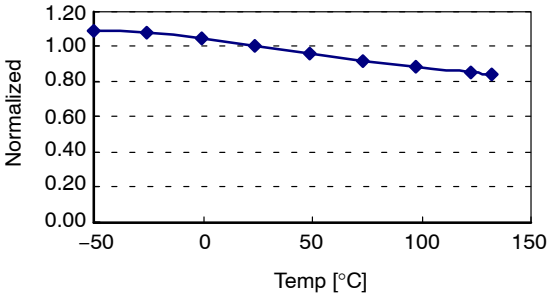



**Figure 10. Start Up Charging Current ($I_{CH}$) vs. Ta**

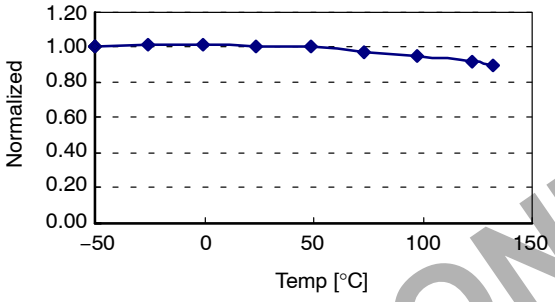



**Figure 11. Peak Current Limit ($I_{LIM}$) vs. Ta**

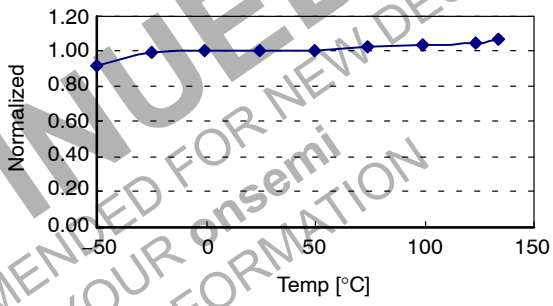



**Figure 12. Burst Peak Current ($I_{BUR(pk)}$) vs. Ta**

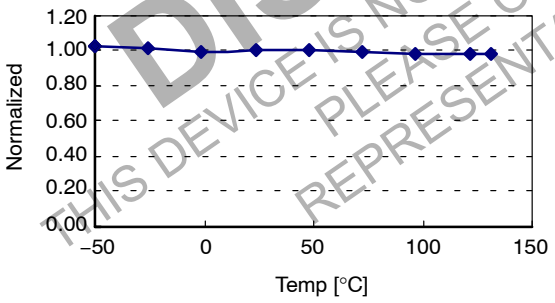



**Figure 13. Over Voltage Protection ($V_{OVP}$) vs. Ta**

## FUNCTIONAL DESCRIPTION

### Startup

In previous generations of Power Switches the Vstr pin had an external resistor to the DC input voltage line. In this generation the startup resistor is replaced by an internal high voltage current source and a switch that shuts off when 15 ms goes by after the supply voltage, Vcc, gets above 12 V. The source turns back on if Vcc drops below 8 V.

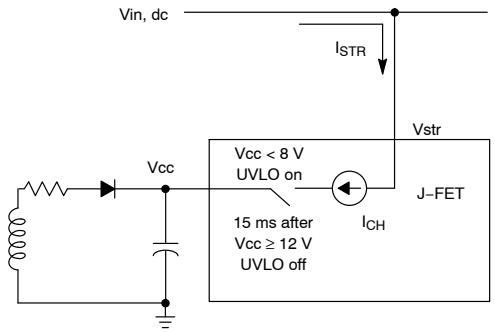



**Figure 14. High Voltage Current Source**

### Feedback Control

The FSDx321 employs current mode control, as shown in Figure 15. An opto−coupler (such as the H11A817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the Rsense resistor plus an offset voltage makes it possible to control the switching duty cycle. When the KA431 reference pin voltage exceeds the internal reference voltage of 2.5 V, the optocoupler LED current increases, the feedback voltage Vfb is pulled down and it reduces the duty cycle. This event typically happens when the input voltage is increased or the output load is decreased.

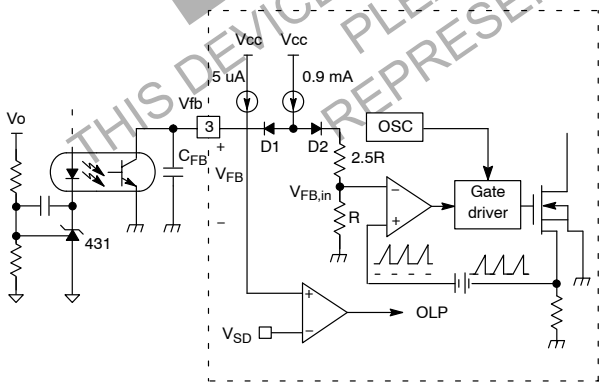



**Figure 15. Pulse Width Modulation (PWM) Circuit**

### Leading Edge Blanking (LEB)

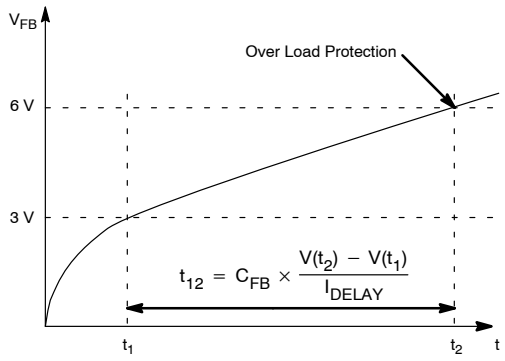
At the instant the internal SENSEFET is turned on, the primary side capacitance and secondary side rectifier diode reverse recovery typically cause a high current spike through the SENSEFET. Excessive voltage across the Rsense resistor leads to incorrect feedback operation in the current mode PWM control. To counter this effect, the power switch employs a leading edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time ($t_{LEB}$) after the SENSEFET is turned on.

### Protection Circuits

The power switch has several protective functions such as over load protection (OLP), over voltage protection (OVP), abnormal over current protection (AOCP), under voltage lock out (UVLO) and thermal shutdown (TSD). Because these protection circuits are fully integrated inside the IC without external components, the reliability is improved without increasing cost. Once a fault condition occurs, switching is terminated and the SENSEFET remains off. This causes Vcc to fall. When Vcc reaches the UVLO stop voltage $V_{STOP}$ (8 V), the protection is reset and the internal high voltage current source charges the Vcc capacitor via the Vstr pin. When Vcc reaches the UVLO start voltage $V_{START}$ (12 V), the power switch resumes its normal operation. In this manner, the auto−restart can alternately enable and disable the switching of the power SENSEFET until the fault condition is eliminated.

*Over Load Protection (OLP)*

Overload is defined as the load current exceeding a pre−set level due to an unexpected event. In this situation, the protection circuit should be activated in order to protect the SMPS. However, even when the SMPS is operating normally, the over load protection (OLP) circuit can be activated during the load transition. In order to avoid this undesired operation, the OLP circuit is designed to be activated after a specified time to determine whether it is a transient situation or an overload situation. In conjunction with the Ipk current limit pin (if used) the current mode feedback path would limit the current in the SENSEFET when the maximum PWM duty cycle is attained. If the output consumes more than this maximum power, the output voltage (Vo) decreases below its rating voltage. This reduces the current through the opto−coupler LED, which also reduces the opto−coupler transistor current, thus increasing the feedback voltage ($V_{FB}$). If $V_{FB}$ exceeds 3 V, the feedback input diode is blocked and the 5 μA current source ($I_{DELAY}$) starts to charge Cfb slowly up to Vcc. In this condition, $V_{FB}$ increases until it reaches 6 V, when the switching operation is terminated as shown in Figure 16. The shutdown delay time is the time required to charge Cfb from 3 V to 6 V with 5 μA current source.




$$t_{12} = C_{FB} \times \frac{V(t_2) - V(t_1)}{I_{DELAY}} ; I_{DELAY} = 5\ \mu A, V(t_1) = 3\ V, V(t_2) = 6\ V$$

**Figure 16. Over Load Protection (OLP)**

*Thermal Shutdown (TSD)*

The SENSEFET and the control IC are integrated, making it easier for the control IC to detect the temperature of the SENSEFET. When the temperature exceeds approximately 145°C, thermal shutdown is activated.

*Abnormal Over Current Protection (AOCP)*

Even though the power switch has OLP (Over Load Protection) and current mode PWM feedback, these are not enough to protect the power switch when a secondary side diode short or a transformer pin short occurs. In addition to start−up, soft−start is also activated at each restart attempt during auto−restart and when restarting after latch mode is activated. The power switch has an internal AOCP (Abnormal Over Current Protection) circuit, as shown in Figure 17. When the gate turn−on signal is applied to the power SENSEFET, the AOCP block is enabled and monitors the current through the sensing resistor. The voltage across the resistor is then compared with a preset AOCP level. If the sensing resistor voltage is greater than the AOCP level, pulse−by−pulse AOCP is triggered regardless of uncontrollable LEB time. Here, pulse−by−pulse AOCP stops the SENSEFET within 350 ns after it is activated.

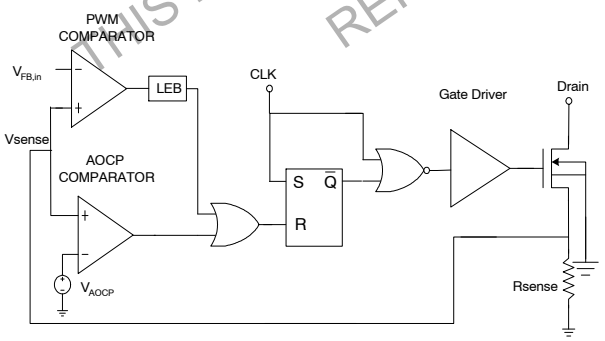



**Figure 17. Abnormal Over Current Protection (AOCP)**

*Over Voltage Protection (OVP)*

In the event of a malfunction in the secondary side feedback circuit, or an open feedback loop caused by a soldering defect, the current through the opto−coupler transistor becomes almost zero (refer to Figure 15). Then, $V_{FB}$ climbs up in a similar manner to the over load situation, forcing the preset maximum current to be supplied to the SMPS until the over load protection is activated. Because excess energy is provided to the output, the output voltage may exceed the rated voltage before the over load protection is activated, resulting in the breakdown of the devices in the secondary side. In order to prevent this situation, an over voltage protection (OVP) circuit is employed. In general, $V_{CC}$ is proportional to the output voltage and the power switch uses $V_{CC}$ instead of directly monitoring the output voltage. If $V_{CC}$ exceeds 19 V, OVP circuit is activated resulting in termination of the switching operation. In order to avoid undesired activation of OVP during normal operation, Vcc should be properly designed to be below 19 V.

### Soft Start

The power switch has an internal soft start circuit that slowly increases the feedback voltage together with the SENSEFET current after it starts up. The typical soft start time is 15 ms, as shown in Figure 18, where progressive increments of the SENSEFET current are allowed during the start−up phase. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. It also helps to prevent transformer saturation and reduce the stress on the secondary diode.

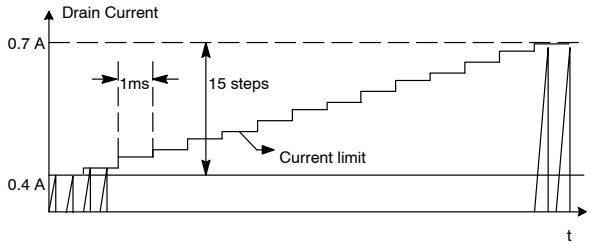



**Figure 18. Soft Start Function**

### Burst Operation

In order to minimize power dissipation in standby mode, the power switch enters burst mode operation. As the load decreases, the feedback voltage decreases. As shown in Figure 19, the device automatically enters burst mode when the feedback voltage drops below $V_{BURH}$ (500 mV). Switching still continues but the current limit is set to a fixed limit internally to minimize flux density in the transformer. The fixed current limit is larger than that defined by $V_{FB}$ = $V_{BURH}$ and therefore, $V_{FB}$ is driven down further. Switching continues until the feedback voltage drops below $V_{BURL}$ (350 mV). At this point switching stops and the

output voltages start to drop at a rate dependent on the standby current load. This causes the feedback voltage to rise. Once it passes $V_{BURH}$, switching resumes. The feedback voltage then falls and the process repeats. Burst mode operation alternately enables and disables switching of the Sense FET and reduces switching loss in Standby mode.

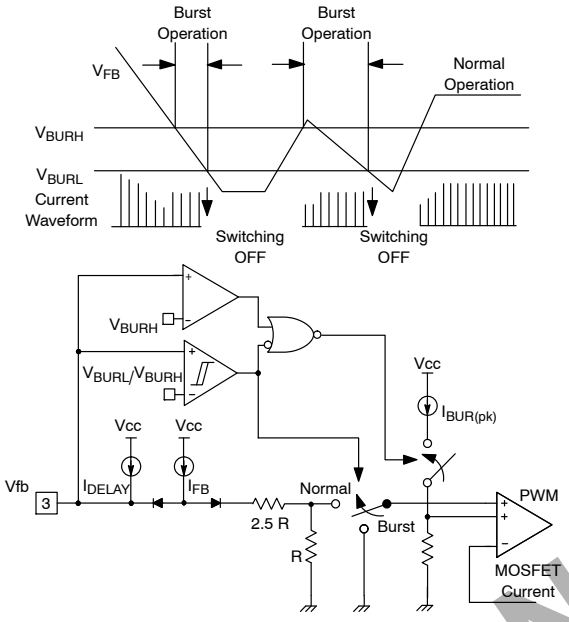



**Figure 19. Burst Operation Function**

### Frequency Modulation

Modulating the switching frequency of a switched power supply can reduce EMI. Frequency modulation can reduce EMI by spreading the energy over a wider frequency range than the bandwidth measured by the EMI test equipment. The amount of EMI reduction is directly related to the depth of the reference frequency. As can be seen in Figure 20, the frequency changes from 97 KHz to 103 KHz in 4 ms for the FSDH321 (48.5 KHz to 51.5 KHz for FSDL321). Frequency modulation allows the use of a cost effective inductor instead of an AC input mode choke to satisfy the requirements of world wide EMI limits.

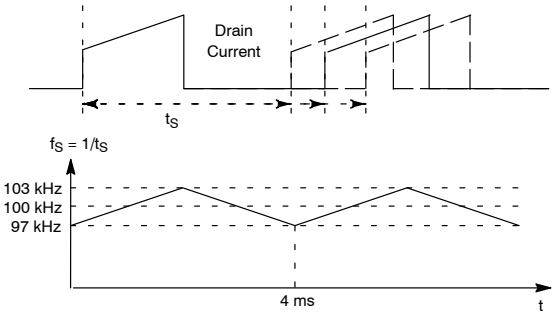



**Figure 20. Frequency Modulation Waveform**

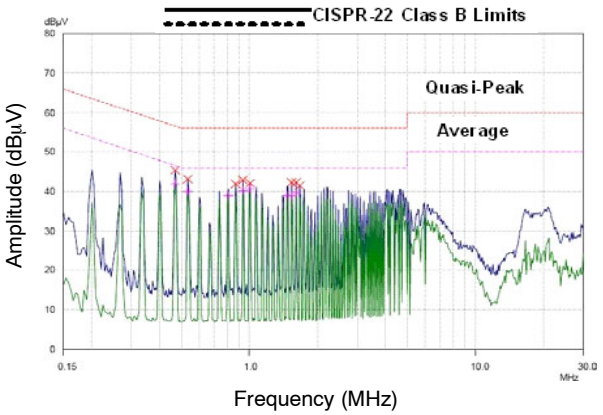



**Figure 21. KA5−series Power Switch Full Range EMI Scan (67 KHz, no Frequency Modulation) with DVD Player SET**

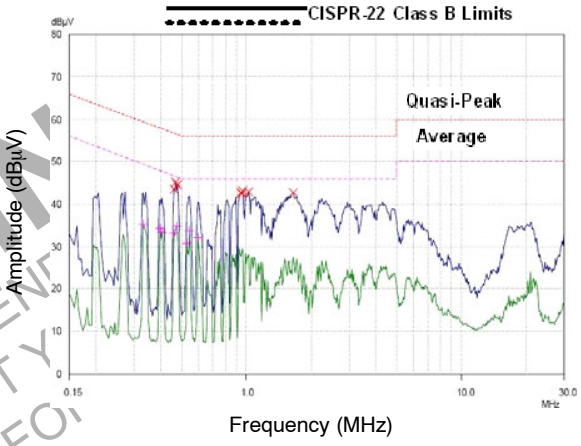



**Figure 22. FSDX−series Power Switch Full Range EMI Scan (67 KHz, with Frequency Modulation) with DVD Player SET**

### Adjusting Peak Current Limit

As shown in Figure 23, a combined 2.8 kΩ internal resistance is connected to the non−inverting lead on the PWM comparator. An external resistance of Rx on the current limit pin forms a parallel resistance with the 2.8 kΩ when the internal diodes are biased by the main current source of 900 μA.

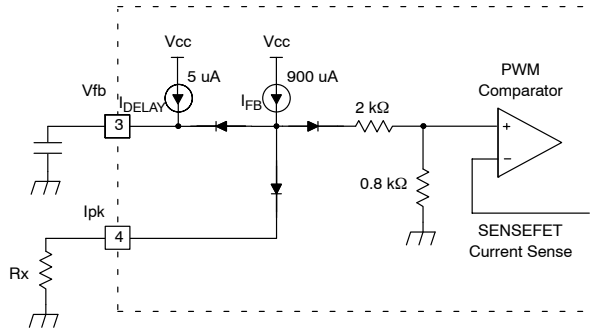



**Figure 23. Peak Current Limit Adjustment**

For example, FSDx321 has a typical SENSEFET peak current limit ($I_{LIM}$) of 0.7 A. ILIM can be adjusted to 0.5 A by inserting Rx between the Ipk pin and the ground. The value of the Rx can be estimated by the following equations:

$$0.7\ A : 0.5\ A = 2.8\ k\Omega : X\ k\Omega \quad \text{(eq. 1)}$$

$$X = Rx \parallel 2.8\ k\Omega \quad \text{(eq. 2)}$$

(X represents the resistance of the parallel network)

## APPLICATION TIPS

### Methods of Reducing Audible Noise

Switching mode power converters have electronic and magnetic components, which generate audible noises when the operating frequency is in the range of 20~20,000 Hz. Even though they operate above 20 kHz, they can make noise depending on the load condition. Designers can employ several methods to reduce these noises. Here are three of these methods:

*Glue or Varnish*

The most common method involves using glue or varnish to tighten magnetic components. The motion of core, bobbin and coil and the chattering or magnetostriction of core can cause the transformer to produce audible noise. The use of rigid glue and varnish helps reduce the transformer noise. But, it also can crack the core. This is because sudden changes in the ambient temperature cause the core and the glue to expand or shrink in a different ratio according to the temperature.

*Ceramic Capacitor*

Using a film capacitor instead of a ceramic capacitor as a snubber capacitor is another noise reduction solution. Some dielectric materials show a piezoelectric effect depending on the electric field intensity. Hence, a snubber capacitor becomes one of the most significant sources of audible noise. It is considerable to use a zener clamp circuit instead of an RCD snubber for higher efficiency as well as lower audible noise.

*Adjusting Sound Frequency*

Moving the fundamental frequency of noise out of 2~4 kHz range is the third method. Generally, humans are more sensitive to noise in the range of 2~4 kHz. When the fundamental frequency of noise is located in this range, one perceives the noise as louder although the noise intensity level is identical. Refer to Figure 24. Equal Loudness Curves.

When power switch acts in Burst mode and the Burst operation is suspected to be a source of noise, this method may be helpful. If the frequency of Burst mode operation lies in the range of 2~4 kHz, adjusting feedback loop can shift the Burst operation frequency. In order to reduce the Burst operation frequency, increase a feedback gain capacitor ($C_F$), opto−coupler supply resistor ($R_D$) and feedback capacitor ($C_B$) and decrease a feedback gain resistor ($R_F$) as shown in Figure 25. Typical Feedback Network of power switch.

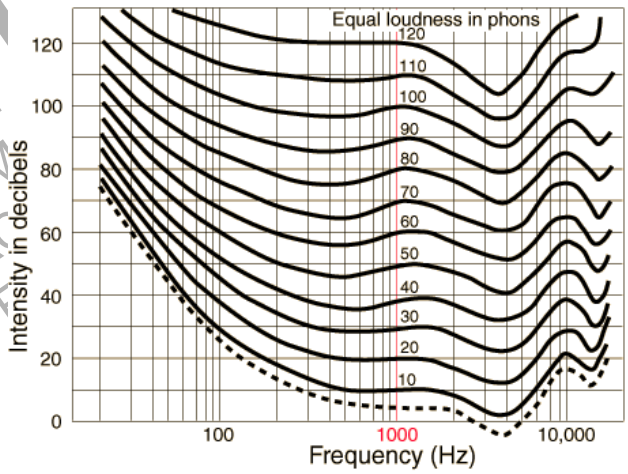



**Figure 24. Equal Loudness Curves**

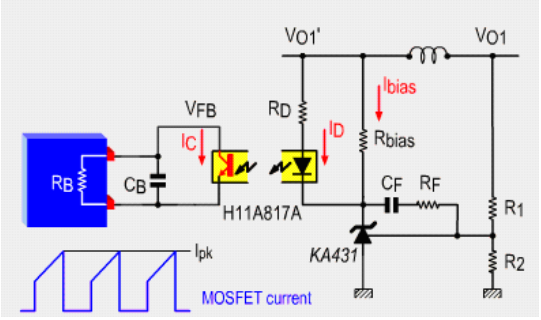



**Figure 25. Typical Feedback Network of Power Switch**

### Other Reference Materials

AN−4134: Design Guidelines for Off−line Forward Converters Using ON Semiconductor Power Switch

AN−4137: Design Guidelines for Off−line Flyback Converters Using ON Semiconductor Power Switch

AN−4140: Transformer Design Consideration for Off−line Flyback Converters using ON Semiconductor Power Switch

AN−4141: Troubleshooting and Design Tips for ON Semiconductor Power Switch Flyback Applications

AN−4147: Design Guidelines for RCD Snubber of Flyback

AN−4147: Audible Noise Reduction Techniques for FPS Applications

**Table 4. TYPICAL APPLICATION CIRCUIT**

| Application | Output Power | Input Voltage | Output Voltage (Max Current) |
|---|---|---|---|
| PC Auxiliary Power Supply | 10 W | DC 140~375 V | 5.0 V (2.0 A) |



### Features

- High efficiency (> 70% at full load, full input range)
- Low standby mode power consumption (< 1 W at DC 375 V input and 0.5 W load)
- Low component count
- Enhanced system reliability through various protection functions
- Low EMI through frequency modulation
- Internal soft−start (15 ms)

### Key Design Notes

- The delay time for over load protection is designed to be about 13 ms with C104 of 22 nF. If faster/slower triggering of OLP is required, C104 can be changed to a smaller/larger value (eg. 47 nF for about 30 ms).
- The pule−by−pulse peak current limit level($I_{LIM}$) is set to default value 0.7 A by floating the Ipk pin (#4).
- R102 and C101 clamp the DRAIN voltage of MOSFET below 650 V under all conditions.

### Schematic

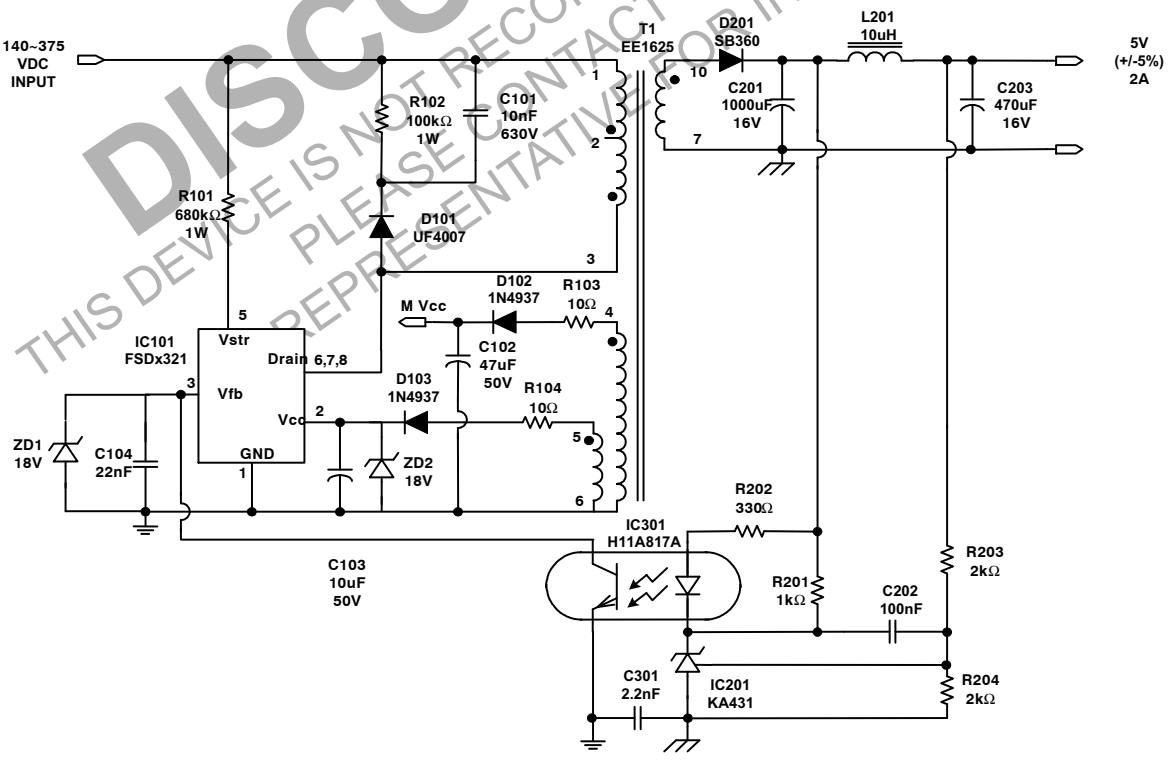



**Figure 26. 10 W PC Auxiliary Power Circuit**

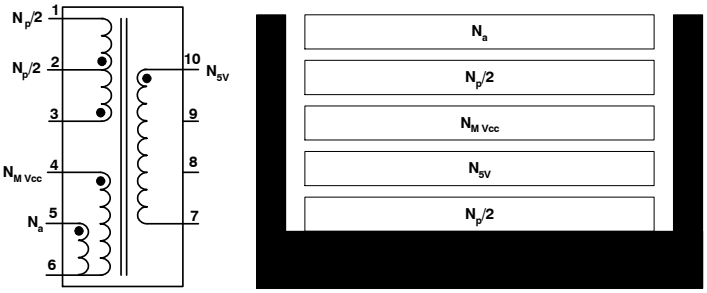



**Figure 27. Transformer Schematic Diagram**

**Table 5. WINDING SPECIFICATION**

| | Pin (S → F) | Wire | Turns | Winding Method |
|---|---|---|---|---|
| $N_p/2$ | 3 → 2 | 0.15 φ × 1 | 80 | Solenoid Winding |
| Insulation: Polyester Tape t = 0.050 mm, 3 Layers | | | | |
| $N_{5V}$ | 10 → 7 | 0.55 φ × 1 | 12 | Solenoid Winding |
| Insulation: Polyester Tape t = 0.050 mm, 3 Layers | | | | |
| $N_{MVcc}$ | 4 → 6 | 0.20 φ × 1 | 40 | Solenoid Winding |
| Insulation: Polyester Tape t = 0.050 mm, 3 Layers | | | | |
| $N_{P/2}$ | 2 → 1 | 0.15 φ × 1 | 80 | Solenoid Winding |
| Insulation: Polyester Tape t = 0.050 mm, 3 Layers | | | | |
| $N_a$ | 5 → 6 | 0.20 φ × 1 | 34 | Solenoid Winding |
| Outer Insulation: Polyester Tape t = 0.050 mm, 3 Layers | | | | |

**Table 6. ELECTRICAL CHARACTERISTICS**

| | Pin | Spec. | Remark |
|---|---|---|---|
| Inductance | 1–3 | 1.8 mH | 1 kHz, 1 V |
| Leakage | 1–3 | 100 μH | 2nd side all short |

**Core & Bobbin**

Core: EER1625

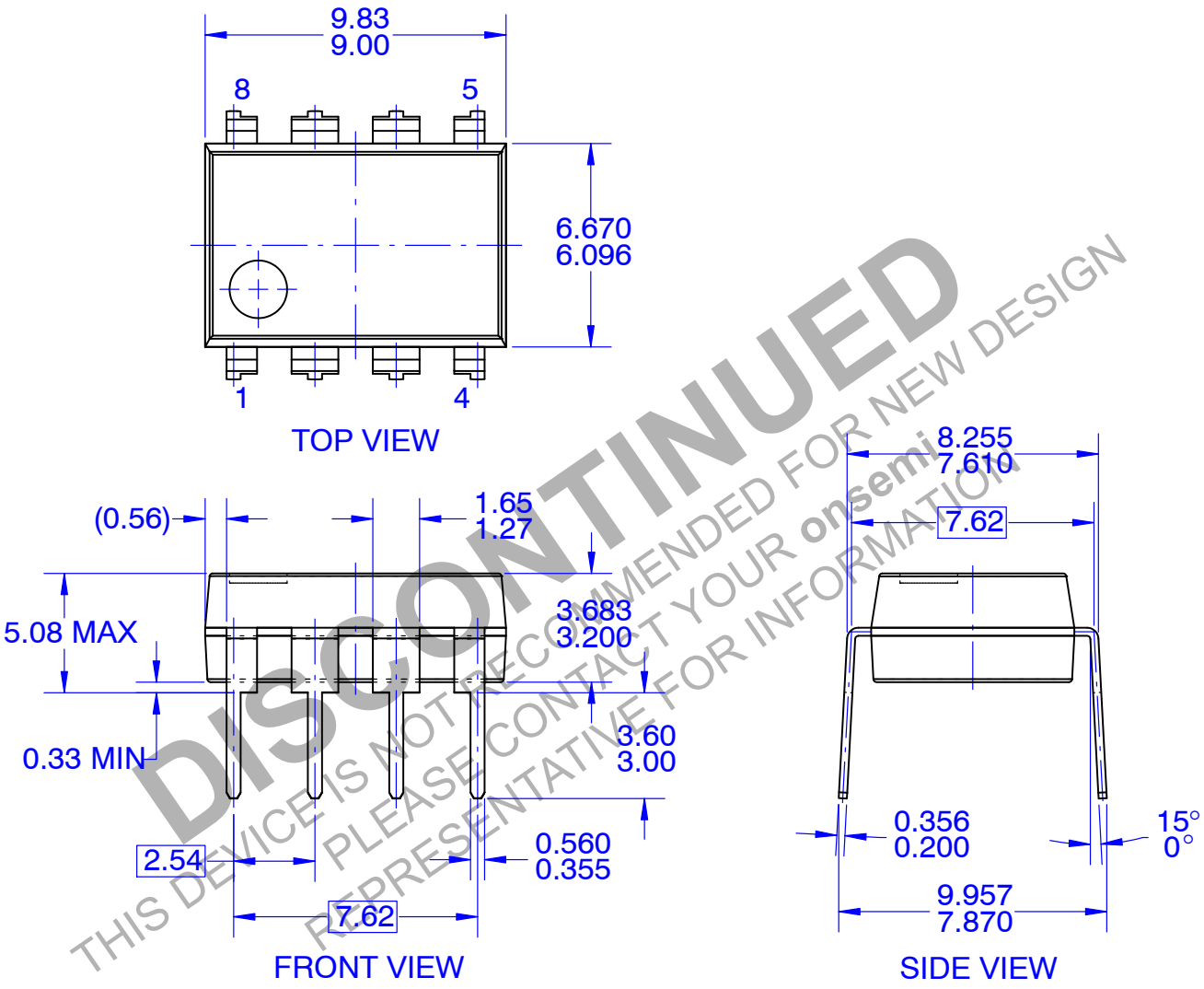
Bobbin: EER1625

**Table 7. DEMO CIRCUIT PART LIST**

| Part | Value | Note | Part | Value | Note |
|---|---|---|---|---|---|
| **Resistor** | | | **Inductor** | | |
| R101 | 680 K | 1 W | L201 | 10 uH | – |
| R102 | 100 K | 1 W | | | |
| R103 | 10 | 1/4 W | **Diode** | | |
| R104 | 10 | 1/4 W | D101 | UF4007 | PN Ultra Fast |
| R201 | 1 K | 1/4 W | D102 | 1N4937 | PN Ultra Fast |
| R202 | 330 | 1/4 W | D103 | 1N4937 | PN Ultra Fast |
| R203 | 2 K | 1/4 W | D201 | SB360 | Schottky |
| R204 | 2 K | 1/4 W | ZD1 | 1N4746A | 18V Zener |
| | | | ZD2 | 1N4746A | 18V Zener |
| **Capacitor** | | | | | |
| C101 | 10 nF / 630 V | Film | **IC** | | |
| C102 | 47 uF / 50 V | Electrolytic | IC101 | FSDH321 | Power Switch |
| C103 | 10 uF / 50 V | Electrolytic | IC201 | KA431 (TL431) | Voltage reference |
| C104 | 22 nF / 50 V | Film | IC301 | H11A817A | Opto−Coupler |
| C201 | 1000 uF / 16 V | Electrolytic | | | |
| C202 | 100 nF / 50 V | Ceramic | | | |
| C203 | 1 uF / 100 V | Electrolytic | | | |
| C204 | 470 uF / 16 V | Electrolytic | | | |
| C301 | 2.2 nF / 35 V | Ceramic | | | |

## PACKAGE DIMENSIONS

**PDIP8 9.42x6.38, 2.54P**
CASE 646CM
ISSUE O






NOTES:
A. CONFORMS TO JEDEC MS−001, VARIATION BA
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M−2009

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