USB Type-C Analog Audio Switch with Protection Function

FSA4486

WLCSP25 2.24 x 2.28 x 0.586
CASE 567UZ

MARKING DIAGRAM

6E = Device Code
&K = 2−Digits Lo Run Traceability Code
&. = Pin One Dot
&2 = 2−Digit Date Code
&Z = Assembly Plant Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 27 of this data sheet.

Description

FSA4486 is a high−performance USB Type−C port multimedia switch which supports analog audio headsets. FSA4486 allows the sharing of a common USB Type−C port to pass USB2.0 signal, analog audio, sideband use wires and analog microphone signal. FSA4486 also supports high voltage on SBU port and USB port on USB Type−C receptacle side.

Features

- Power Supply: VCC, 2.7 V to 5.5 V
- VCC Range from 2.7 V to 5.5 V (Primary)
- OVP Function on Common Node Pins
- Over Current Protection for Analog Ground Switch
- Analog Audio Device Unplug Detection and Can Be Used as General Comparator Also
- 20 V DC Tolerance on Connector Side Pins: DP_R, DN_L, GBSUx, SBUx
- 20 V DC Tolerance on CC_IN
- High Performance Audio/USB SW:
  - Audio SW, THD+N < −110 dB; 1 VRMS, 32 Ω Load;
  - USB SW, BW: 900 MHz
- 300 mΩ (Typical) Sense to GSBUx on Resistance
- 50 mΩ (Typical) SBUx to AGND on Resistance
- Moisture/Resistance Detection on DP_R, DN_L and SBUx
- 1.2v/1.8v Capable I^2C Interface
- 1:3 USB Switch with Third Data Path
- Two I^2C Address
- This is a Pb−Free Device

Applications

- Mobile Phone, Tablet, Notebook PC, Media Player

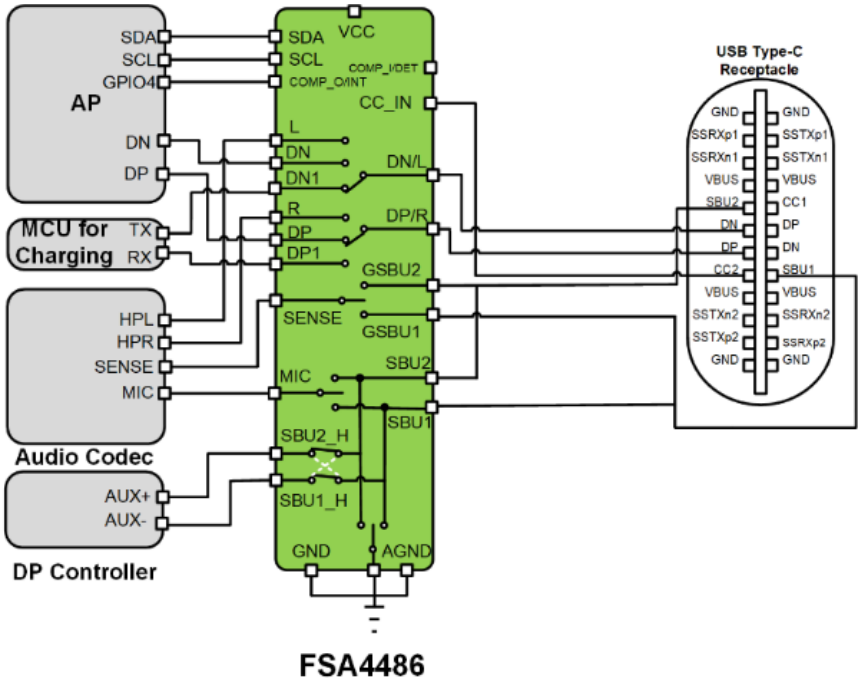


Figure 1. Application Block Diagram

PIN CONFIGURATION

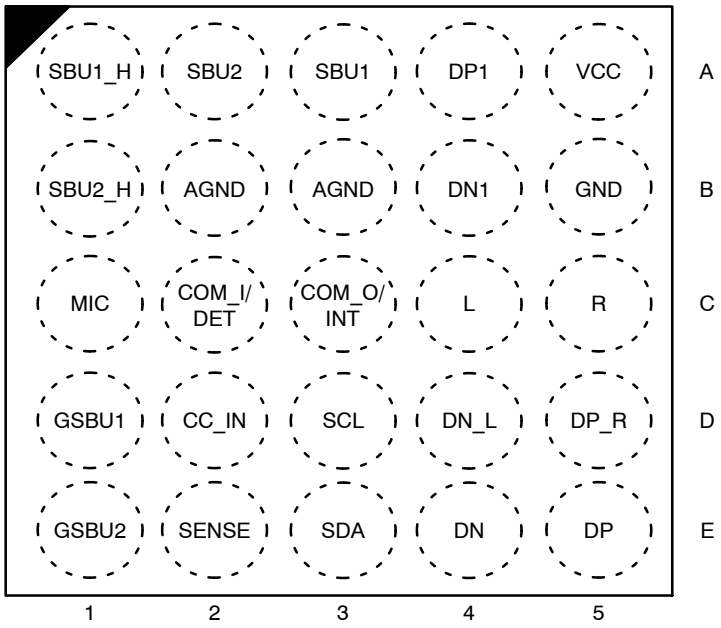


Figure 2. Pin Assignment (Top Through View)

Table 1. PIN DESCRIPTIONS

Name	Ball	Name	Description
1	A5	VCC	Power Supply (2.7 to 5.5 V) chip will be enabled after VCC is valid
2	B5	GND	Chip ground
3	D5	DP/R	USB/Audio Common Connector
4	D4	DN/L	USB/Audio Common Connector
5	E5	DP	USB Data (Differential +)
6	E4	DN	USB Data (Differential −)
7	C5	R	Audio − Right Channel
8	C4	L	Audio − Left Channel
9	A3	SBU1	Sideband use wire 1
10	A2	SBU2	Sideband use wire 2
11	C1	MIC	Analog audio microphone
12	B2	AGND	Audio ground
13	B3	AGND	Audio ground
14	E2	SENSE	Audio ground reference output
15	C3	COMP_O/INT	Internal comparator output/I^2C Interrupt output, active low (open drain)
16	D2	CC_IN	Audio accessary detach detection, also input of general comparator for device attach detection
17	D1	GSBU1	Audio sense path 1 to headset jack GND
18	E1	GSBU2	Audio sense path 2 to headset jack GND
19	C2	COMP_I/DET	INPUT/Open drain output.
20	D3	SCL1/SDA2	I^2C clock/Data
21	E3	SDA1/SCL2	I^2C data/Clock
22	B1	SBU2_H	Host Side Sideband Use Wire 2
23	A1	SBU1_H	Host Side Sideband Use Wire 1
24	A4	DP1	Data Path “+”
25	B4	DN1	Data Path “−”

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage from VCC	−0.5	6.5	V
V_{CC_IN}	V_{CC_IN}, to GND	−0.5	20	V
V_{SW_USB}	USB Switch Voltage, (DP_R, DN_L) to GND	−3.6	20	V
V_{SW_SBU}	SBU Switch Voltage, (SBUx, GSBUx) to GND	−0.5	20	V
V_{SW_HOST}	Host Side Switch Voltage, (DP, DN, S1H, S2H, SENSE, MIC) to GND	−0.5	6.5	V
V_{SW_DP1DN1}	Host Side Switch Voltage, (DP1, DN1) to GND	−3.6	6.5	V
V_{SW_Audio}	Host Side Switch Voltage, (L, R) to GND	−3.6	6.5	V
V_{CNTRL}	Control Pin Input Voltage, (SDA, SCL, COMPI/DET, COMPO/INT) to GND	−0.5	6.5	V
I_{IK}	DC Input Diode Current	−50	–	mA
I_{SW_USB}	USB Switch Current, between DP_R and DP or DN_L and DN	–	100	mA
I_{SW_DP1DN1}	Third Switch Current, between DP_R and DP1 or DN_L and DN1	–	100	mA
I_{SW_SBU}	SBU Switch Current, (S1H, S2H, MIC) to SBUx	–	50	mA
I_{SW_SENSE}	Sense Switch Current, SENSE to GSBUx	–	100	mA
I_{SW_AGND}	Analog Ground Current, AGND to SBUx	–	500	mA
I_{SW_Auido}	Audio Switch Current, between DP_R and R or DN_L and L	−250	250	mA
ESD_{HBM}	Human Body Model, JEDEC: JS−001−2017, for Host Pins	2	–	kV
ESD_{HBM_Con}	Human Body Model, JEDEC: JS−001−2017, for Connector Side Pins and Power Pins	2	–	kV
ESD_{CDM}	Charged Device Model, JEDEC: JS−002−2018	1	–	kV
T_A	Absolute Maximum Operating Temperature	−40	85	°C
T_{STG}	Storage Temperature	−65	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Max	Unit
POWER					
V_{CC}	Supply Voltage	2.7	–	5.5	V
USB SWITCH					
V_{SW_USB}	USB Switch Voltage, (DP_R, DN_L, DP, DN, DP1, DN1) to GND	0	–	3.6	V
AUDIO SWITCH					
V_{SW_Audio}	Audio Switch Voltage, (DP_R, DN_L, L, R) to GND	–3	–	3	V
DP1 DN1 SWITCH					
V_{VGSBU_SEN}	V_{GSBU1} to GND, V_{GSBU2} to GND, V_{SENSE} to GND	–1	–	3.6	V
SBU SWITCH					
V_{SW_SBU}	(SBUx, GSBUx) to GND	0	–	3.6	V
HOST SIDE SWITCH					
V_{SW_HOST}	(DP, DN, S1H, S2H, SENSE, MIC) to GND	0	–	3.6	V
CC_IN SWITCH					
V_{CC_IN}	V_{CC_IN}, to GND	0	–	5.5	V
CONTROL INPUT VOLTAGE (COMPI/DET, COMPO/INT, SDA, SCL)					
V_{CNTRL}	Input Voltage High	0	–	5.5	V
OPERATING TEMPERATURE					
TA	Ambient Operating Temperature	–40	25	+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. DC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 V to 5.5 V, V_{CC} (Typ.) = 3.3 V, T_A = −40°C to 85°C, and T_A (Typ.) = 25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Power	Min	Typ	Max	Unit
I_{CC}	Supply Current	USB switches on, SBUx to SBUx_H switches on	VCC: 2.7 V to 5.5 V	–	–	65	μA
I_{CC_AUDIO}	Audio Supply Current	Audio switches on, MIC switch on and Audio GND switch on		–	–	65	μA
ICCZ	Quiescent Current, Software Disabled	ENN = L, 04H'b7 = 0		–	–	5	μA
USB/AUDIO/MCU COMMON PINS: DP/R, DN_L							
IOZ	USB Connector Side Off Leakage Current	DP_R, DN_L = 0 V to 3.6 V	VCC: 2.7 V to 5.5 V	–3	–	3	μA
IOFF	USB Connector Side Power Off Leakage Current	DP_R, DN_L = 0 V to 3.6 V, VCC = 0 V	Power off	–3	–	3	μA
VOV_TRIP	Input OVP Lockout	Rising Edge of DP_R, DN_L	VCC: 2.7 V to 5.5 V	4.5	5	5.3	V
VOV_HYS	Input OVP Hysteresis			–	0.3	–	V
USB SWITCH							
ION_USB	USB Switch ON Leakage Current	DN_L, DP_R = 0 V to 3.6 V, DP, DN, R, L, DP1, DN1 = Float	VCC: 2.7 V to 5.5 V	–3	–	3	μA
IOZ_USB	USB Host Side Off Leakage Current	DN, DP = 0 V to 3.6 V		–3	–	3	μA
IOFF_USB	USB Host Side Power Off Leakage Current	DN, DP = 0 V to 3.6 V, VCC = 0 V	Power off	–3	–	3	μA
RON_USB	USB Switch On Resistance	ISW = 8 mA, VSW = 0.4 V	VCC: 2.7 V to 5.5 V	–	3	5.2	Ω
DP1 DN1 SWITCH							
ION_DN1DP1	DN1DP1 Switch ON Leakage Current	DN_L, DP_R = 0 V to 3.6 V, DP, DN, R, L , DP1, DN1 = Float	VCC: 2.7 V to 5.5 V	–3	–	10	μA
IOZ_DN1DP1	DN1DP1 Host Side Off Leakage Current	DN1, DP1 = 0 V to 3.6 V		–3	–	3	μA
IOFF_DN1DP1	DN1DP1 Host Side Power Off Leakage Current	DN1, DP1 = 0 V to 3.6 V, VCC = 0 V	Power off	–3	–	3	μA
RON_DN1DP1	DN1DP1 Switch On Resistance	ISW = 8 mA, VSW = 0.4 V	VCC: 2.7 V to 5.5 V	–	3	6.2	Ω
AUDIO SWITCH							
ION_AUDIO	ON Leakage Current of Audio Switch	DN_L, DP_R = –3 V to 3.0 V, DP, DN, R, L, DP1, DN1 = Float	VCC: 2.7 V to 5.5 V	–2.5	–	2.5	μA
IOFF_AUDIO	Power Off Leakage Current of Audio Switch L, R	L, R = 0 V to 3 V; DP_R, DN_L = Float, VCC = 0V	Power off	–1	–	1	μA
RON_AUDIO	Audio Switch On Resistance	ISW = 100 mA, VSW = –3 V to 3 V	VCC: 2.7 V to 5.5 V	–	1	2.1	Ω
RON_FLAT	Audio Switch On Resistance Flatness	VSW = –3.0 V to +3.0 V	VCC: 2.7 V to 5.5 V	–	10	–	mΩ
RSHUNT	Pull Down Resistor on R/L Pin when Audio Switch is Off	L = R = 3 V	VCC: 2.7 V to 5.5 V	6	10	14	kΩ
SBU COMMON PINS							
IOZ_SBU	Off Leakage Current (SBU1, SBU2)	SBUx = 0 V to 3.6 V	VCC: 2.7 V to 5.5 V	–3	–	3	μA
IOFF_SBU	Power Off Leakage Current (SBU1, SBU2)	SBUx = 0 V to 3.6 V, VCC = 0 V	Power off	–3	–	3	μA
VOV_TRIP	Input OVP Lockout	Rising edge	VCC: 2.7 V to 5.5 V	4.5	5	5.3	V
VOV_HYS	Input OVP Hysteresis			–	0.3	–	V

Table 4. DC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 V to 5.5 V, V_{CC} (Typ.) = 3.3 V, T_A = −40°C to 85°C, and T_A (Typ.) = 25°C, unless otherwise specified.) (continued)

Symbol	Parameter	Condition	Power	Min	Typ	Max	Unit
SBU DATA SWITCH							
ION_SxH	ON Leakage Current of SBU Switch	SBUx = 0 V to 3.6 V, SxH = Float	VCC: 2.7 V to 5.5 V	−3	–	3	μA
IOZ_SxH	Off Leakage Current (S1H, S2H)	SxH = 0 V to 3.6 V		−1	–	1	μA
IOFF_SxH	Power Off Leakage Current (S1H, S2H)	SxH = 0 V to 3.6 V, VCC = 0 V	Power off	−1	–	1	μA
RON_SxH	SBU Switch On Resistance to (S1H, S2H)	VSW = 0 V to 3.6 V, ISW = 20 mA	VCC: 2.7 V to 5.5 V	1	3	5	Ω
MIC SWITCH							
ION_MIC	ON Leakage Current of SBU Switch	SBUx = 0 V to 3.6 V, MIC = Float	VCC: 2.7 V to 5.5 V	−3	–	3	μA
IOZ_MIC	Off Leakage Current (S1H, S2H)	MIC = 0 V to 3.6 V		−1	–	1	μA
IOFF_MIC	Power Off Leakage Current (S1H, S2H)	MIC = 0 V to 3.6 V, VCC = 0 V	Power off	−1	–	1	μA
RON_MIC	SBU Switch On Resistance to (S1H, S2H)	VSW = 0 V to 3.6 V, ISW = 20 mA	VCC: 2.7 V to 5.5 V	1	3	5	Ω
AGND SWITCH							
RON_AGND	SBUx Switch On Resistance to AGND	ISW = 100 mA on SBUx	VCC: 2.7 V to 5.5 V	25	50	90	mΩ
IOC_TRIP	Input OCP Lockout SBUx to AGND	04h'b0 = 1, 07h = xx010xxxb or xxxxx010b		–	1.5	–	A
SENSE SWITCH							
ION_SENSE	ON Leakage Current of SENSE Switch	On GSBUx = 0 V to 1.0 V, Sense = Float	VCC: 2.7 V to 5.5 V	−2	–	2	μA
IOZ_SENSE	Off Leakage Current of SENSE	Sense = 0 V to 1.0 V		−2	–	2	μA
IOZ_GSBU	Off Leakage Current of GSBUx	GSBUx = 0 V to 3.6 V		−3	–	3	μA
IOFF_SENSE	Power Off Leakage Current of SENSE	Sense = 0 V to 1.0 V, VCC = 0 V	Power off	−2	–	2	μA
IOFF_GSBU	Power Off Leakage Current of GSBUx	GSBUx = 0 V to 3.6 V, VCC = 0 V		−3	–	3	μA
RON_SENSE	Sense Switch On Resistance	IOUT = 100 mA, VSW =1 V	VCC: 2.7 V to 5.5 V	150	300	500	mΩ
CC IN PIN							
IIN_CC	CC_IN Input Leakage Current	CC_IN = 0 V to 5.5 V	VCC: 2.7 V to 5.5 V	–	–	1	μA
CC IN THRESHOLD WHEN MODE_SEL = 1							
V_CC_Trip	Input High Threshold		VCC: 2.7 V to 5.5 V	–	0.27	–	V
V_CC_HYS	Input Hysteresis Voltage			–	0.03	–	V
CC IN THRESHOLD WHEN MODE_SEL = 0							
VTH_L_CC	Input Low Threshold		VCC: 2.7 V to 5.5 V	–	1.2	–	V
VTH_H_CC	Input High Threshold			–	1.5	–	V
COMP_O/INT PIN							
VOL	Output Voltage Low	IOUT = 2 mA		–	–	0.275	V
IIN	COMP_O/INT Input Leakage Current	COMP_O/INT = 0 V to VCC; VCC = 2.7 V – 5.5 V	VCC: 2.7 V to 5.5 V	−3	–	3	μA

Table 4. DC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 V to 5.5 V, V_{CC} (Typ.) = 3.3 V, T_A = −40°C to 85°C, and T_A (Typ.) = 25°C, unless otherwise specified.) (continued)

Symbol	Parameter	Condition	Power	Min	Typ	Max	Unit
COMP_I/DET PIN							
V_COMP/I_Trip	High Voltage Input		VCC: 2.7 V to 5.5 V	–	0.27	–	V
V_COMP/I_HYS	Input hysteresis voltage			–	30	–	mV
VOL_DET	Output Low Voltage	IOUT = 2 mA		–	–	0.275	V
IIN	Input Current			–3	–	3	μA
I²C PINS							
VIL_I2C	Low Level Input Voltage		VCC: 2.7 V to 5.5 V	–	–	0.45	V
VIH_I2C	High Level Input Voltage			0.72	–	VCC	V
IIN_I2C	Input Current	SCL1/SDA2, SDA1/SCL2 = 0 V to 3.6 V		–2	–	2	μA
IOL_I2C	Low Level Output Current	VOL = 0.2 V		10	–	–	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 5. AC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 V to 5.5 V, V_{CC} (Typ.) = 3.3 V, T_A = −40°C to 85°C, and T_A (Typ.) = 25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Power	Min	Typ	Max	Unit
AUDIO SWITCH							
tDELAY_Audio	Turn On Time	DP/R = DN/L = 0 V → to 1 V, L, R = 32 Ω to GND	VCC = 3.3 V	–	65	–	μs
tOFF_Audio	Audio Switch Turn Off Time	DP_R = DN_L = 1 V, RL = 32 Ω		–	25	–	μs
XTALK_Audio	Crosstalk between Left and Right	f = 1 kHz, RL = 50 Ω, VSW = 1 VRMS		–	−100	–	dB
BW_Audio	–3 dB Bandwidth	RL = 50 Ω		–	500	–	MHz
OIRR_Audio	Off Isolation	f = 1 kHz, RL = 50 Ω, CL = 0 pF, VSW = 1 VRMS, all of switches need to be opened		–	−100	–	dB
THD+N_600	Total Harmonic Distortion + Noise Performance with A–weighting Filter	RL = 600 Ω, f = 20 Hz~20 kHz, VSW = 2 VRMS		–	−110	–	dB
THD+N_32	Total Harmonic Distortion + Noise Performance with A–weighting Filter	RL = 32 Ω, f = 20 Hz~20 kHz, VSW = 1 VRMS		–	−110	–	dB
THD+N_16	Total Harmonic Distortion + Noise Performance with A–weighting Filter	RL = 16 Ω, f = 20 Hz~20 kHz, VSW = 0.5 VRMS		–	−108	–	dB
PSRR	Power Supply Rejection Ratio	VPSRR = VCC+ 100 mVRMS RL = 32 Ω at DP/R, DN/L f = 1 kHz		–	−120	–	dB
USB SWITCH							
tON_USB	USB Switch Turn–on Time	DP_R = DN_L = 1.5 V, RL = 50 Ω	VCC = 3.3 V	–	60	–	μs
tOFF_USB	USB Switch Turn–off Time	DP_R = DN_L = 1.5 V, RL = 50 Ω		–	25	–	μs
BW_USB	–3 dB Differential Bandwidth	RL = 50 Ω		–	0.9	–	GHz
OIRR_USB	Off Isolation between DP, DN and Common Node Pins	f = 1 kHz, RL = 50 Ω, CL = 0 pF, VSW = 1 VRMS, all of switch need to be opened		–	−100	–	dB
tOVP_USB	DP_R and DN_L Pins OVP Response Time	Rload = 50 Ω, VSW = 4 V to 6 V		–	0.5	1	μs

Table 5. AC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 V to 5.5 V, V_{CC} (Typ.) = 3.3 V, T_A = −40°C to 85°C, and T_A (Typ.) = 25°C, unless otherwise specified.) (continued)

Symbol	Parameter	Condition	Power	Min	Typ	Max	Unit
DP1DN1 SWITCH							
tON_DP1DN1	DP1DN1 Switch Turn−on Time	DP_R = DN_L = 1.5 V, RL = 50 Ω	VCC = 3.3 V	–	70	–	μs
tOFF_DP1DN1	DP1DN1 Switch Turn−off Time	DP_R = DN_L = 1.5 V, RL = 50 Ω		–	25	–	μs
BW_DP1DN1	−3 dB Differential Bandwidth	RL = 50 Ω		–	100	–	MHz
OIRR_DP1DN1	Off Isolation between DP1, DN1 and Common Node Pins	f = 1 kHz, RL = 50 Ω, CL = 0 pF, VSW = 1 VRMS, all of switches need to be opened		–	−100	–	dB
MIC/AUDIO GROUND SWITCH							
tON_MIC	MIC Switch Turn On Delay Time with Slow Turn On	SBUx = 1 V, RL = 50 Ω, MIC_SLOW = 00000000b	VCC = 3.3 V	–	250	–	μs
tOFF_MIC	MIC Switch Turn Off Time	SBUx = 2.5 V → GND, MIC = 50 Ω to GND		–	25	–	μs
tON_AGND	AGND Switch Turn On Time	SBUx pulled up to 0.5 V by 16 Ω, AGND connect to GND		–	250	–	μs
tOFF_AGND	AGND Switch Turn Off Time	SBUx = 0.5 V by 16 Ω		–	25	–	μs
BW	MIC Switch Bandwidth	RL = 50 Ω		–	50	–	MHz
PSRR_MIC	Power Supply Rejection Ratio to MIC	Supply Noise = 300 mVpp, f = 1 kHz, RL = 2000 Ω		–	−100	–	dB
SBU SWITCH							
tON_SBU	SBUx_H Switch Turn On Time	SBUx = 2.5 V, RL = 50 Ω	VCC = 3.3 V	–	100	–	μs
tOFF_SBU	SBUx_H Switch Turn Off Time	SBUx = 2.5 V, RL = 50 Ω		–	25	–	μs
BW_SBU	Bandwidth	RL = 50 Ω		–	50	–	MHz
tOVP_SBU	SBUx Pins OVP Response Time	Rload = 50 Ω, Vsw = 4 V to 6 V		–	0.5	1	μs
SENSE SWITCH							
tON_SENSE	Turn−On Time	GSBUx = 0 V to 1 V, SENSE = 50 Ω to GND	VCC = 3.3 V	–	400	–	μs
tOFF_SENSE	Sense Switch Turn Off Time	GSBUx = 1 V, RL = 50 Ω		–	25	–	μs
tOVP_SENSE	GSBUx Pins OVP Response Time	Rload = 50 Ω, Vsw = 4 V to 6 V		–	0.5	1	μs
BW_SENSE	Bandwidth	RL = 50 Ω		–	150	–	MHz
DET DELAY							
tDELAY_DET	DET Response Delay	Transition from High−Z to Low (DET to 10% VIO) or Low to High−Z (DET to 90% of VIO)	VCC = 3.3 V	–	5	–	μs

1. Refer to Typical Characteristics waveforms/graphs for closed loop data and variation with input supply and temperature. Electrical specifications reflect open loop steady state data. System specifications reflects both steady state and dynamic close loop data associated with the recommended external components.

Table 6. I²C SPECIFICATION (V_{CC} = 2.7 V to 5.5, V_{CC} (Typ.) = 3.3 V ,T_A = −40°C to 85°C. T_A (Typ.) = 25°C, unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	I2C_SCL Clock Frequency	–	400	–	kHz
tHD; STA	Hold Time (Repeated) START Condition	0.6	–	–	μs
tLOW	Low Period of I2C_SCL Clock	1.3	–	–	μs
tHIGH	High Period of I2C_SCL Clock	0.6	–	–	μs
tSU; STA	Set−up Time for Repeated START Condition	0.6	–	–	μs
tHD; DAT	Data Hold Time (Note 2)	0	–	0.9	μs
tSU; DAT	Data Set−up Time	100	–	–	ns
tr	Rise Time of I2C_SDA and I2C_SCL Signals (Note 3)	20 + 0.1Cb	–	300	ns
tf	Fall Time of I2C_SDA and I2C_SCL Signals (Note 3)	20 + 0.1Cb	–	300	ns
tSU; STO	Set−up Time for STOP Condition	0.6	–	–	μs
tBUF	Bus−Free Time between STOP and START Conditions	1.3	–	–	μs
tSP	Pulse Width of Spikes that Must Be Suppressed by the Input Filter	0	–	50	ns

2. Guaranteed by characterization, not production tested.
3. C_b = capacitance of one bus line in pF (10 pF ≤ C_b ≤ 400 pF).

Table 7. CAPACITANCE (V_{CC} = 2.7 V to 5.5 V, V_{CC} (Typ.) = 3.3 V, T_A = −40°C to 85°C, and T_A (Typ.) = 25°C)

Symbol	Parameter	Condition	Power	Min	Typ	Max	Unit
CON_USB	On Capacitance of USB Common Pins	f = 1 MHz, 100 mVPK−PK, 100 mV DC	VCC = 3.3 V	–	9	–	pF
COFF_ USB	Off Capacitance of USB Common Pins	f = 1 MHz, 100 mVPK−PK, 100 mV DC		–	7.5	–	pF
COFF_USBHost	Off Capacitance of USB Host Pins	f = 1 MHz, 100 mVPK−PK, 100 mV DC		–	3	–	pF
COFF_DP1DN1 Switch	Off Capacitance of USB DP1,DN1 Pins	f = 1 MHz, 100 mVPK−PK, 100 mV DC		–	3	–	pF
CON_SENSE	On Capacitance of GSBUx	f = 1 MHz, 100 mVPK−PK, 100 mV DC		–	40	–	pF
COFF_SENSE	Off Capacitance of GSBUx	f = 1 MHz, 100 mVPK−PK, 100 mV DC		–	60	–	pF
CON_MIC	On Capacitance of SBUx to MIC Switch	f = 1 MHz, 100 mVPK−PK, 100 mV DC		–	170	–	pF
COFF_MIC	Off Capacitance of MIC	f = 1 MHz, 100 mVPK−PK, 100 mV DC		–	10	–	pF
CON_AGND	On Capacitance of SBUx to AGND Switch	f = 1 MHz, 100 mVPK−PK, 100 mV DC		–	150	–	pF
CON_SBU	On Capacitance of SBUx to SxH Switch	f = 1 MHz, 100 mVPK−PK, 100 mV DC		–	110	–	pF
CCNTRL	Control Input Pin Capacitance	f = 1 MHz, 100 mVPK−PK, 100 mV DC		–	3	–	pF

Table 8. REGISTER MAPS

ADDR	Register Name	Type	Reset Value	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00H	Device ID	R	0x08	0	0	0	0	1	0	0	1
01H	OVP Interrupt Mask	R/W	0x00	Mask OCP_AGND	Mask OVP interrupt	Mask OVP/ DP_R	Mask OVP/ DN_L	Mask OVP/ SBU1	Mask OVP/ SBU2	Mask OVP/ GSBU1	Mask OVP/ GSBU2
02H	OVP Interrupt Flag	R/C	0x00	OCP_AGND	OVP_ALL	DP_R	DN_L	SBU1	SBU2	GSBU1	GSBU2
03H	OVP Status	R	0x00	Reserved	OCP_STAT_ AGND	OVP/ DP_R	OVP/ DN_L	OVP/SB U1	OVP/SB U2	OVP/ GSBU1	OVP/ GSBU2
04H	Switch Settings Enable	R/W	0xF8	Device control	SBU1_H to SBUx	SBU2_H to SBUx	DN_L EN	DP_R EN	SENSE_EN	MIC_EN	AGND_EN
05H	Switch Select	R/W	0x08	Reserved	SBU1_H	SBU2_H	DN_L	DP_R	Sense	MIC	AGND
06H	Switch Status1	R	0x05	Reserved		Sense Switch Status		DP_R Switch Status		DN_L Switch Status	
07H	Switch Status2	R	0x23	Reserved		SBU2 Switch Status			SBU1 Switch Status		
08H	CURR_Source_Status	R	0x02	Reserved						Current source Status	
09H	Protection_EN	R/W	0x03	Reserved					Mode_sel	EN_OVP	EN_OCP
0AH	MIC_Slow	R/W	0x00	MIC switch right channel slow control [7:0]							
0BH	Protection Status	R	0x2C	Reserved		USB_OVP	GSBU_OVP	SBU1_OVP	SBU2_OVP	OCP1	OCP2
0CH	CURR_Source_Set	R/W	0x02	Audio ground switch right channel slow control [7:0]						Curr_source_set	
0DH	L2R_EN_Delay	R/W	0x00	L2R_EN_Delay							
0EH	MIC2L_EN_Delay	R/W	0x00	MIC2L_EN_Delay							
0FH	SENSE2L_EN Delay	R/W	0x00	SENSE2L_EN Delay							
10H	AGND2L_EN Delay	R/W	0x00	AGND2L_EN Delay							
11H	Audio Accessory Status	R	0x01	Reserved						CC_IN	DET
12H	Function Enable	R/W	0XC0	DET_FUNCT	RES_DET_RANGE		HIZ_ACC_DET	AUTO_REST	MIC auto OFF	RES DET	AUDIO_JACK_ DET
13H	RES_PIN_SEL	R/W	0x01	Reserved					RES_PIN_SEL		
14H	RES Value	R	0xFF	RES value							
15H	RES_DET_THRESH	R/W	0x16	RES_DET_THRESH							
16H	RES Detection Interval	R/W	0x0C	Reserved		TIMER_REST		AUTO_REST_TIMER		RES_DET_INTV	
17H	Audio Jack Status	R	0x01	Reserved		UNKOWN_Audio_ACC		4pole_A	4pole_B	3pole	No audio
18H	Detection Interrupt	R/C	0x00	Reserved		I_CC/IN_CHG		I_DET_FUNCT	I_AUDIO_ JACK_DET	I_LOW_RES	I_RES_DET_ COMP
19H	Detection Interrupt Mask	R/W	0x10	Reserved		M _CC/IN_CHG		M_DET_ FUNCT	M_AUDIO_ JACK_DET	M_LOW_RES	M_RES_DET_ COMP
1AH	AUDIO_JACK_DET1	R	0xFF	AUDIO_JACK_DET1							
1BH	AUDIO_JACK_DET2	R	0xFF	AUDIO_JACK_DET2							
1CH	MIC_DET_TH_LOW	R/W	0x20	MIC_DET_TH_LOW							
1DH	MIC_DET_TH_UP	R/W	0xFF	MIC_DET_TH_UP							

DEVICE ID

Address: 00h
Reset Value: 8'b 0000_1000
Type: Read

Bit	Name	Default	Description
7:6	VENID	00	Vendor ID
5:3	VERID	001	Version ID Low: 001h [Version ID]_revA: 0x001 (e.g. A_revA) [Version ID]_revA: 0x010 (e.g. B_revA) [Version ID]_revA: 0x011 (e.g. C_revA) etc
2:0	REVID	000	Revision ID Low: 000h A_[Revision ID]: 0x000 (e.g. A_revA) A_[Revision ID]: 0x001 (e.g. A_revB) A_[Revision ID]: 0x010 (e.g. A_revC) etc

OVP /OCP INTERRUPT MASK

Address: 01h
Reset Value: 8'b 0000_0000
Type: Read/Write

Bit	Name	Default	Description
7	M_OCP_AGND	0	0b: Do not mask OCP interrupt 1b: Mask OCP interrupt on SBUx to AGND
6	OVP Interrupt mask control	0	OVP Interrupt function Enable/Disable 0: Controlled by [5:0] bit 1: Mask all connector side pins OVP interrupt
5	DP_R OVP Interrupt mask control	0	0: Do not mask OVP interrupt 1: Mask OVP interrupt
4	DN_L OVP Interrupt mask control	0	0: Do not mask OVP interrupt 1: Mask OVP interrupt
3	SBU1 OVP Interrupt mask control	0	0: Do not mask OVP interrupt 1: Mask OVP interrupt
2	SBU2 OVP Interrupt mask control	0	0: Do not mask OVP interrupt 1: Mask OVP interrupt
1	GSBU1 OVP Interrupt mask control	0	0: Do not mask OVP interrupt 1: Mask OVP interrupt
0	GSBU2 OVP Interrupt mask control	0	0: Do not mask OVP interrupt 1: Mask OVP interrupt

OVP/OCP INTERRUPT FLAG

Address: 02h
Reset Value: 8'b 0000_0000
Type: Read Clear

Bit	Name	Default	Description
7	I_OCP_AGND	0	0: OCP has not occured 1: OCP event has occured on SBUx to AGND
6	I_OVP_ALL	0	0: OVP or OCP event has not occurred 1: OVP or OCP event has occurred
5	DP_R OVP	0	0: OVP event has not occurred 1: OVP event has occurred
4	DN_L OVP	0	0: OVP event has not occurred 1: OVP event has occurred
3	SBU1 OVP	0	0: OVP event has not occurred 1: OVP event has occurred
2	SBU2 OVP	0	0: OVP event has not occurred 1: OVP event has occurred
1	GSBU1 OVP	0	0: OVP event has not occurred 1: OVP event has occurred
0	GSBU2 OVP	0	0: OVP event has not occurred 1: OVP event has occurred

OVP/OCP STATUS

Address: 03h
Reset Value: 8'b 0000_0000
Type: Read

Bit	Name	Default	Description
7	Reserved	0	Do Not Use
6	OCP_STAT_AGND	0	0: OCP event has not occurred 1: OCP event has occurred on SBUx to AGND
5	OVP on DP_R PIN	0	0: OVP event has not occurred 1: OVP event has occurred
4	OVP on DN_L PIN	0	0: OVP event has not occurred 1: OVP event has occurred
3	OVP on SBU1 PIN	0	0: OVP event has not occurred 1: OVP event has occurred
2	OVP on SBU2 PIN	0	0: OVP event has not occurred 1: OVP event has occurred
1	OVP on GSBU1 PIN	0	0: OVP event has not occurred 1: OVP event has occurred
0	OVP on GSBU2 PIN	0	0: OVP event has not occurred 1: OVP event has occurred

SWITCHING SETTING ENABLE

Address: 04h
Reset Value: 8'b 1111_1000
Type: Read/Write

Bit	Name	Default	Description
7	Device Enable	1	0: Device Disable; All switch nodes will be high−Z. 1: Device Enable.
6	SBU1_H to SBUx switches	1	0: Switch Disable; SBU1_H will be high−Z. 1: Switch Enable Internal Notes: Priority: SBU > AGND > MIC
5	SBU2_H to SBUx switches	1	0: Switch Disable; SBU2_H will be high−Z. 1: Switch Enable Internal Notes: Priority: SBU > AGND > MIC
4	DN/L to DN/L/DN1 switches	1	0: Switch Disable; DN/L, DN/L/DN1 will be high−Z 1: Switch Enable
3	DP/R to DP/R/DP1 switches	1	0: Switch Disable; DP/R, DP/R/DP1 will be high−Z 1: Switch Enable
2	Sense to GSBUx switches	0	0: Switch Disable; Sense, GSBU1 and GSBU2 will be high−Z 1: Switch Enable
1	MIC to SBUx switches	0	0: Switch Disable: MIC will be high−Z. 1: Switch Enable Internal Notes: Priority: SBU > AGND > MIC
0	AGND to SBUx switches	0	0: Switch Disable: AGND will be high−Z. 1: Switch Enable Internal Notes: Priority: SBU > AGND > MIC

SWITCH SELECT

Address: 05h
Reset Value: 8'b 0000_1000
Type: Read/Write

Bit	Name	Default	Description
7	Reserve	0	No Use
6	S1H_SEL	0	0b: S1H to SBU1 switch is CLOSED 1b: S1H to SBU2 switch is CLOSED Internal Notes: Priority: SBU > AGND > MIC
5	S2H_SEL	0	0b: S2H to SBU2 switch is CLOSED 1b: S2H to SBU1 switch is CLOSED Internal Notes: Priority: SBU > AGND > MIC
4:3	USB_SWITCH_SEL	01	00b: DN_L/DP_R to L/R switch is CLOSED 01b: DN_L/DP_R to DN/DP switch is CLOSED 10b: DN_L/DP_R to DN1/DP1 switch is CLOSED 11b: Reserved
2	SENSE_SEL	0	0b: SENSE to GSBU1 switch is CLOSED 1b: SENSE to GSBU2 switch is CLOSED
1	MIC_SEL	0	0b: MIC to SBU2 switch is CLOSED 1b: MIC to SBU1 switch is CLOSED If AGND_SEL = 0b and MIC_SEL = 1b when AGND_EN and MIC_EN = 1b then MIC = High−Z If AGND_SEL = 1b and MIC_SEL = 0b when AGND_EN and MIC_EN = 1b then MIC = High−Z Internal Notes: Priority: SBU > AGND > MIC
0	AGND_SEL	0	0b: AGND to SBU1 switch is CLOSED 1b: AGND to SBU2 switch is CLOSED Internal Notes: Priority: SBU > AGND > MIC

SWITCH STATUS1

Address: 06h
Reset Value: 8'b 0000_0101
Type: Read Only

Bit	Name	Default	Description
7:6	Reserved	00	Do Not Use
5:4	SENSE_STAT	00	00b: SENSE switch is OPEN 01b: SENSE switch is CLOSED to GSBU1 10b: SENSE Switch is CLOSED to GSBU2 11b: Not Valid
3:2	DP_R_DP1_STAT	01	00b: DP_R switch is OPEN 01b: DP_R switch is CLOSED to DP 10b: DP_R Switch is CLOSED to R 11b: DP_R switch is CLOSED to DP1
1:0	DN_L_DN1_STAT	01	00b: DN_L switch is OPEN 01b: DN_L switch is CLOSED to DN 10b: DN_L Switch is CLOSED to L 11b: DN_L switch is CLOSED to DN1

SWITCH STATUS2

Address: 07h
Reset Value: 8'b 0010_0011
Type: Read Only

Bit	Name	Default	Description
7:6	Reserved	00	Do Not Use
5:3	SBU2_STAT	100	000b: SBU2 switch is OPEN 001b: SBU2 switch is CLOSED to MIC 010b: SBU2 Switch is CLOSED to AGND 011b: SBU2 Switch is CLOSED to S1H 100b: SBU2 Switch is CLOSED to S2H 101b: SBU2 Switch is CLOSED to both S1H and S2H 110b: Not Valid 111b: Not Valid
2:0	SBU1	011	000b: SBU1 switch is OPEN 001b: SBU1 switch is CLOSED to MIC 010b: SBU1 Switch is CLOSED to AGND 011b: SBU1 Switch is CLOSED to S1H 100b: SBU1 Switch is CLOSED to S2H 101b: SBU1 Switch is CLOSED to both S1H and S2H 110b: Not Valid 111b: Not Valid

CURR_SOURCE_STATUS

Address: 08h
Reset Value: 8'b 0000_0010
Type: Read

Bit	Name	Default	Description
7:2	Reserved	000000	Do Not Use
1:0	CURR_SOURCE_STAT	10	00b: 20 μA 01b: 100 μA 10b: 700 μA (DEFAULT) 11b: 1500 μA

PROTECTION EN

Address: 09h
Reset Value: 8'b 0000_0001
Type: Read/Write

Bit	Name	Default	Description
7:3	Reserve	00000	Reset condition: 00000 Not Use
2	MODE_SEL	0	Reset condition: 0 0: COMP_I/DET will works as COMP_I; COMP_O/INT will work as COMP_O 1: COMP_I/DET will works as DET; COMP_O/INT will work as INT CC_IN will behaves as descripted in "Device attached and detach detection" accordingly
1	EN_OVP	1	0b: Over Voltage Protection is Disabled 1b: Over Voltage Protection is Enabled (DEFAULT)
0	EN_OCP	1	0b: Over Current Protection is Disabled 1b: Over Current Protection is Enabled (DEFAULT)

OVP OCP PROTECTION STATUS

Address: 0Bh
Reset Value: 8'b 0010_1100
Type: Read/Write

Bit	Name	Default	Description
7:6	Reserved	00	Do Not Use
5	USB_OVP	1	0b: Over Voltage Protection on DP_R and DN_L is Disabled 1b: Over Voltage Protection on DP_R and DN_L is Enabled
4	GSBU_OVP	0	0b: Over Voltage Protection on GSBUx is Disabled 1b: Over Voltage Protection on GSBUx is Enabled
3	SBU1_OVP	1	0b: Over Voltage Protection on SBU1 is Disabled 1b: Over Voltage Protection on SBU1 is Enabled
2	SBU2_OVP	1	0b: Over Voltage Protection on SBU2 is Disabled 1b: Over Voltage Protection on SBU2 is Enabled
1	OCP1	0	0b: Over Current Protection from SBU1 to AGND is Disabled (DEFAULT) 1b: SBU1_STAT = 010b, Over Current Protection from SBU1 to AGND is Enabled
0	OCP2	0	0b: Over Current Protection from SBU2 to AGND is Disabled (DEFAULT) 1b: SBU2_STAT = 010b, Over Current Protection from SBU2 to AGND is Enabled

CURR SOURCE SET

Address: 0Ch
Reset Value: 8'b 0000_0010
Type: Read/Write

Bit	Name	Default	Description
7:2	Reserved	000000	Do Not Use
1:0	CURR_SOURCE_SET	10	00b: 20 μA 01b: 100 μA 10b: 700 μA (DEFAULT) 11b: 1500 μA

L2R_EN_DELAY

Address: 0Dh
Reset Value: 8'b 0000_0000
Type: Read/Write

Bit	Name	Default	Description
7:0	L2R_EN_DELAY	0000000	00000000b: = 0 μs (DEFAULT) 00000001b: = 100 μs ..... 11111111b: = 25500 μs Increment size is 100 μs per bit

MIC2L_EN_DELAY

Address: 0Eh
Reset Value: 8' 0000_0000
Type: Read/Write

Bit	Name	Default	Description
7:0	MIC2L_EN_DELAY	0000000	00000000b: = 0 μs (DEFAULT) 00000001b: = 100 μs ..... 11111111b: = 25500 μs Increment size is 100 μs per bit

SENSE2L_EN_DELAY
Address: 0Fh
Reset Value: 8'b 0000_0000
Type: Read/Write

Bit	Name	Default	Description
7:0	SENSE2L_EN_DELAY	0000000	00000000b: = 0 μs (DEFAULT) 00000001b: = 100 μs ..... 11111111b: = 25500 μs Increment size is 100 μs per bit

AGND2L_EN_DELAY
Address: 10h
Reset Value: 8'b 0000_0000
Type: Read/Write

Bit	Name	Default	Description
7:0	AGND2L_EN_DELAY	0000000	00000000b: = 0 μs (DEFAULT) 00000001b: = 100 μs ..... 11111111b: = 25500 μs Increment size is 100 μs per bit

AUDIO ACCESSORY STATUS
Address: 11h
Reset Value: 8'b 0000_0001
Type: Read

Bit	Name	Default	Description
7:2	Reserved	000000	Reserved
1	CC_IN_STAT	0	0b: CC_IN = Low 1b: CC_IN = High
0	DET_STAT	1	0b: DET output is LOW 1b: DET output is High−Z

FUNCTION ENABLE
Address: 12h
Reset Value: 8'b 1100_0000
Type: Read/Write

Bit	Name	Default	Description
7:6	DET_FUNCT	11	DET Output Configuration 00b: Type−C Attach Detection 01b: Audio Accessory Attach Detection 10b: Audio Accessory Detach Detection from 0b to 1b 11b: Disabled, DET = High−Z (DEFAULT)
5	RES_DET_RANGE	0	Resistor Detection Range Setting 0b: 1 kΩ to 256 kΩ 1b: 10 kΩ to 2560 kΩ
4	HIZ_ACC_DET	0	High Impedance Audio Accessory Detection 0b: Automatic Hi−Z Accessory Detection is disabled 1b: Automatic Hi−Z Accessory Detection is enabled
3	EN_AT_RESET	0	1: Enable auto reset function 0: disable auto reset function
2	MIC_AUTO_OFF	0	0b: MIC Switch Auto Off Function is Disabled 1b: MIC Switch Auto Off Function is Enabled
1	RES_DETECT	0	Resistance Detection Enabled 0b: Resistance Detection is Disabled 1b: Resistance Detection is Enabled (automatically reset to 0b by I_LOW_RES = 1b)
0	AUDIO_JACK_DET	0	Audio Jack Detection and Configuration Enabled 0b: Audio Jack Detection is Disabled 1b: Audio Jack Detection and Configuration is Enabled (automatically reset to 0b by I_AUDIO_JACK_DET = 1b)

RES DETECTION PIN SETTING
Address: 13h
Reset Value: 8'b 0000_0001
Type: Read/Write

Bit	Name	Default	Description
7:3	Reserved	00000	Do Not Use
2:0	RES_PIN_SEL	001	000b: Not Valid 001b: DP_R (DEFAULT) 010b: DN_L 011b: SBU1 100b: SBU2 101b to 111b: Not Valid RES_PIN_SEL must be set prior to setting RES_DETECT to Enabled

Recommend user to select the pin first before setting the RES detection pin enable.

RES VALUE
Address: 14h
Reset Value: 8'b 1111_1111
Type: Read

Bit	Name	Default	Description
7:0	RES_VALUE	11111111	0000_0000: R < 1 kΩ …… 1111_1111: R > 300 kΩ

RES DETECTION THRESHOLD

Address: 15h
Reset Value: 8'b 0001_0110
Type: Read

Bit	Name	Default	Description
7:0	RES_DET_THRESH	00010110	Selection by 1 kΩ per step if Reg 12h [5] = 0 Selection by 10 kΩ per step if Reg 12h [5] = 1 Default Value = 22 kΩ 0000_0000: 1 kΩ / 10 kΩ ..... 1111_1111: 256 kΩ / 2560 kΩ

AUTO REST & DET_INTV

Address: 16h
Reset Value: 8'b 0000_1100
Type: Read/ Write

Bit	Name	Default	Description
7:5	Reserved	000	Do Not Use
4	TIMER_RESET	0	1: Reset the Timer for auto reset function, and it will be changed back to "0" automatically once timer was rested 0: Not reset the timer for auto reset function
3:2	AUTO_RESET_TIMER	11	00: 10 s 01: 30 s 10: 60 s 11: 5 s
1:0	RES_DET_INTV	00	00b: One Time Detection 01b: Detection is performed every 100 ms 10b: Detection is performed every 1 s 11b: Detection is performed every 10 s

AUDIO JACK STATUS

Address: 17h
Reset Value: 8'b 0000_0001
Type: Read

Bit	Name	Default	Description
7:5	Reserved	000	Do Not Use
4	UNKNOWN_AUDIO_ACC	0	0b: OTHER 1b: Unknown Audio Accessory
3	4POLE_A	0	0b: OTHER 1b: 4 Pole Audio, SBU2 to MIC, SBU1 to AGND
2	4POLE_B	0	0b: OTHER 1b: 4 Pole Audio, SBU1 to MIC, SBU2 to AGND
1	3POLE	0	0b: OTHER 1b: 3 Pole Audio
0	NO_AUDIO_ACC	1	0b: Audio Accessory Attached 1b: No Audio Accessory

RES DETECTION /AUDIO JACK DETECTION INTERRUPT FLAG

Address: 18h
Reset Value: 8'b 0000_0000
Type: Read Clear

Bit	Name	Default	Description
7:5	Reserved	000	Do Not Use
4	I_CC/IN_CHG	0	0b: CC_IN change has not been detected 1b: CC_IN change has been detected
3	I_DET_FUNCT	0	Audio Accessory Detach has occurred 0b: DET_FUNCT = 00b, 01b, 11b, or DET_FUNCT = 10b and DET_STAT = 1b 1b: DET_FUNCT = 10b and DET_STAT = 0b Clearing I DET FUNCT will return the DET output to High−Z
2	I_AUDIO_JACK_DET	0	0b: Audio Jack Detection and Configuration has not occurred 1b: Audio Jack Detection and Configuration has occurred
1	I_LOW_RES	0	0b: A Resistance < RES_DET_THRESH has not been detected 1b: A Resistance < RES_DET_THRESH has been detected
0	I_RES_DET_COMP	0	0b: Resistance Detection has not been completed 1b: Resistance Detection has been completed

RES /AUDIO JACK DETECTION INTERRUPT MASK

Address: 19h
Reset Value: 8'b 0001_0000
Type: Read/Write

Bit	Name	Default	Description
7:5	Reserved	000	Do Not Use
4	M_CC/IN_CHG	1	0b: Do not mask CC/IN_CHG interrupt 1b: Mask CC/IN_CHG interrupt
3	M_DET_FUNCT	0	0b: Do not mask Audio Accessory Detach interrupt 1b: Mask Audio Accessory Detach interrupt
2	M_AUDIO_JACK_DET	0	0b: Do not mask Audio Jack Detection and Configuration interrupt 1b: Mask Audio Jack Detection and Configuration interrupt
1	M_LOW_RES	0	0b: Do not mask Low Resistance Detection interrupt 1b: Mask Low Resistance Detection interrupt
0	M_RES_DET_COMP	0	0b: Do not mask Resistance Detection completed interrupt 1b: Mask Resistance Detection completed interrupt

AUDIO JACK DETECTION REG1 VALUE

Address: 1Ah
Reset Value: 8'b 1111_1111
Type: Read

Bit	Name	Default	Description
7:0	AUDIO_JACK_DET1	11111111	Voltage from resistance between SBU1 and SBU2 (SBU2 = ground) 00000000b: = 0 V ..... 11111111b: = 2.4 V Increment is 9.375 mV per bit. Resistance is calculated as AUDIO_JACK_DET1 / CURR_SOURCE_SET

AUDIO JACK DETECTION REG2 VALUE

Address: 1Bh
Reset Value: 8'b 1111_1111
Type: Read

Bit	Name	Default	Description
7:0	AUDIO_JACK_DET2	11111111	Voltage from resistance between SBU2 and SBU1 (SBU1 = ground) 00000000b: = 0 V ..... 11111111b: = 2.4 V Increment is 9.375 mV per bit. Resistance is calculated as AUDIO_JACK_DET2 / CURR_SOURCE_SET

MIC DETECTION THRESHOLD LOW

Address: 1Ch
Reset Value: 8'b 0010_0000
Type: Read/Write

Bit	Name	Default	Description
7:0	MIC_DET_TH_LOW	00100000	00000000b: = 0 mV ..... 00100000b: = 300 mV (DEFAULT) ..... 11111111b: = 2.4 V Increment = 9.375 mV per bit

MIC DETECTION THRESHOLD UP

Address: 1Dh
Reset Value: 8'b 1111_1111
Type: Read/Write

Bit	Name	Default	Description
7:0	MIC_DET_TH_UP	11111111	00000000b: = 0 mV ..... 00100000b: = 300 mV ..... 11111111b: = 2.4 V (DEFAULT) Increment = 9.375 mV per bit

I2C RESET

Address: 1Eh
Reset Value: 8'b 0000_0000
Type: W/C

Bit	Name	Default	Description
7:1	Reserved	0000000	Do Not Use
0	I2C_RESET	0	0b: DEFAULT 1b: Reset all I2C Register Values to Default

APPLICATION INFORMATION

I2C Address

The I2C Address can be selected by routing the SDA/SCL signals per the table below. The FSA4486 will detect the clock and automatically configure the I/O and address. The I^2C interface will operate with VDDIO pull up from 1.2 V to 1.8 V.

Table 9.

SDA	SCL	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SDA1	SCL1	1	0	0	0	0	1	0	R/W
SDA2	SCL2	1	0	0	0	0	1	1	R/W

Over Voltage Protection

FSA4486 features over voltage protection (OVP) on the receptacle side pins. This will automatically switch open the internal signal routing path if the input voltage exceeds the OVP threshold. If OVP has occurred an interrupt signal will be send using the INT signal. The OVP_INTERRUPT register will indicate which pin had the OVP event. If the over voltage is no longer present, indicated by the OVP_STAT register, the signal path can be restored automatically.

Over Current Protection

When the EN_OCP register is set to Enable and the SBUx switch is closed to AGND Over Current Protection (OCP) will be enabled. OCP monitors the voltage drop from SBUx to AGND across the closed switch to limit the current to 1.5 A for 500 μs. This will prevent a short from VBUS to AGND through SBUx. OCP will not automatically reset. When an OCP event occurs an interrupt will be sent to the processor. The interrupt is cleared by reading the I_OCP_AGND register. The SBUx to AGND switch can be closed after an OCP event by setting AGND_EN = 1b.

MIC Switch Auto−Off

MIC switch auto−off is controlled by the MIC_AUTO_OFF register (12h, Bit 2). If enabled, when the port is configured for audio (L, R, MIC, AGND switches are closed) and a detach is detected (CC_IN > 0.27 V when mode_sel = 1 ‖ CC_IN > 1.5 V when mode_sel = 0 or CC_IN_STAT transitions from 0 to 1) the receptacle side of the MIC switch will connect to ground for 50 μs prior to becoming high impedance.

Mode Selection For Device Attach and Detach Detection

If Bit[2] of 0x09h register is set to “1”, then COMP_I/DET will works as DET, COMP_O/INT will works as INT, CC_IN will go with 0.27/0.24 V threshold, and device attach and detach will behaves as following:

Device attach and detach detection will be performed by the CC_IN input and indicated by the CC_IN_STAT register (11h, Bit 2). Attach and detach detection can also be indicated by the DET output. DET is an Open Drain user configurable attach/detach detection output. It can be configured or disabled from the I2C register DET_FUNCT. The DET output once triggered can be cleared by reading the Detection Interrupt Register I_DET_FUNCT. When configured for Type−C or Audio Accessory attach detection DET will clear automatically when the Type−C device or audio accessory is detached.

If Bit[2] of 0x09h register is set to “0”, then COMP_I/DET will works as COMP_I which go with 0.27/0.24 V threshold, COMP_O/INT will works as COMP_O. and CC_IN go with 1.5/1.2 V threshold and only links with Mic_auto_off function when CC_IN > 1.5 V, not links with DET anymore.

when COMP_I > 0.27 V, COMP_O = High−z

when COMP_I < 0.24 V, COMP_O = Low

when CC_IN > 1.5 V, MIC_AUTO_OFF being triggered

Table 10.

Value	DET_FUNCT	Description
00b	00b: Type−C Attach Detection, DET = LOW if CC_IN_STAT = 0b, I_CC_IN_CHG will be triggered once CC_IN_STAT changed from 1 to 0 or 0 to 1.	Type−C Attach/Detach Detect
01b	01b: Audio Accessory Present Detection, DET = LOW if NO_AUDIO_ACC = 0b	Audio Accessory Present Detect
10b	10b: Audio Accessory Detach Detection, DET = LOW if CC_IN_STAT transitions from 0b to 1b	Audio Accessory Detach Detect
11b	Disabled, DET = Hi−Z (DEFAULT)	Disabled

Audio Ground Detection and Configuration

Automatic audio jack detection is enabled by the AUDIO_JACK_DET register (12h, Bit 0). When the DN_L, DP_R, and AGND switches are enabled in the SWITCH_EN register (04h) and AUDIO_JACK_DET = 1b, automatic ground configuration will be performed when an audio accessory is detected. The SBU switches will be configured for audio ground and MIC based on the plug orientation.

During detection and configuration, the R, L, Sense, MIC and AGND switches will be open. After detection and configuration, the R and L switches will close according to the switch configuration and timing settings. MIC, Sense and AGND will close according to detection results and timing control settings.

The FSA4486 also has an option to perform detection of High Impedance Audio Accessories which is enabled by the HZ_ACC_DET register (12h, Bit 4). When enabled, high impedance detection will be performed after normal detection has failed to detect a resistance on either SBUx input or AUDIO_JACK_DET1 = AUDIO_JACK_DET2. It will detect any resistance greater than 15k Ohms and less than 120 kΩ.

Moisture Detection

The moisture detection function is controlled the RES_DETECT register (12h, Bit 1). It will detect moisture or any foreign object that creates resistance between the receptacle side pins and ground. During resistance detection, the switch associated with the pin will be open. The detection result will be saved in the RES_VALUE register (14h). The measurement range is from 1 kΩ to 2.56 MΩ and is controlled by the RES_DET_RANGE register (12h, Bit 5). Detection can be performed manually, or an automatic detection interval can be set to 100 ms, 1 s or 10 s by the RED_DET_INTV register (16h).

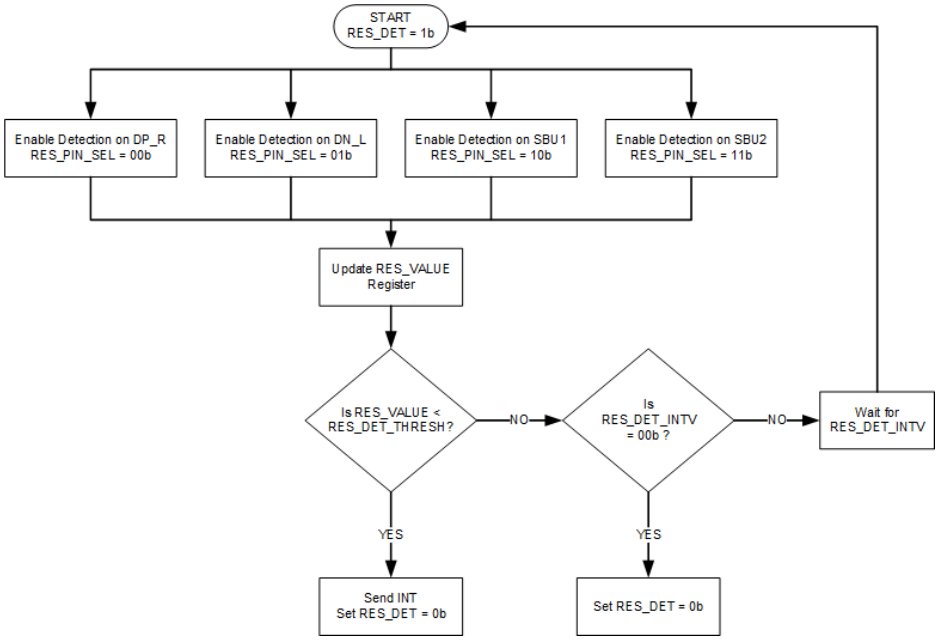


Figure 3. Flow for RES_DET

Auto Reset Function

The function will be active during control bit 0x12h bit[3] = 1.When the bit[4] of register DET_INTV not being written before timer (can be set through bit[2][3]) out, FSA4486 will be reset automatically, and all of channel restore to default state including USB switch will be switched to DP/DN for logging purpose during debugging scenarios, even AP hang up happens when FSA4486 stays audio or other mode.

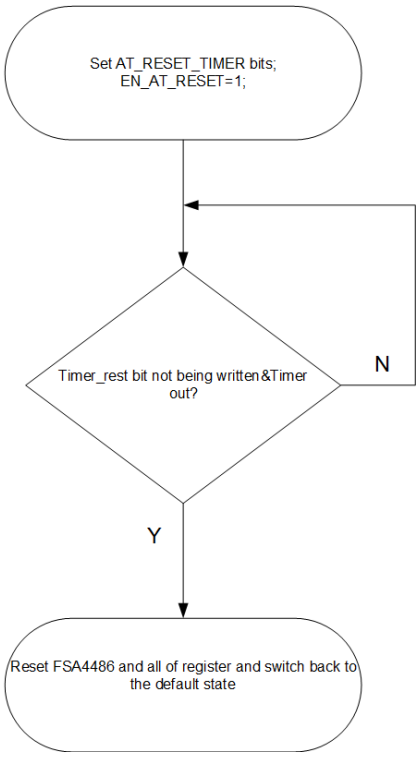
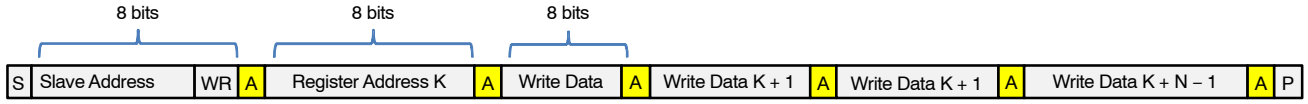


Figure 4. Auto Reset

I²C INTERFACE

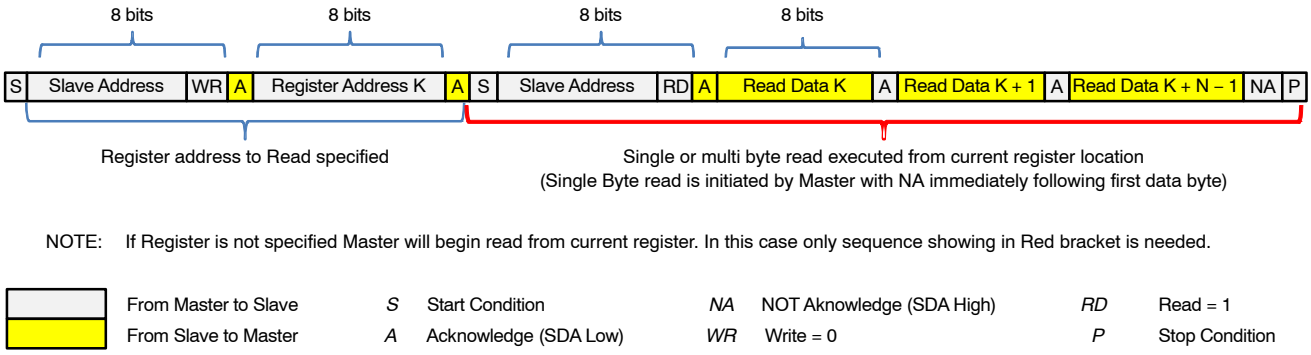
The FSA4486 includes a full I²C slave controller. The I²C slave fully complies with the I²C specification version 2.1 requirements. This block is designed for fast mode, 400 kHz, signals.

Examples of an I²C write and read sequence are shown in below figures respectively.



NOTE: Single Byte read is initiated by Master with P immediately following first data byte.

Figure 5. I²C Write Example



NOTE: If Register is not specified Master will begin read from current register. In this case only sequence showing in Red bracket is needed.

	From Master to Slave	*S*	Start Condition	*NA*	NOT Aknowledge (SDA High)	*RD*	Read = 1
	From Slave to Master	*A*	Acknowledge (SDA Low)	*WR*	Write = 0	*P*	Stop Condition

Figure 6. I²C Read Example

Test Diagrams

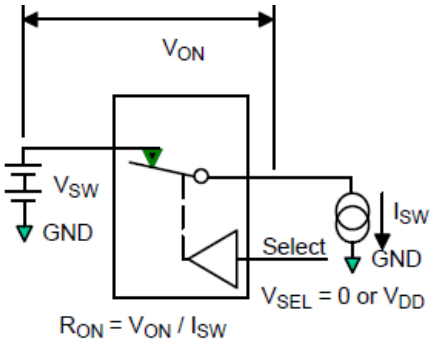


Figure 7. On Resistance

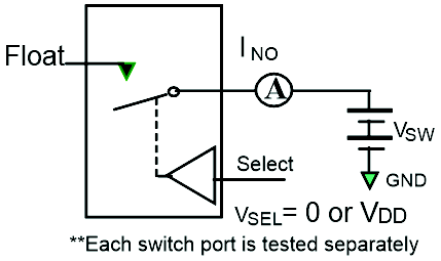


Figure 8. Off Leakage (Ioz)

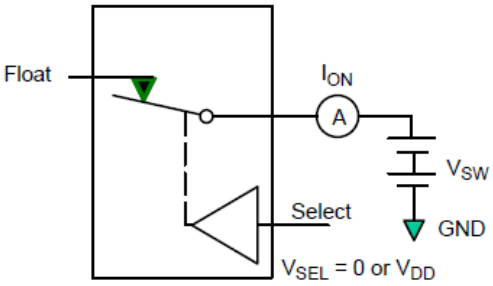


Figure 9. On Leakage

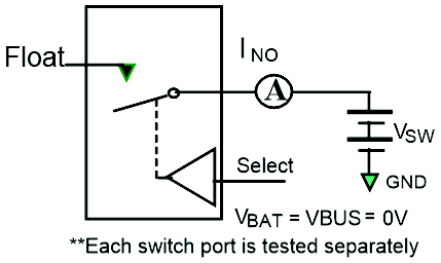


Figure 10. Power Off Leakage (Ioff)

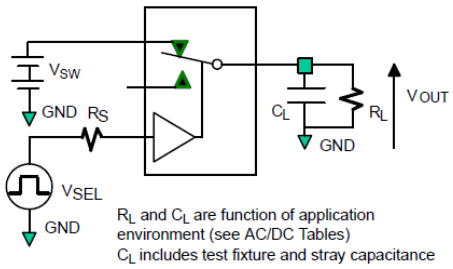


Figure 11. Test Circuit Load

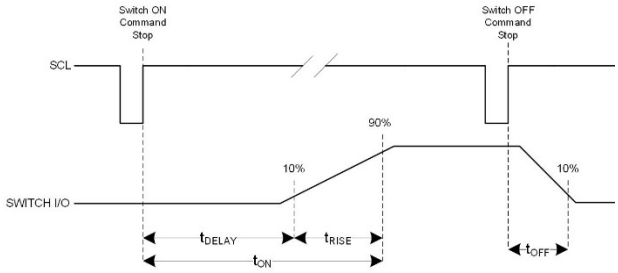


Figure 12. Turn On/Off Waveforms under Manual Mode

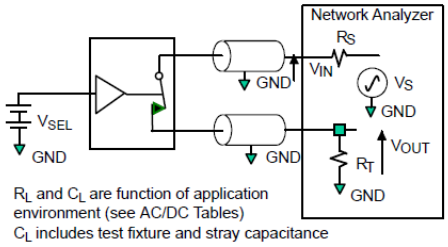


Figure 13. Bandwidth

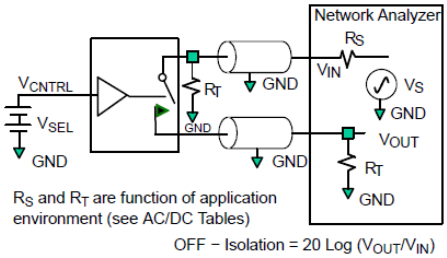


Figure 14. Channel Off Isolation

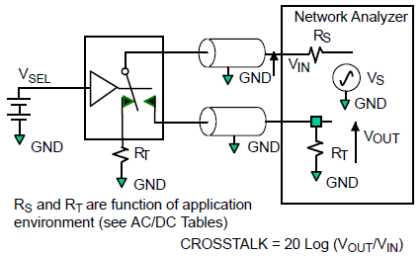


Figure 15. Adjacent Channel Crosstalk

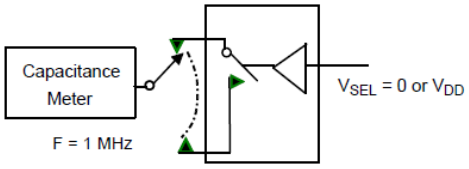


Figure 16. Channel Off Capacitance

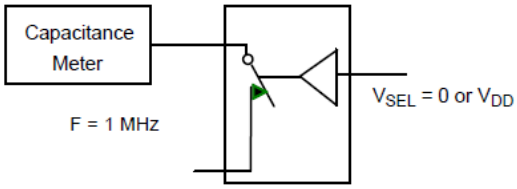


Figure 17. Channel On Capacitance

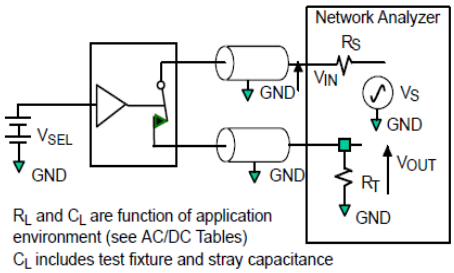


Figure 18. Total Harmonic Distortion (THD+N)

ORDERING INFORMATION

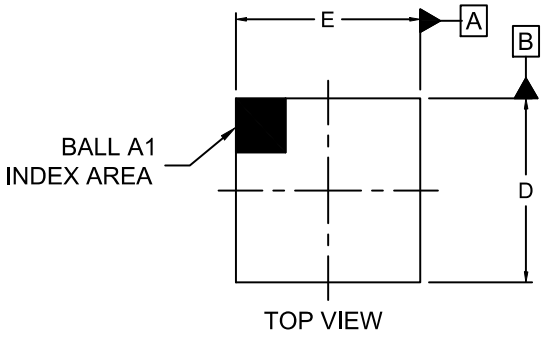
Part Number	Marking	Operating Temperature	Package Type	Shipping†
FSA4486UCX	6E	–40 to +85°C	25–Ball WLCSP, Non–JEDEC 2.24 x 2.28 mm, 0.4 mm Pitch (Pb–Free)	3000 / Tape & Reel

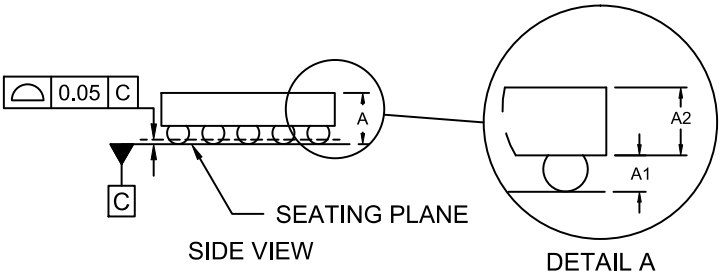
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

onsemi is licensed by the Philips Corporation to carry the I^2C bus protocol.

WLCSP25 2.24x2.28x0.586
CASE 567UZ
ISSUE B

DATE 03 JAN 2018

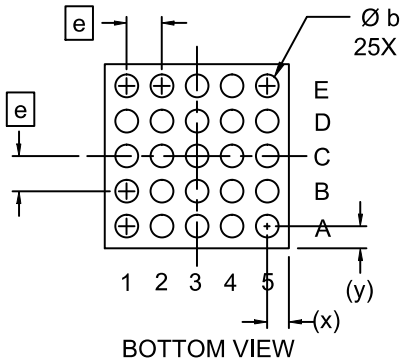


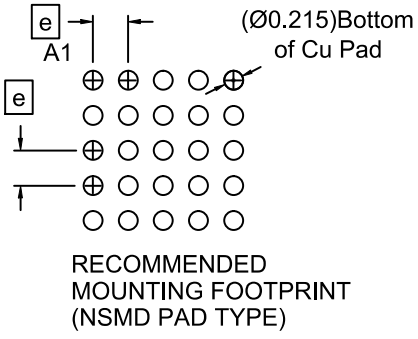


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C APPLIES TO THE SPHERICAL CROWN OF THE SOLDER BALLS

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.547	0.586	0.625
A1	0.178	0.208	0.238
A2	0.360	0.378	0.396
b	0.24	0.26	0.28
D	2.250	2.280	2.310
E	2.210	2.240	2.270
e	0.40 BSC		
x	0.305	0.320	0.335
y	0.325	0.340	0.355





ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales