DATA SHEET
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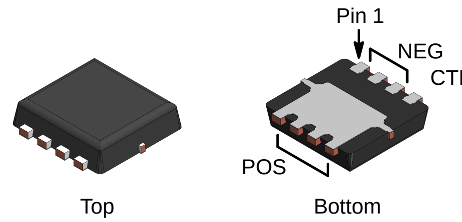
High-Side Reverse Bias / Reverse Polarity Protector with Integrated Over Voltage Transient Suppression

FR014H5JZ



WDFN8 3.3 x 3.3, 0.65P
(MLP 3.3 x 3.3)
CASE 511DR

Description

Reverse bias is an increasingly common fault event that may be generated by user error, improperly installed batteries, automotive environments, erroneous connections to third−party chargers, negative “hot plug” transients, inductive transients, and readily available negatively biased rouge USB chargers.

onsemi circuit protection is proud to offer a new type of reverse bias protection devices. The FR devices are low resistance, series switches that, in the event of a reverse bias condition, shut off power and block the negative voltage to help protect downstream circuits.

The FR devices are optimized for the application to offer best in class reverse bias protection and voltage capabilities while minimizing size, series voltage drop, and normal operating power consumption.

In the event of a reverse bias application, FR014H5JZ devices effectively provide a full voltage block and can easily protect −0.3 V rated silicon.

From a power perspective, in normal bias, a 14 mΩ FR device in a 1.5 A application will generate only 21 mV of voltage drop or 32 mW of power loss. In reverse bias, FR devices dissipate less then 20 μW in a 16 V reverse bias event. This type of performance is not possible with a diode solution.

Benefits extend beyond the device. Due to low power dissipation, not only is the device small, but heat sinking requirements and cost can be minimized as well.

Features

- Up to −30 V Reverse−Bias Protection
- Nano Seconds of Reverse−Bias Blocking Response Time
- +32 V 24−Hour “Withstand” Rating
- 14 mΩ Typical Series Resistance at 5 V
- Integrated TVS Over Voltage Suppression
- MLP 3.3 x 3.3 Package Size
- USB Tested and Compatible
- This Device is Pb−Free, Halide Free and is RoHS Compliant

Applications

- USB 1.0, 2.0 and 3.0 Devices
- USB Charging
- Mobile Devices
- Mobile Medical
- POS Systems
- Toys

MARKING DIAGRAM

$Y&Z&2&K
14H

$Y = Logo
&Z = Assembly Plant Code
&2 = 2−Digit Date Code
&K = 2−Digits Lot Run Traceability Code
14H = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

Applications (Continued)

- Any DC Barrel Jack Powered Device
- Any DC Devices subject to Negative Hot Plug or Inductive Transients
- Automotive Peripherals
- Any DC Barrel Jack Powered Device
- Any DC Devices subject to Negative Hot Plug or Inductive Transients

DIAGRAMS

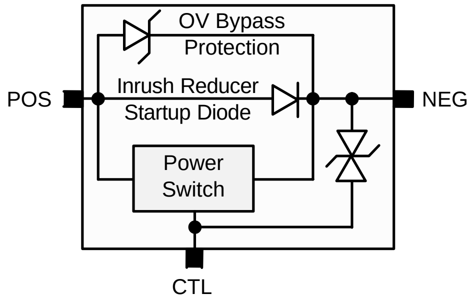


Figure 1. Block Diagram

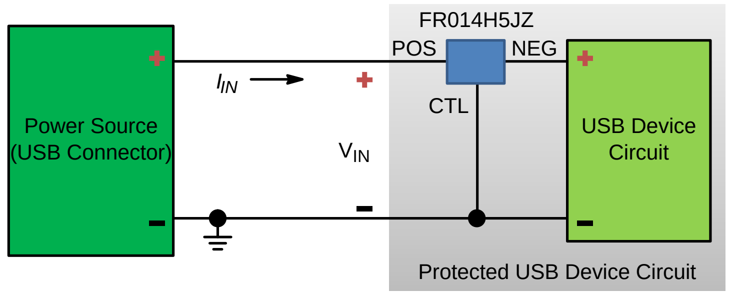


Figure 2. Typical Schematic

PIN CONFIGURATION

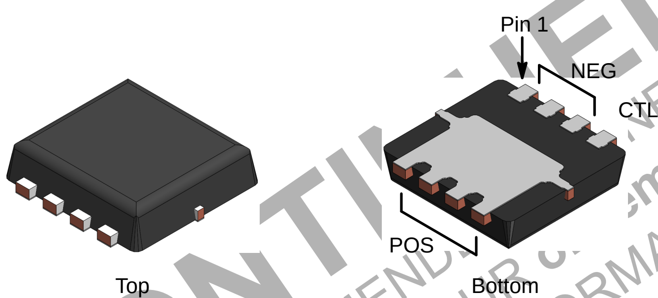


Figure 3. Pin Assignments

PIN DEFINITIONS

Name	Pin	Description
POS	5, 6, 7, 8	The positive terminal of the power source. Current flows into this pin during normal operation.
CTL	4	The control pin of the device. A negative voltage to the POS pin turns the switch on and a positive voltage turns the switch to a high−impedance state.
NEG	1, 2, 3	The positive terminal of the load circuit to be protected. Current flows out of this pin during normal operation.

ABSOLUTE MAXIMUM RATINGS (Values are at T_A = 25°C unless otherwise noted)

Symbol	Parameter				Value	Unit
$V+_{MAX\_OP}$	Steady−State Normal Operating Voltage between POS and CTL Pins (V_{IN} = $V+_{MAX\_OP}$, I_{IN} = 1.5 A, Switch On)				+25	V
$V+_{24}$	24−Hour Normal Operating Voltage Withstand Capability between POS and CTL Pins (V_{IN} = $V+_{24}$, I_{IN} = 1.5 A, Switch On) (Note 1)				+32	
$V-_{MAX\_OP}$	Steady−State Reverse Bias Standoff Voltage between POS and CTL Pins (V_{IN} = $V-_{MAX\_OP}$)				−30	
I_{IN}	Input Current	V_{IN} = 5 V, Continuous (Note 2) *(See Figure 4)*			8	A
T_J	Operating Junction Temperature				150	°C
P_D	Power Dissipation	T_C = 25°C			36	W
		T_A = 25°C (Note 2) *(See Figure 4)*			2.3	
I_{DIODE_CONT}	Steady−State Diode Continuous Forward Current from POS to NEG (Note 2) *(See Figure 4)*				2	A
I_{DIODE_PULSE}	Pulsed Diode Forward Current from POS to NEG (300 μs Pulse) (Note 2) *(See Figure 5)*				450	
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22−A114			8	kV
		Charged Device Model, JESD22−C101			2	
		System Model, IEC61000−4−2	NEG is Shorted to CTL and Connected to GND	Contact	8	
				Air	15	
			No External Connection between NEG and CTL	Contact	3	
				Air	4	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The V_{+24} rating is NOT a survival guarantee. It is a statistically calculated survivability reference point taken on qualification devices, where the predicted failure rate is less than 0.01% at the specified voltage for 24 hours. It is intended to indicate the device's ability to withstand transient events that exceed the recommended operating voltage rating. Specification is based on qualification devices tested using accelerated destructive testing at higher voltages, as well as production pulse testing at the V_{+24} level. Production device field life results may vary. Results are also subject to variation based on implementation, environmental considerations, and circuit dynamics. Systems should never be designed with the intent to normally operate at V_{+24} levels. *Contact* ***onsemi*** *for additional information*.
2. The device power dissipation and thermal resistance (R_θ) are characterized with device mounted on the following FR4 printed circuit boards, as shown in Figure 4 and Figure 5.

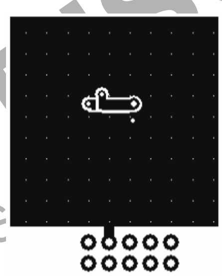


Figure 4. 1 Square Inch of 2−ounce Copper

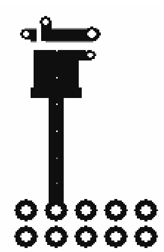


Figure 5. Minimum Pads of 2−ounce Copper

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 2) *(See Figure 4)*	50	

ELECTRICAL CHARACTERISTICS (Values are at T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
POSITIVE BIAS CHARACTERISTICS						
R_{ON}	Device Resistance, Switch On	V_{IN} = +4 V, I_{IN} = 1.5 A	–	18	23	mΩ
		V_{IN} = +5 V, I_{IN} = 1.5 A	–	14	19	
		V_{IN} = +5 V, I_{IN} = 1.5 A, T_J = 125°C	–	20	–	
		V_{IN} = +12 V, I_{IN} = 1.5 A	–	11	14	
V_{ON}	Input Voltage, V_{IN}, at which Voltage at POS, V_{POS}, Reaches a Certain Level at Given Current	I_{IN} = 100 mA, $V_{POS} - V_{NEG}$ = 50 mV, V_{CTL} = 0 V	2.0	2.4	3.0	V
$\Delta V_{ON} / \Delta T_J$	Temperature Coefficient of V_{ON}		–	−3.52	–	mV/°C
V_F	Diode Forward Voltage	$V_{CTL} = V_{NEG}$, I_{DIODE} = 0.1 A, Pulse width < 300 µs	0.57	0.63	0.70	V
I_{BIAS}	Bias Current Flowing into POS Pin During Normal Bias Operation	V_{POS} = 5 V, V_{CTL} = 0 V, No Load	–	30	–	nA
NEGATIVE BIAS CHARACTERISTICS						
$V-_{MAX\_OP}$	Reverse Bias Breakdown Voltage	I_{IN} = −250 µA, $V_{CTL} = V_{NEG}$ = 0 V	–	–	−30	V
$\Delta V-_{MAX\_OP} / \Delta T_J$	Reverse Bias Breakdown Voltage Temperature Coefficient		–	22.5	–	mV/°C
I−	Leakage Current from NEG to POS in Reverse−Bias Condition	V_{POS} = −20 V, $V_{CTL} = V_{NEG}$ = 0 V	–	1	–	µA
t_{RN}	Time to Respond to Negative Bias Condition	V_{CTL} = 5 V, V_{POS} = 0 V, C_{LOAD} = 10 µF, Reverse Bias Startup Inrush Current = 0.2 A	–	–	50	ns
INTEGRATED TVS PERFORMANCE						
V_Z	Breakdown Voltage @ I_T	I_T = 1 mA, 300 µs Pulse	28.5	30	31.2	V
I_R	Leakage Current from NEG to CTL	V_{NEG} = +25 V, V_{CTL} = 0 V	–	1.5	10	µA
		V_{NEG} = −25 V, V_{CTL} = 0 V	–	−1.5	−10	
I_{PPM}	Max Pulse Current from NEG to CTL, IEC61000−4−5 8x20 µs Pulse	$V_{NEG} > V_{CTL}$	–	–	0.8	A
		$V_{NEG} < V_{CTL}$	–	–	−0.9	
V_C	Clamping Voltage form NEG to CTL at I_{PPM}, IEC61000−4−5 8x20 µs Pulse	$V_{NEG} > V_{CTL}$	–	34	–	V
		$V_{NEG} < V_{CTL}$	–	−34	–	
DYNAMIC CHARACTERISTICS						
C_I	Input Capacitance between POS and CTL	V_{IN} = −5 V, $V_{CTL} = V_{NEG}$ = 0 V, f = 1 MHz	–	2440	–	pF
C_S	Switch Capacitance between POS and NEG		–	564	–	
C_O	Output Capacitance between NEG and CTL		–	2526	–	
R_C	Control Internal Resistance		–	3.6	–	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified.)

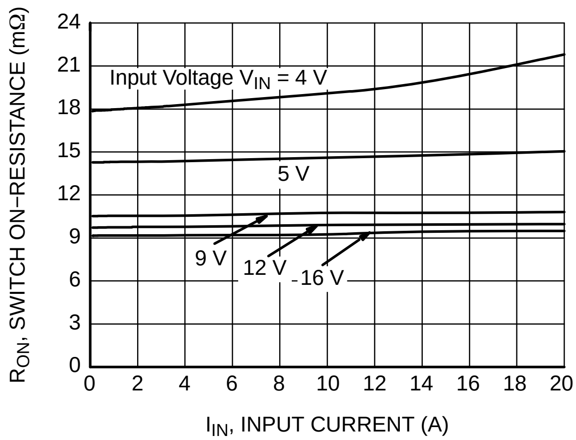


Figure 6. Switch On Resistance vs. Switch Current

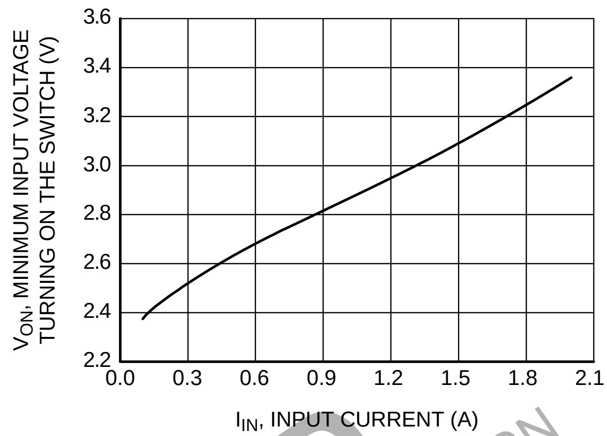


Figure 7. Minimum Input Voltage to Turn On Switch vs. Current at 50 mV Switch Voltage Drop

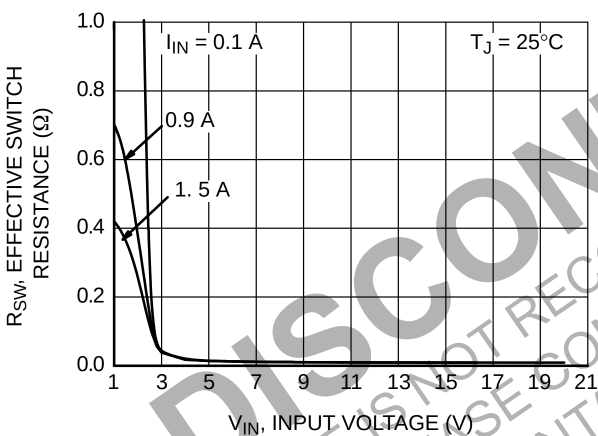


Figure 8. Effective Switch Resistance R_{SW} vs. Input Voltage V_{IN}

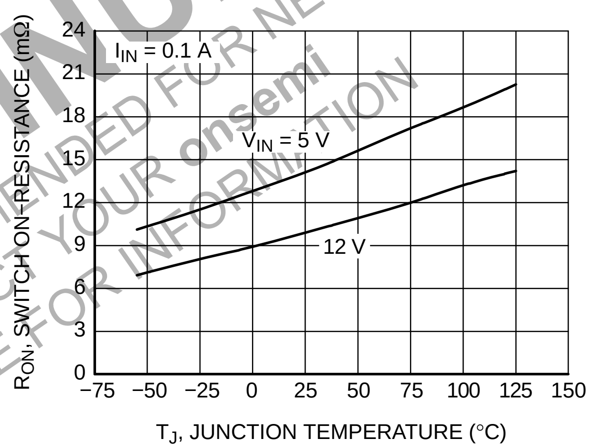


Figure 9. Switch On Resistance vs. Junction Temperature at 0.1 A

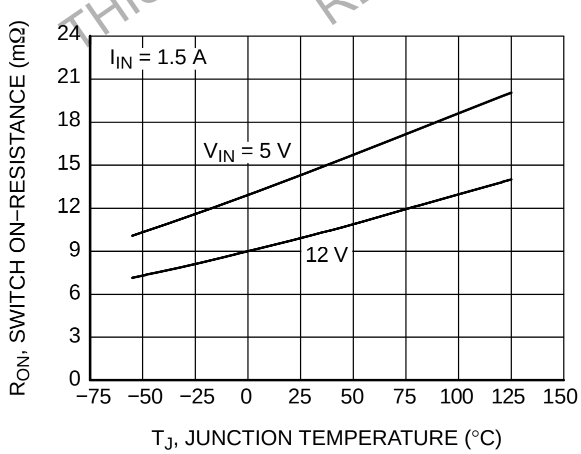


Figure 10. Switch On Resistance vs. Junction Temperature at 1.5 A

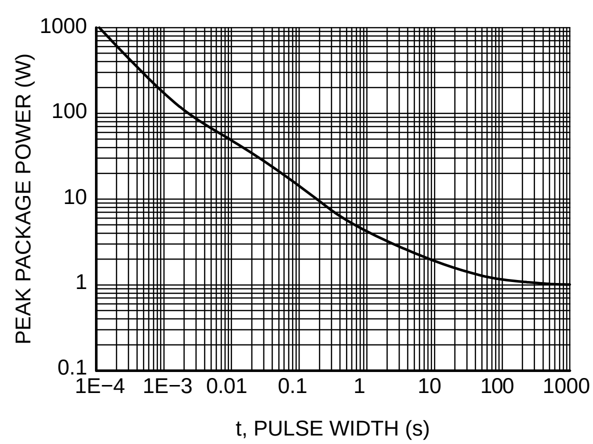


Figure 11. Single−Pulse Maximum Power vs. Time

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified.) (Continued)

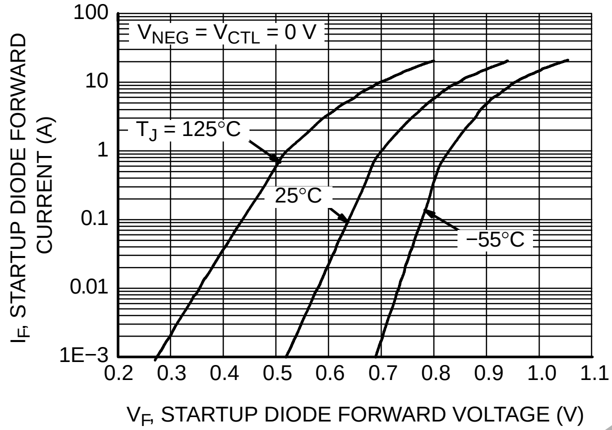


Figure 12. Startup Diode Current vs. Forward Voltage

APPLICATION TEST CONFIGURATIONS

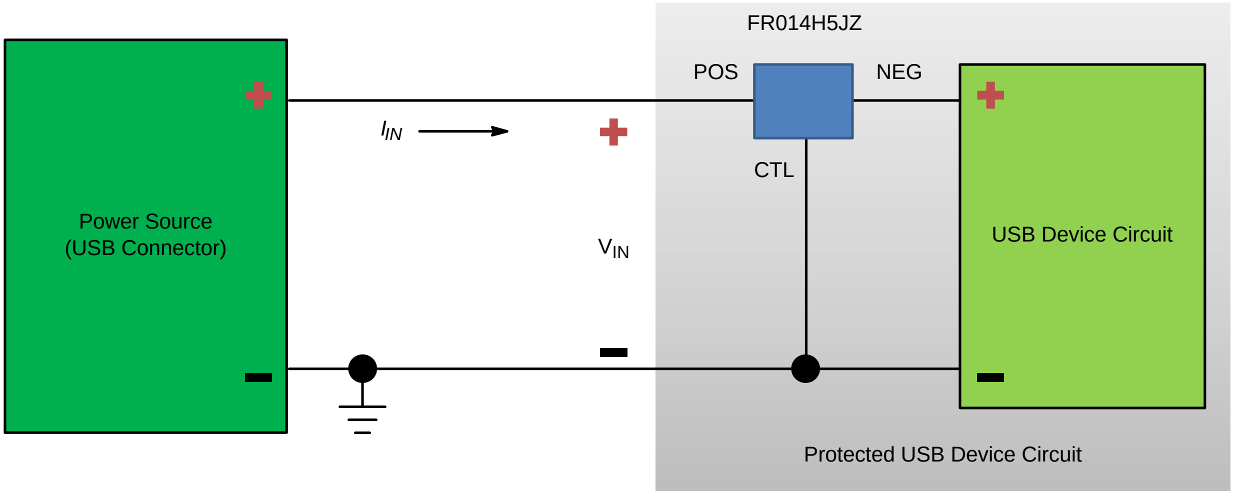


Figure 13. Typical Application Circuit for USB Applications

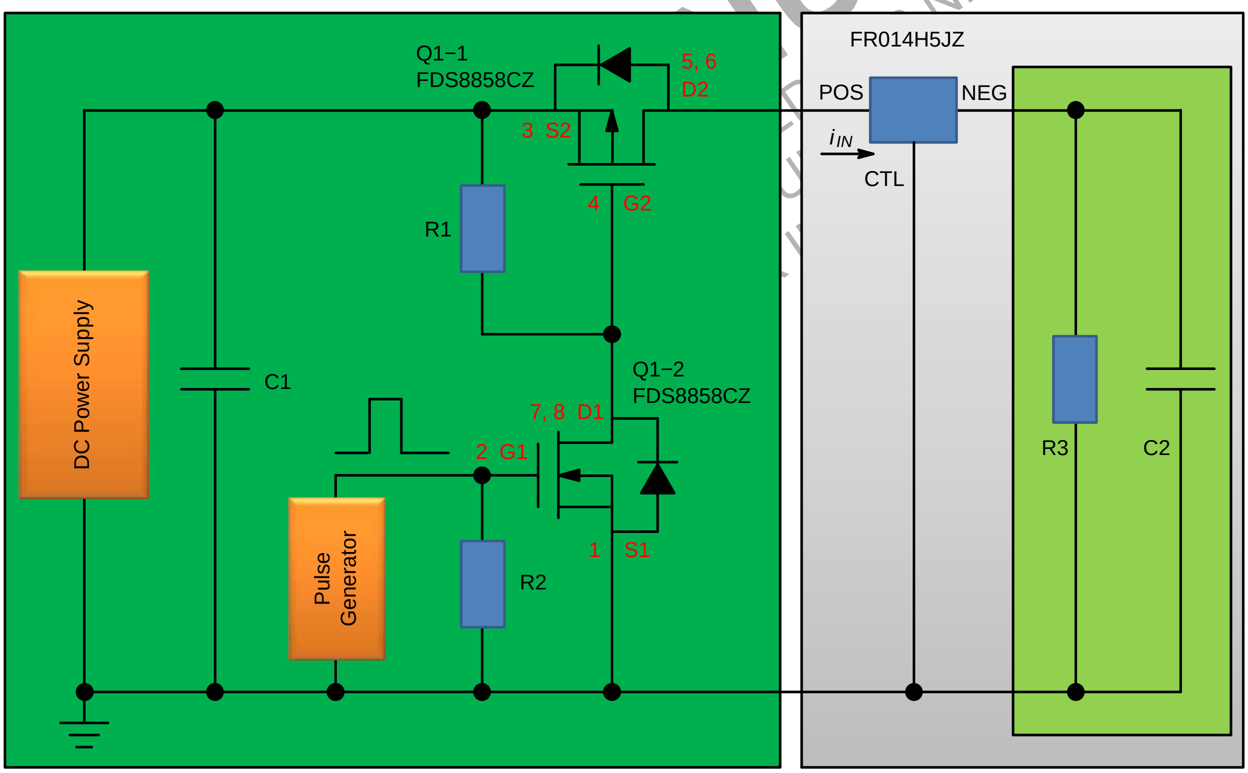


Figure 14. Startup Test Circuit – Normal Bias with FR014H5JZ

APPLICATION TEST CONFIGURATIONS (Continued)

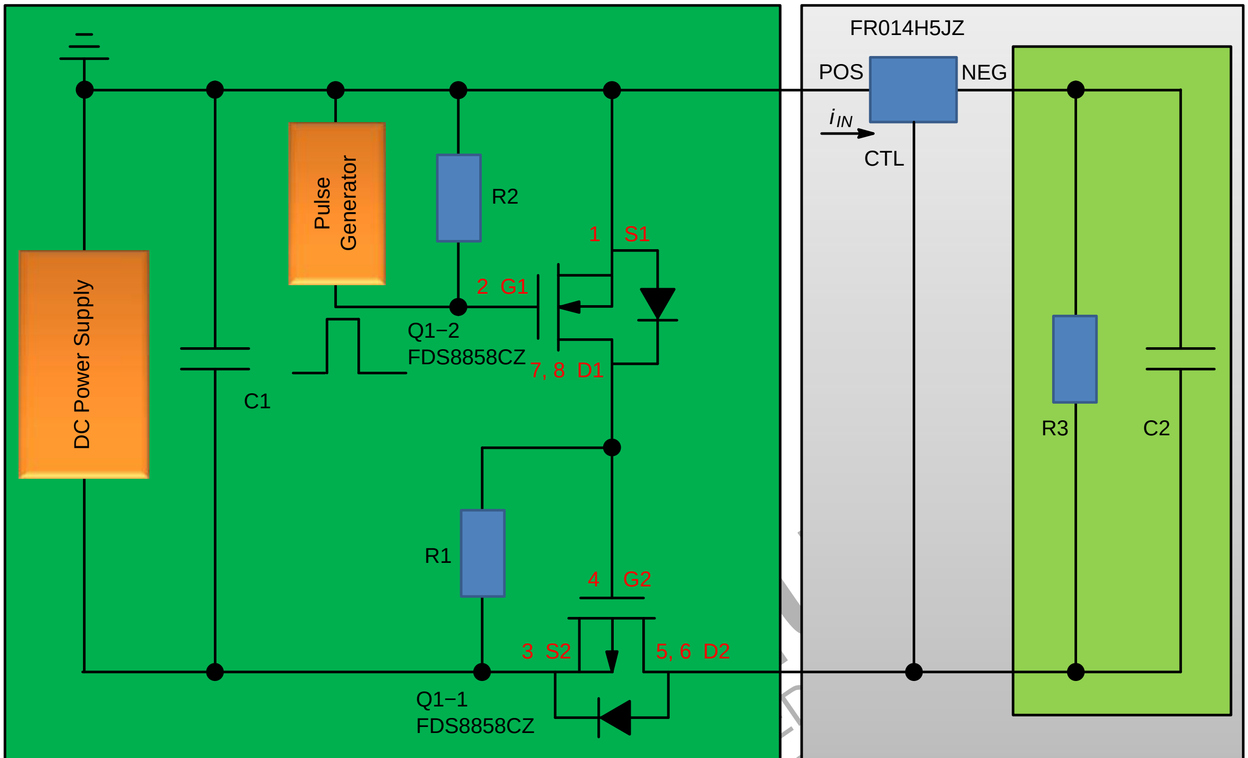


Figure 15. Startup Test Circuit – Reverse Bias with FR014H5JZ

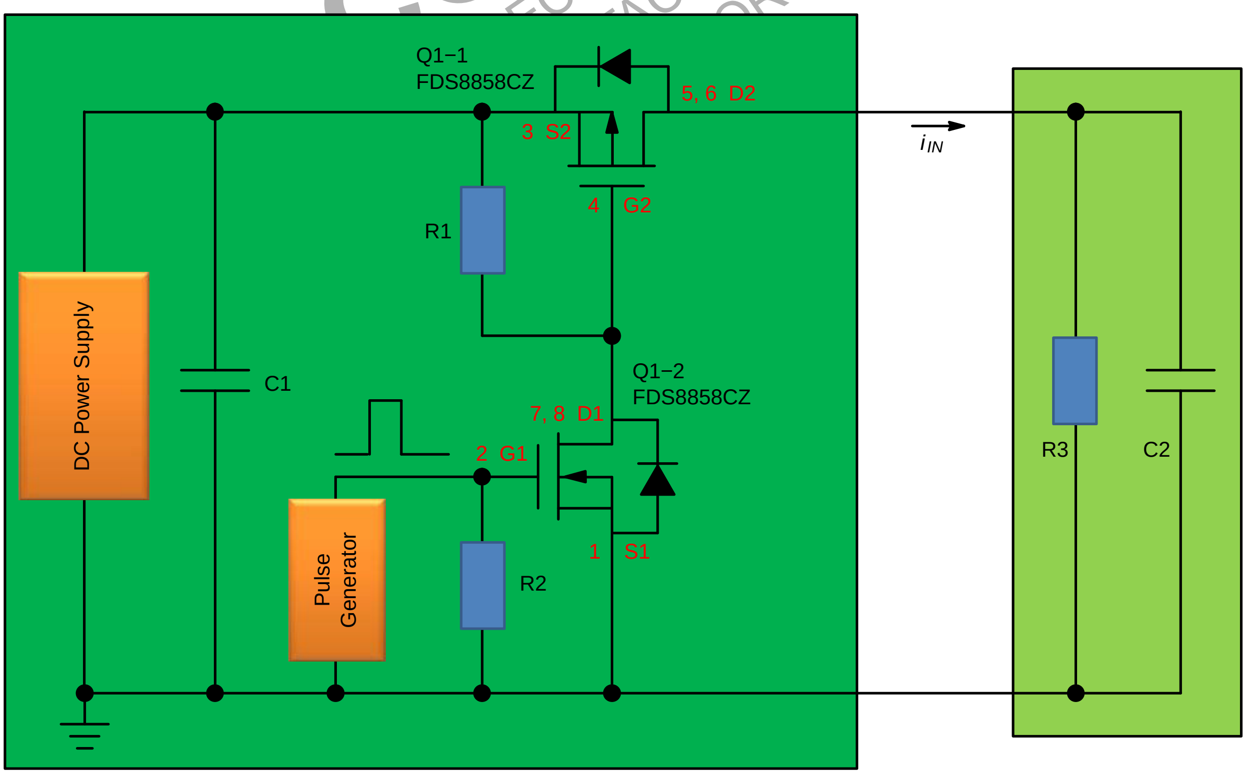


Figure 16. Startup Test Circuit – without FR014H5JZ

TYPICAL APPLICATION WAVEFORMS (Typical USB3.0 conditions)

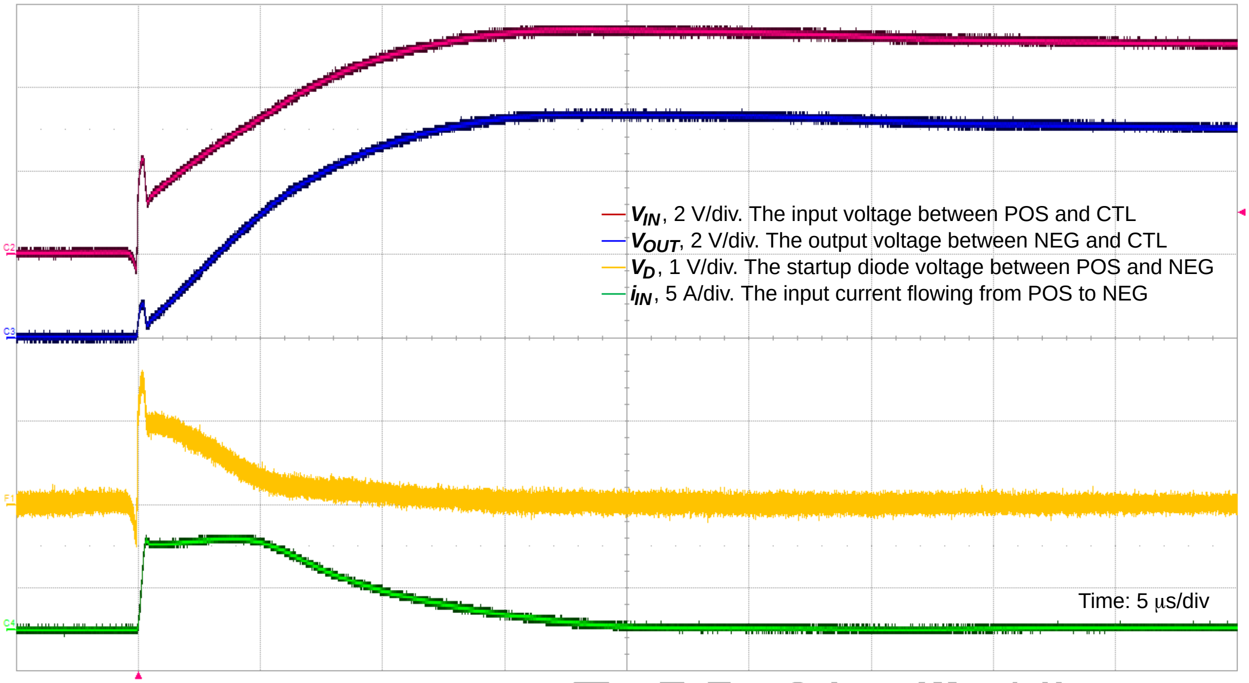


Figure 17. Normal Bias Startup Waveform, DC Power Source = 5 V, C_1 = 100 μF, C_2 = 10 μF, R_1 = R_2 = 10 kΩ, R_3 = 27 Ω

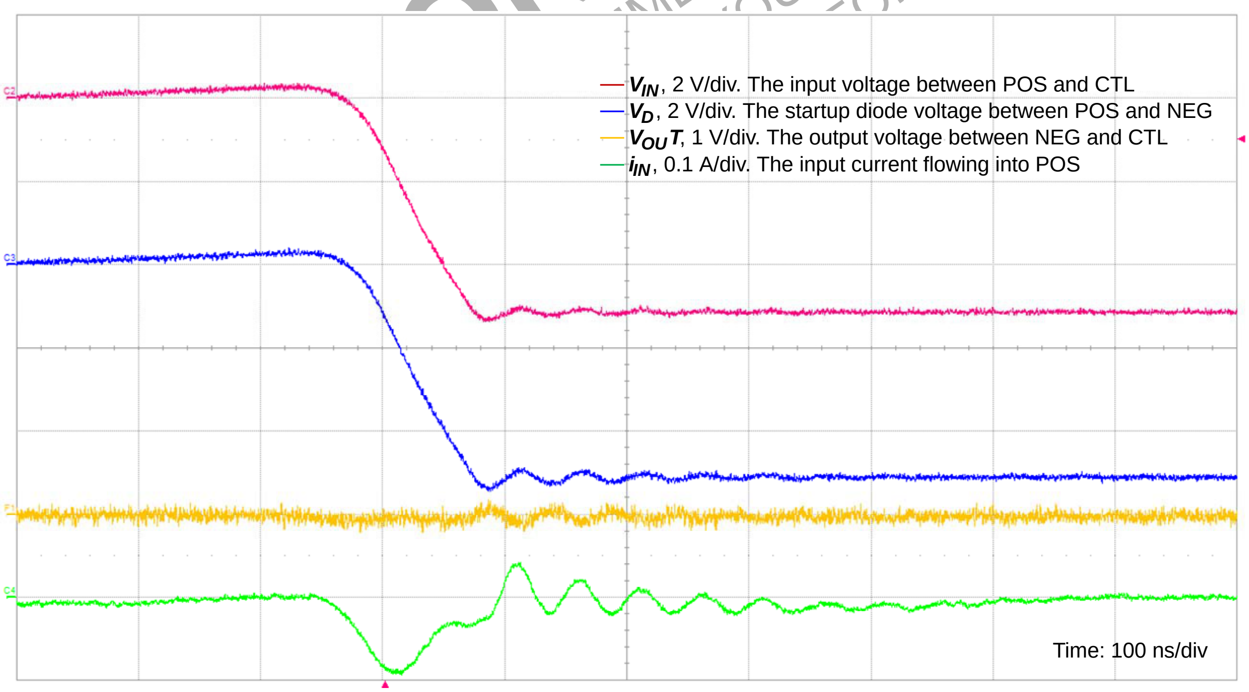


Figure 18. Reverse Bias Startup Waveform, DC Power Source = 5 V, C_1 = 100 μF, C_2 = 10 μF, R_1 = R_2 = 10 kΩ, R_3 = 27 Ω

TYPICAL APPLICATION WAVEFORMS (Typical USB3.0 conditions)

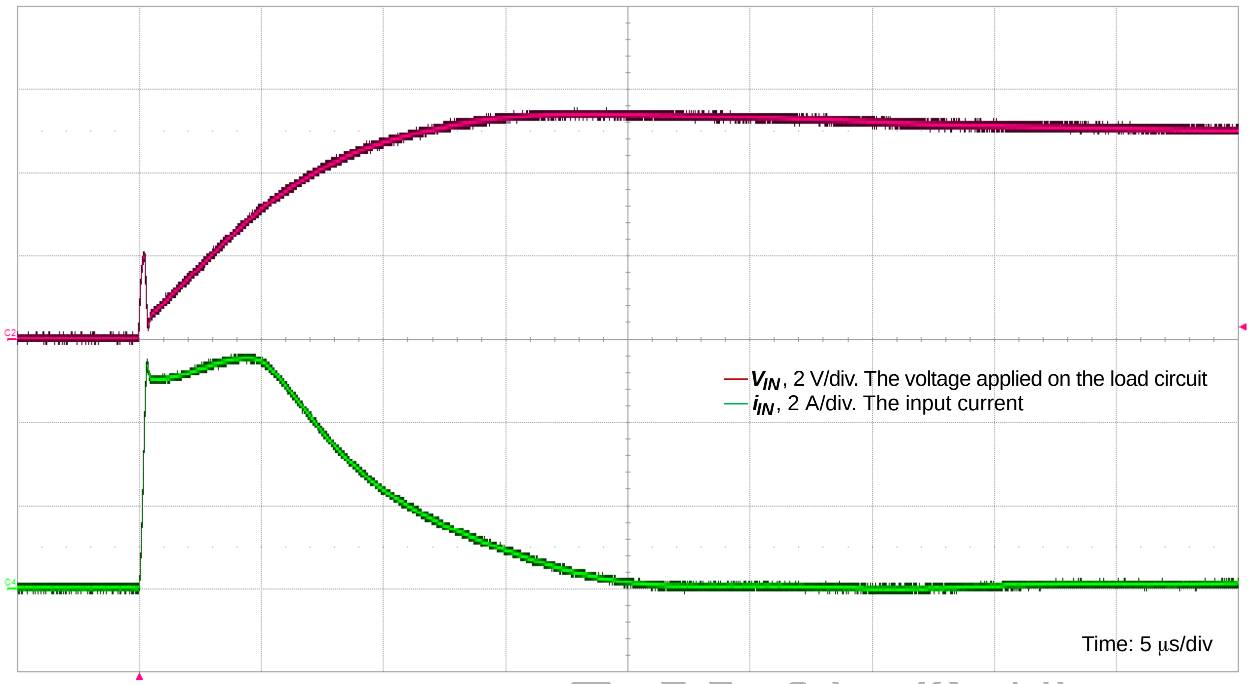


Figure 19. Startup Waveform without FR014H5JZ, DC Power Source = 5 V, C_1 = 100 μF, C_2 = 10 μF, $R_1 = R_2$ = 10 kΩ, R_3 = 27 Ω

APPLICATION INFORMATION

Figure 17 shows the voltage and current waveforms when a virtual USB3.0 device is connected to a 5 V source. A USB application allows a maximum source output capacitance of C_1 = 120 μF and a maximum device−side input capacitance of C_2 = 10 μF plus a maximum load (minimum resistance) of R_3 = 27 Ω. C_1 = 100 μF, C_2 = 10 μF and R_3 = 27 Ω were used for testing.

When the DC power source is connected to the circuit *(refer to Figure 13)*, the built−in startup diode initially conducts the current such that the USB device powers up. Due to the initial diode voltage drop, the FR014H5JZ effectively reduces the peak inrush current of a hot plug event. Under these test conditions, the input inrush current reaches about 6 A peak. While the current flows, the input voltage increases. The speed of this input voltage increase depends on the time constant formed by the load resistance R_3 and load capacitance C_2. The larger the time constant, the slower the input voltage increase. As the input voltage approaches a level equal to the protector’s turn−on voltage, V_{ON}, the protector turns on and operates in Low−Resistance Mode as defined by V_{IN} and operating current I_{IN}.

In the event of a negative transient, or when the DC power source is reversely connected to the circuit, the device blocks the flow of current and holds off the voltage, thereby protecting the USB device. Figure 18 shows the voltage and current waveforms when a virtual USB3.0 device is reversely biased; the output voltage is near 0 and response time is less than 50 ns.

Figure 19 shows the voltage and current waveforms when no reverse bias protection is implemented. In Figure 17, while the reverse bias protector is present, the input voltage, V_{IN}, and the output voltage, V_O, are separated and look different. When this reverse bias protector is removed, V_{IN} and V_O merge, as shown in Figure 19 as V_{IN}. This V_{IN} is also the voltage applied to the load circuit. It can be seen that, with reverse bias protection, the voltage applied to the load and the current flowing into the load look very much the same as without reverse bias protection.

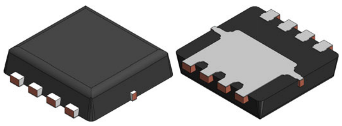
Benefits of Reverse Bias Protection

The most important benefit is to prevent accidently reverse−biased voltage from damaging the USB load. Another benefit is that the peak startup inrush current can be reduced. How fast the input voltage rises, the input/output capacitance, the input voltage, and how heavy the load is determine how much the inrush current can be reduced. In a 5 V USB application, for example, the inrush current can be 5% − 20% less with different input voltage rising rate and other factors. This can offer a system designer the option of increasing C_2 while keeping “effective” USB device capacitance down.

ORDERING INFORMATION

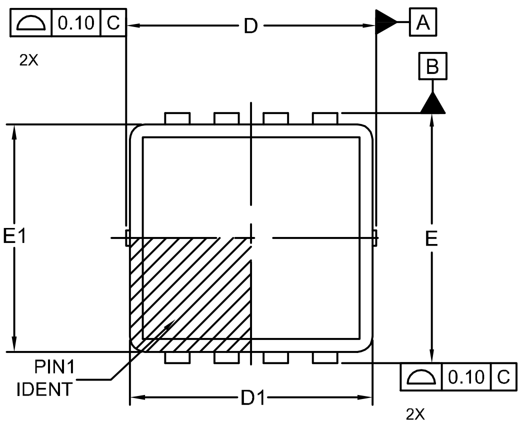
Part Number	Top Mark	Package	Reel	Tape	Shipping†
FR014H5JZ	14H	8−Lead, Molded Leadless Package (MLP), Dual, 3.3 mm Square (Pb−Free. Halide Free)	13−inch	12 mm	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



WDFN8 3.3x3.3, 0.65P
CASE 511DR
ISSUE B

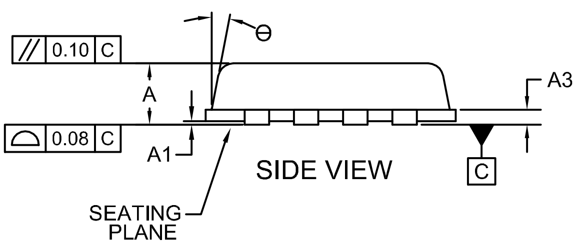
DATE 02 FEB 2022



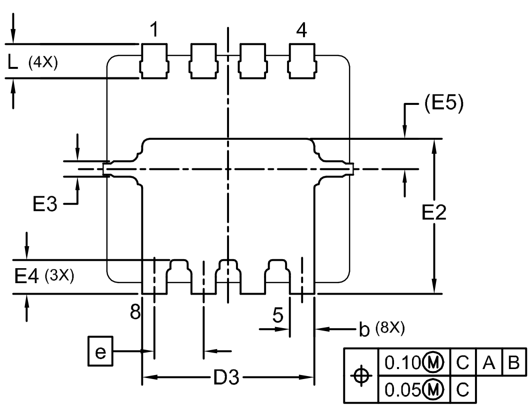
TOP VIEW

NOTES:
A. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
B. SEATING PLANE IS DEFINED BY TERMINAL TIPS ONLY
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATE BURRS. MOLD FLASH PROTRUSION OR GATE BURR DOES NOT EXCEED 0.150MM.

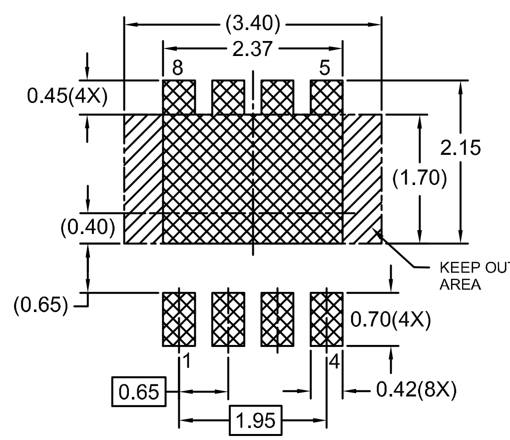
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.15	0.20	0.25
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D1	3.10	3.20	3.30
D3	2.17	2.27	2.37
E	3.20	3.30	3.40
E1	2.90	3.00	3.10
E2	1.95	2.05	2.15
E3	0.15	0.20	0.25
E4	0.30	0.40	0.50
E5	0.40 REF		
e	0.65 BSC		
L	0.30	0.40	0.50
ϴ	0°	-	12°



SIDE VIEW



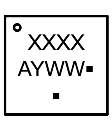
BOTTOM VIEW



RECOMMENDED LAND PATTERN

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**WDFN8 3.3x3.3, 0.65P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

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onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

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