# FQU3N60CTU

# N-Channel QFET® MOSFET

## 600 V, 2.4 A, 3.4 Ω

This N−Channel enhancement mode power MOSFET is produced using ON Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on−state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

### Features

- 2.4 A, 600 V, $R_{DS(on)}$ = 3.4 Ω (Max.) @ $V_{GS}$ = 10 V, $I_D$ = 1.2 A
- Low Gate Charge (Typ. 10.5 nC)
- Low $C_{rss}$ (Typ. 5 pF)
- 100% Avalanche Tested
- These Devices are Pb−Free and are RoHS Compliant

### Applications

- LCD / LED TV
- Lighting
- Charger / Adapter

**ON Semiconductor®**

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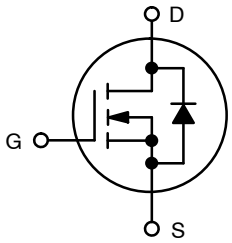


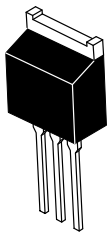

**IPAK3**
**CASE 369AR**

### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 2 of this data sheet.

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{DSS}$ | Drain−to−Source Voltage | | 600 | V |
| $V_{GSS}$ | Gate−to−Source Voltage | | ±30 | V |
| $I_D$ | Drain Current | Continuous ($T_C$ = 25°C) | 2.4 | A |
| | | Continuous ($T_C$ = 100°C) | 1.5 | |
| $I_{DM}$ | Drain Current | Pulsed (Note 1) | 9.6 | A |
| $E_{AS}$ | Single Pulse Avalanche Energy (Note 2) | | 150 | mJ |
| $I_{AR}$ | Avalanche Current (Note 1) | | 2.4 | A |
| $E_{AR}$ | Repetitive Avalanche Energy (Note 1) | | 4.0 | mJ |
| dv/dt | Peak Diode Recovery (Note 3) | | 4.5 | V/ns |
| $P_D$ | Power Dissipation | $T_C$ = 25°C | 50 | W |
| | | Derate Above 25°C | 0.4 | W/°C |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature Range | | −55 to +150 | °C |
| $T_L$ | Maximum Lead Temperature for Soldering Purposes (1/8″ from case for 5 seconds) | | 300 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $I_{AS}$ = 2.4 A, $V_{DD}$ = 50 V, L = 47 mH, $R_G$ = 25 Ω, starting $T_J$ = 25°C.
3. $I_{SD}$ ≤ 3 A, di/dt ≤ 200 A/μs, $V_{DD}$ ≤ $BV_{DSS}$, Starting $T_J$ = 25°C.

**THERMAL CHARACTERISTICS**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction−to−Case, Max. | 2.5 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction−to−Ambient, Max. | 110 | |

**PACKAGE MARKING AND ORDERING INFORMATION**

| Part Number | Top Mark | Package | Packing Method | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|---|
| FQU3N60CTU | FQU3N60C | IPAK | Tube | N/A | N/A | 75 units |

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise specified)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain−to−Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V | 600 | – | – | V |
| $\Delta BV_{DSS}/\Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to 25°C | – | 0.6 | – | V/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 600 V, $V_{GS}$ = 0 V | – | – | 1 | μA |
| | | $V_{DS}$ = 480 V, $T_C$ = 125°C | – | – | 10 | |
| $I_{GSSF}$ | Gate−to−Body Leakage Current | $V_{GS}$ = 30 V, $V_{DS}$ = 0 V | – | – | 100 | nA |
| $I_{GSSR}$ | Gate−to−Body Leakage Current | $V_{GS}$ = −30 V, $V_{DS}$ = 0 V | – | – | −100 | nA |
| **ON CHARACTERISTICS** | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | 2.0 | – | 4.0 | V |
| $R_{DS(on)}$ | Static Drain−to−Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 1.2 A | – | 2.8 | 3.4 | Ω |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 40 V, $I_D$ = 1.2 A | – | 3.5 | – | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 25 V, $V_{GS}$ = 0 V, f = 1 MHz | – | 435 | 565 | pF |
| $C_{oss}$ | Output Capacitance | | – | 45 | 60 | |
| $C_{rss}$ | Reverse Transfer Capacitance | | – | 5 | 8 | |
| **SWITCHING CHARACTERISTICS** | | | | | | |
| $t_{d(on)}$ | Turn−On Delay Time | $V_{DD}$ = 300 V, $I_D$ = 3 A, $R_G$ = 25 Ω (Note 4) | – | 12 | 34 | ns |
| $t_r$ | Turn−On Rise Time | | – | 30 | 70 | |
| $t_{d(off)}$ | Turn−Off Delay Time | | – | 35 | 80 | |
| $t_f$ | Turn−Off Fall Time | | – | 35 | 80 | |
| $Q_g$ | Total Gate Charge at 10 V | $V_{DS}$ = 480 V, $I_D$ = 3 A, $V_{GS}$ = 10 V (Note 4) | – | 10.5 | 14 | nC |
| $Q_{gs}$ | Gate−to−Source Gate Charge | | – | 2.1 | – | |
| $Q_{gd}$ | Gate−to−Drain “Miller” Charge | | – | 4.5 | – | |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | |
| $I_S$ | Maximum Continuous Drain to Source Diode Forward Current | | – | – | 3 | A |
| $I_{SM}$ | Maximum Pulsed Drain to Source Diode Forward Current | | – | – | 12 | |
| $V_{SD}$ | Drain to Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 2.4 A | – | – | 1.4 | V |
| $t_{rr}$ | Reverse Recovery Time | $V_{GS}$ = 0 V, $I_S$ = 3 A, $dI_F/dt$ = 100 A/μs | – | 260 | – | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | – | 1.6 | – | μC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature.

## TYPICAL CHARACTERISTICS

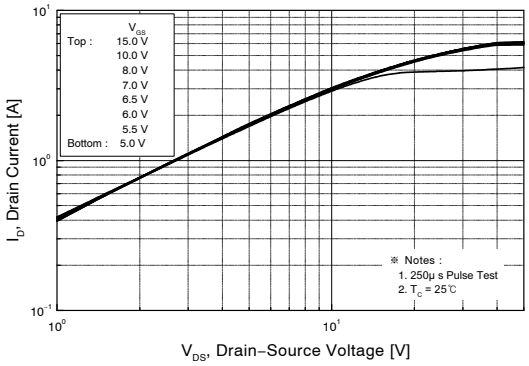


**Figure 1. On−Region Characteristics**

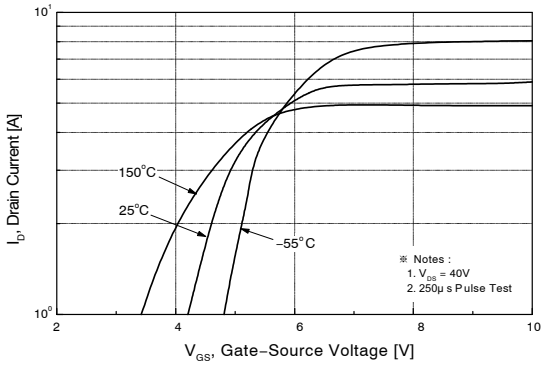


**Figure 2. Transfer Characteristics**

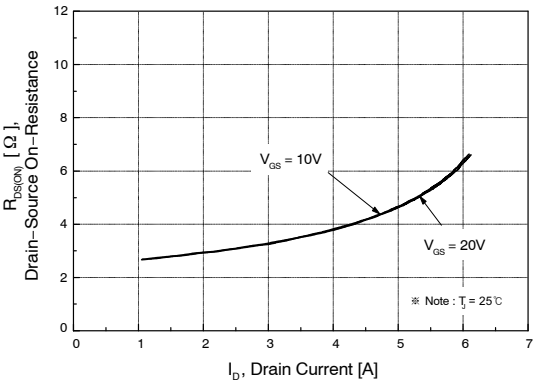


**Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage**

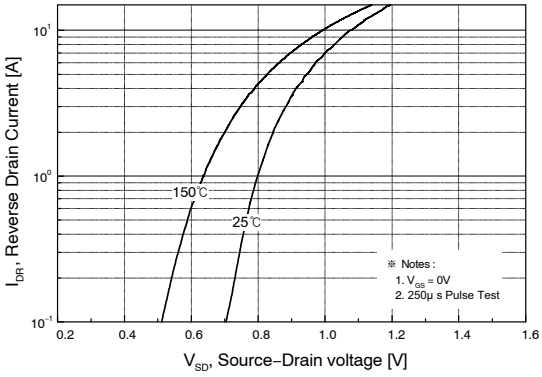


**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**

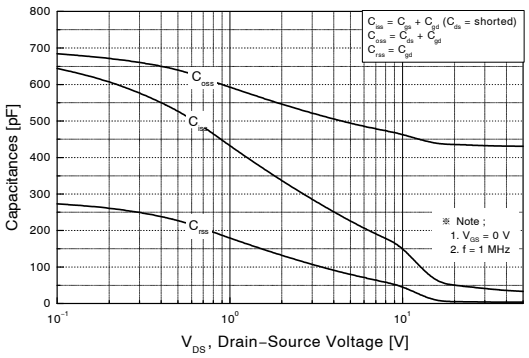


**Figure 5. Capacitance Characteristics**

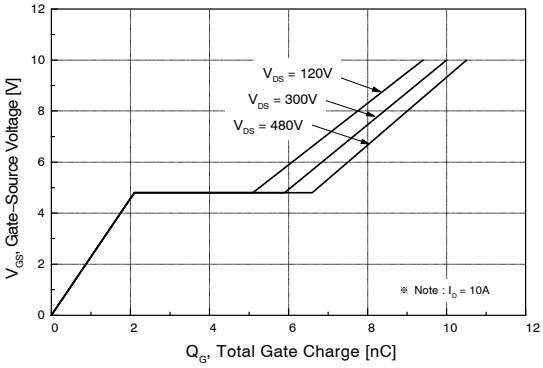


**Figure 6. Gate Charge Characteristics**

## TYPICAL CHARACTERISTICS

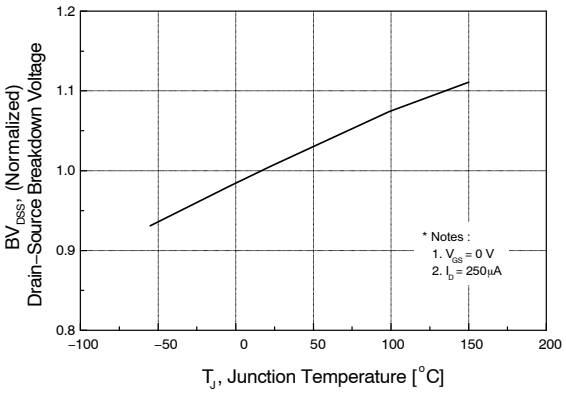


**Figure 7. Breakdown Voltage Variation vs. Temperature**

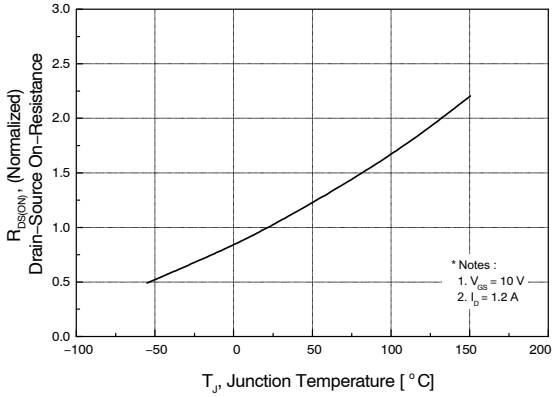


**Figure 8. On−Resistance Variation vs. Temperature**

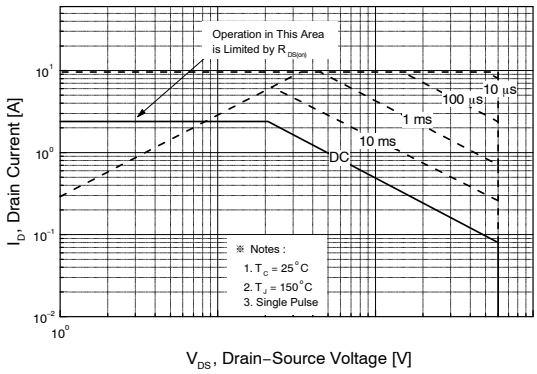


**Figure 9. Maximum Safe Operating Area**

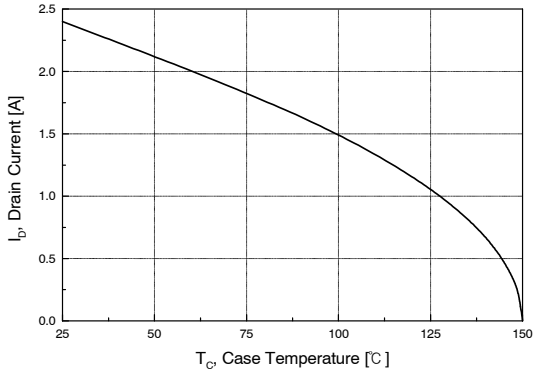


**Figure 10. Maximum Drain Current vs. Case Temperature**

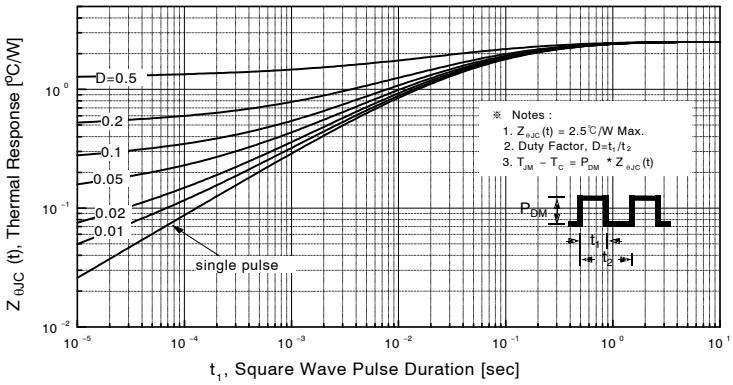


**Figure 11. Transient Thermal Response Curve**

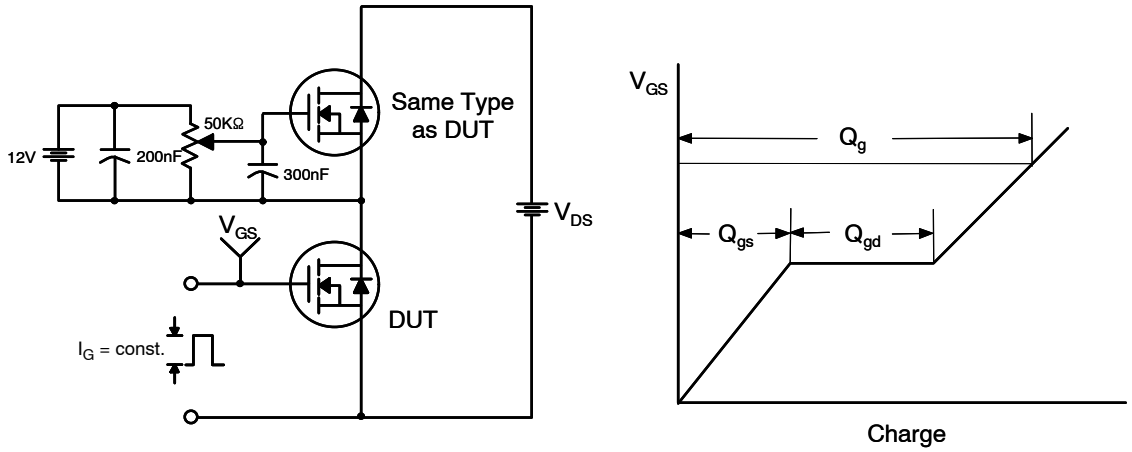


**Figure 12. Gate Charge Test Circuit & Waveform**

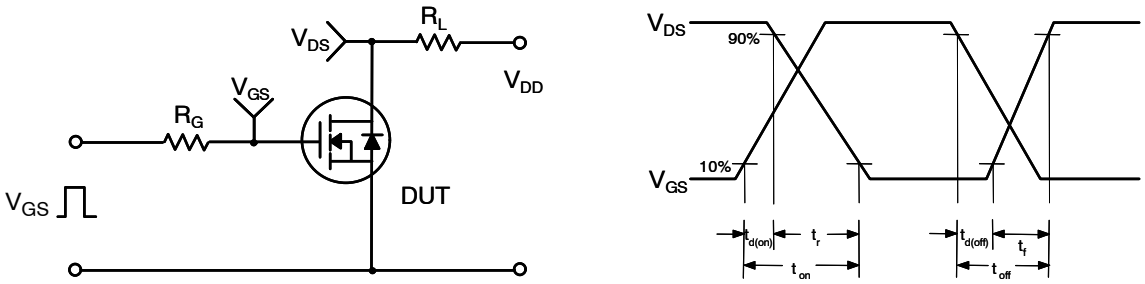


**Figure 13. Resistive Switching Test Circuit & Waveforms**

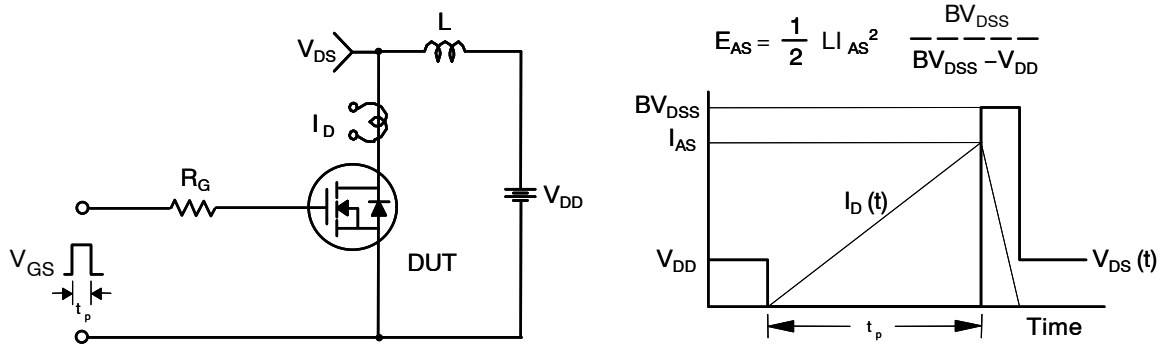


**Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms**

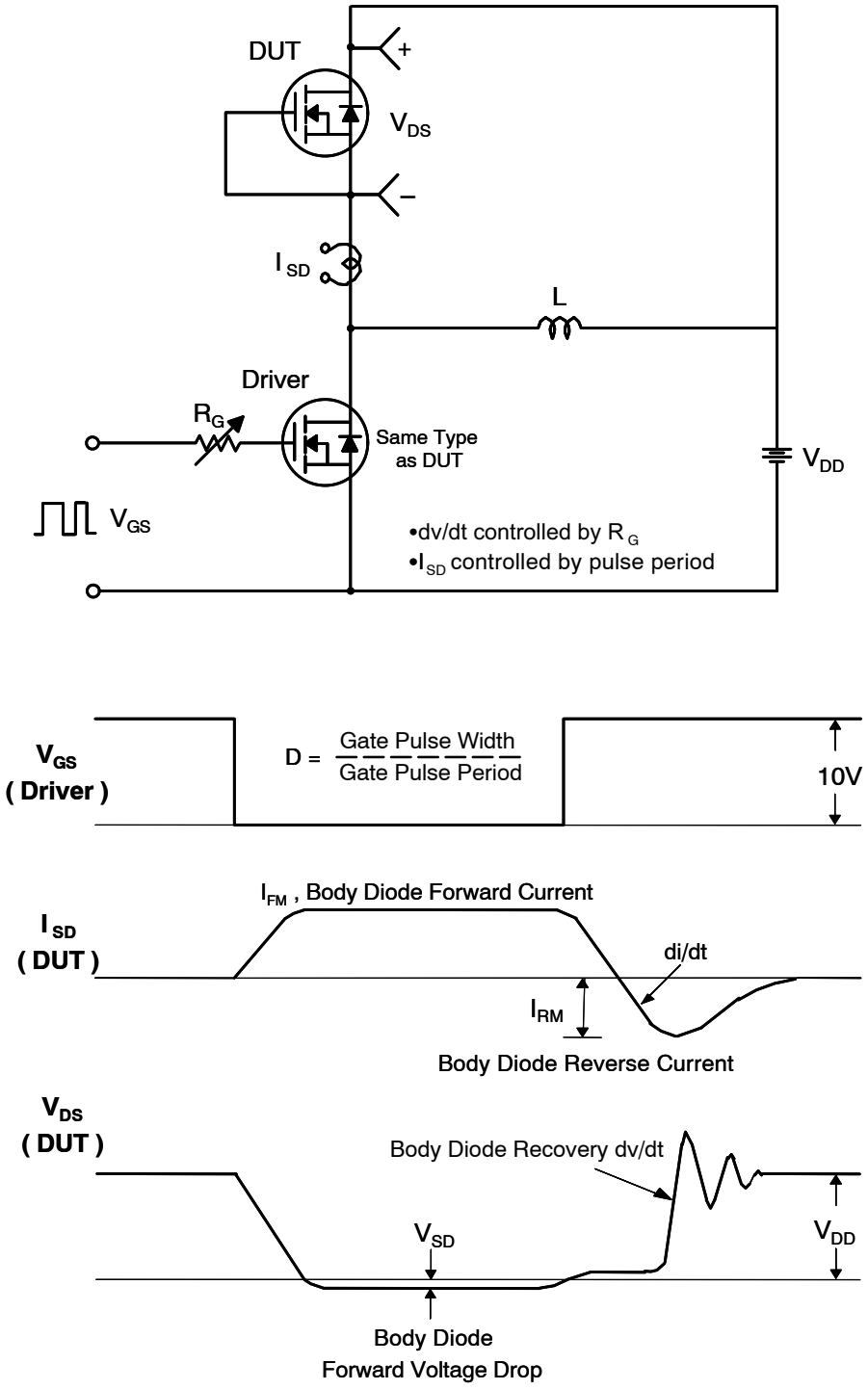


**Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms**

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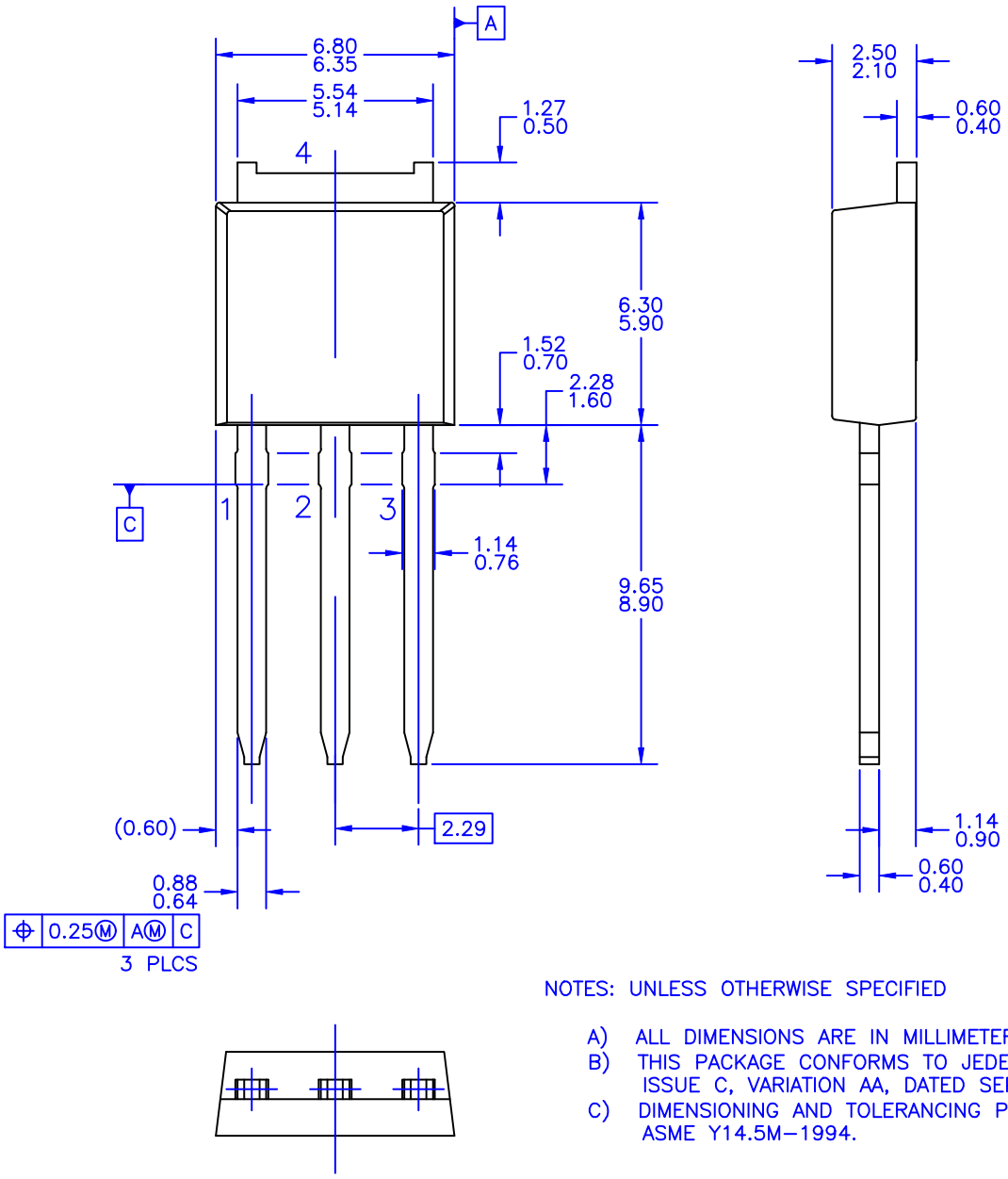




NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.
B) THIS PACKAGE CONFORMS TO JEDEC, TO−251, ISSUE C, VARIATION AA, DATED SEP 1988.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.

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