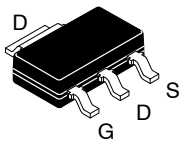
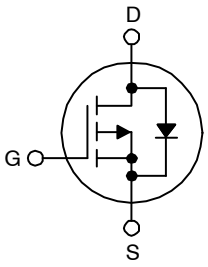
MOSFET – P-Channel QFET®

-200 V, -0.67 A, 2.7 Ω

FQT3P20



SOT−223
CASE 318H−01



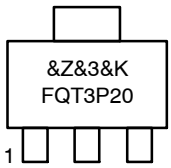
Description

This P-Channel enhancement mode power MOSFET is produced using **onsemi**'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

- −0.67 A, −200 V, $R_{DS(on)}$ = 2.7 Ω (Max) @ V_{GS} = 10 V, I_D = 0.335 A
- Low Gate Charge (Typ. 6.0 nC)
- Low Crss (Typ. 7.5 pF)
- This is a Pb-Free Device

MARKING DIAGRAM



&Z	= Assembly Plant Code
&3	= Date Code
&K	= Lot Run Traceability Code
FQT3P20	= Specific Device Code

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain−Source Voltage	−200	V
I_D	Drain Current Continuous (T_C = 25°C) Continuous (T_C = 70°C)	 −0.67 −0.53	A
I_{DM}	Drain Current − Pulsed (Note 1)	−2.7	A
V_{GSS}	Gate−Source Voltage	±30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	150	mJ
I_{AR}	Avalanche Current (Note 1)	−0.67	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	0.25	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	−5.5	V/ns
P_D	Power Dissipation (T_C = 25°C) Derate above 25°C	 2.5 0.02	 W W/°C
T_J, T_{STG}	Operating and Storage Temperature Range	−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 5 Seconds	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. L = 500 mH, I_{AS} = −0.67 A, V_{DD} = −50 V, R_G = 25 Ω, Starting T_J = 25°C.
3. I_{SD} ≤ −2.8 A, di/dt ≤ 300 A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient	50	°C/W

ORDERING INFORMATION

Device	Package	Shipping†
FQT3P20TF	SOT−223 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTIC						
BV_{DSS}	Drain−Source Breakdown Voltage	V_{GS} = 0 V, I_D = −250 μA	−200	–	–	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = −250 μA, Referenced to 25°C	–	−0.18	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = −200 V, V_{GS} = 0 V	–	–	−1	μA
		V_{DS} = −160 V, T_C = 125°C	–	–	−10	
I_{GSSF}	Gate−Body Leakage Current, Forward	V_{GS} = −30 V, V_{DS} = 0 V	–	–	−100	nA
I_{GSSR}	Gate−Body Leakage Current, Reverse	V_{GS} = 30 V, V_{DS} = 0 V	–	–	100	
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = −250 μA	−3.0	–	−5.0	V
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = −10 V, I_D = −0.335 A	–	2.06	2.7	Ω
g_{FS}	Forward Transconductance	V_{DS} = −40 V, I_D = −0.335 A	–	0.7	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = −25 V, V_{GS} = 0 V, f = 1.0 MHz	–	190	250	pF
C_{oss}	Output Capacitance		–	45	60	pF
C_{rss}	Reverse Transfer Capacitance		–	7.5	10	pF
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = −100 V, I_D = −2.8 A, R_G = 25 Ω (Note 4)	–	8.5	25	ns
t_r	Turn−On Rise Time		–	35	80	ns
$t_{d(off)}$	Turn−Off Delay Time		–	12	35	ns
t_f	Turn−Off Fall Time		–	25	60	ns
Q_g	Total Gate Charge	V_{DS} = −160 V, I_D = −2.8 A, V_{GS} = −10 V (Note 4)	–	6.0	8.0	nC
Q_{gs}	Gate−Source Charge		–	1.7	–	nC
Q_{gd}	Gate−Drain Charge		–	2.9	–	nC
DRAIN−SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain−Source Diode Forward Current		–	–	−0.67	A
I_{SM}	Maximum Pulsed Drain−Source Diode Forward Current		–	–	−2.7	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_S = −0.67 A	–	–	−5.0	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = −2.8 A, dI_F/dt = 100 A/μs	–	100	–	ns
Q_{rr}	Reverse Recovery Charge		–	0.34	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

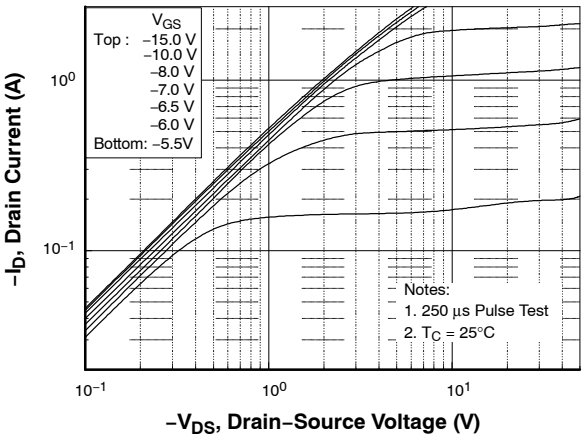


Figure 1. On−Region Characteristics

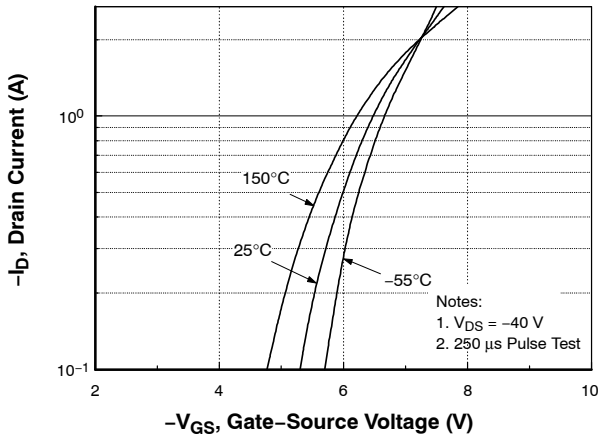


Figure 2. Transfer Characteristics

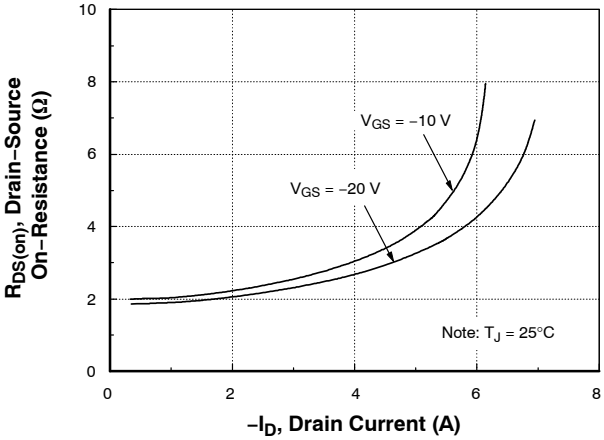


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

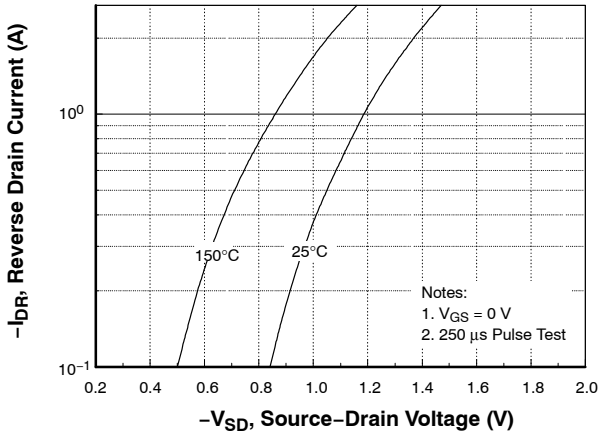


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

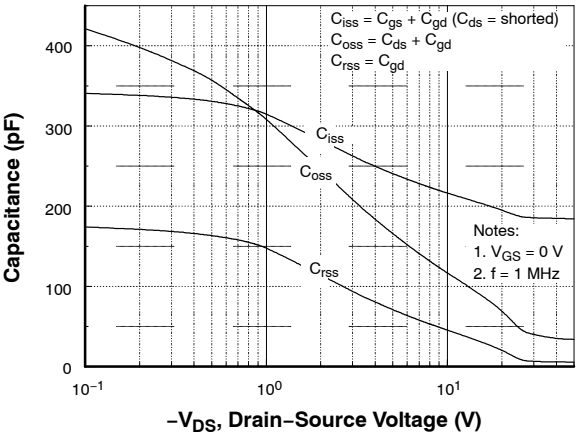


Figure 5. Capacitance Characteristics

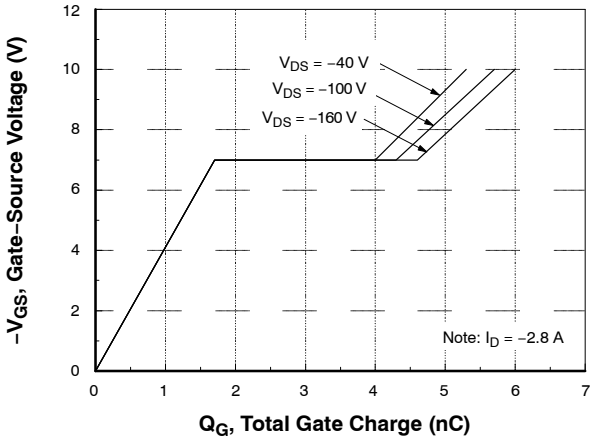


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (Continued)

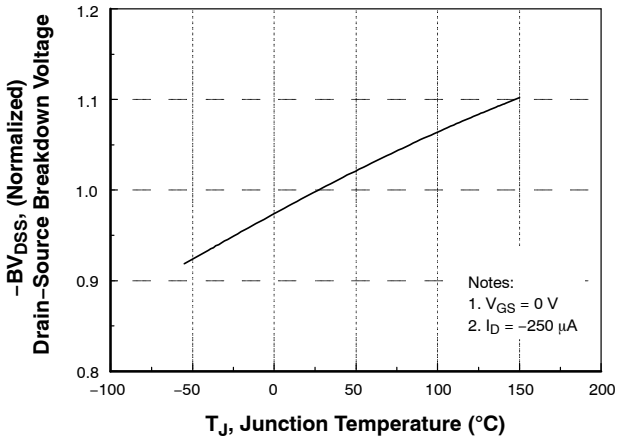


Figure 7. Breakdown Voltage Variation vs. Temperature

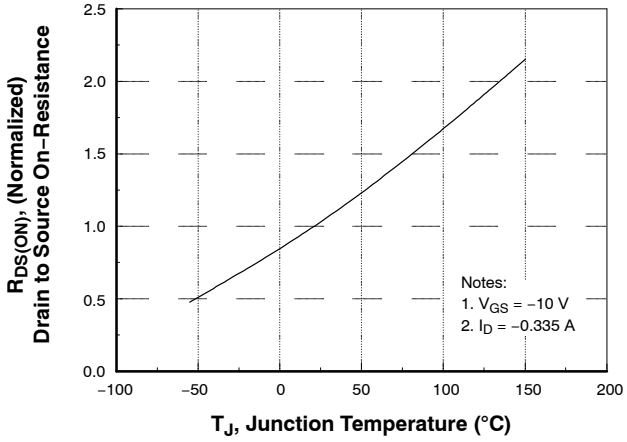


Figure 8. On−Resistance Variation vs. Temperature

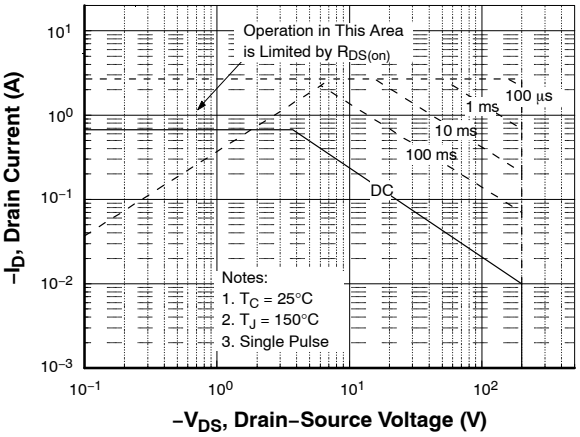


Figure 9. Maximum Safe Operating Area

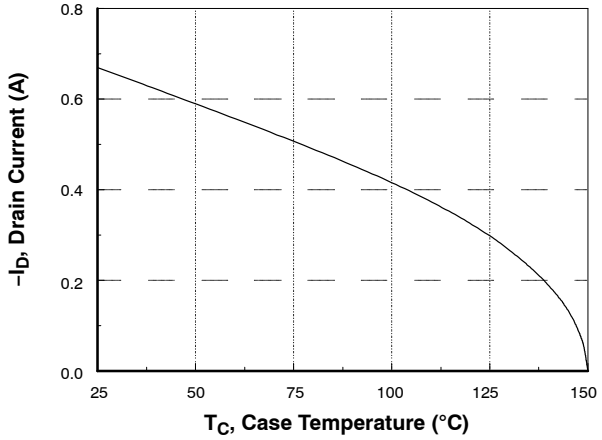


Figure 10. Maximum Drain Current vs. Case Temperature

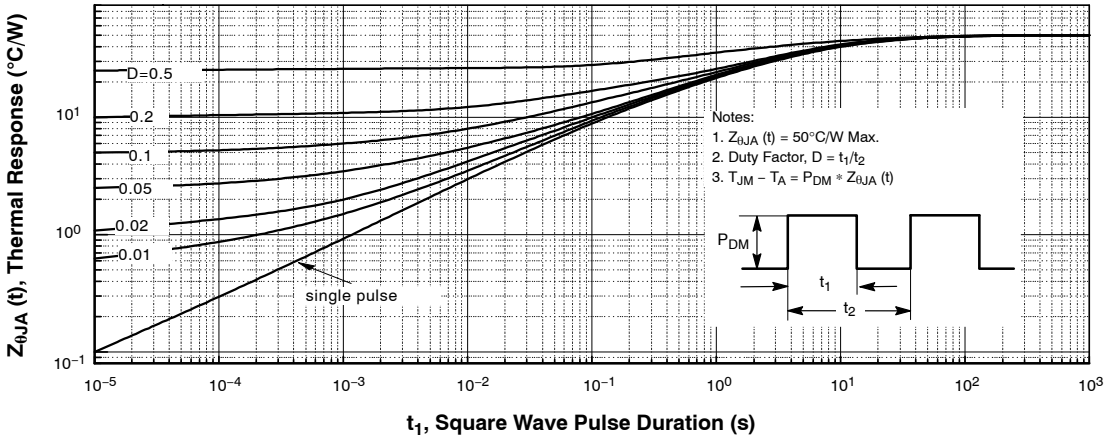


Figure 11. Transient Thermal Response Curve

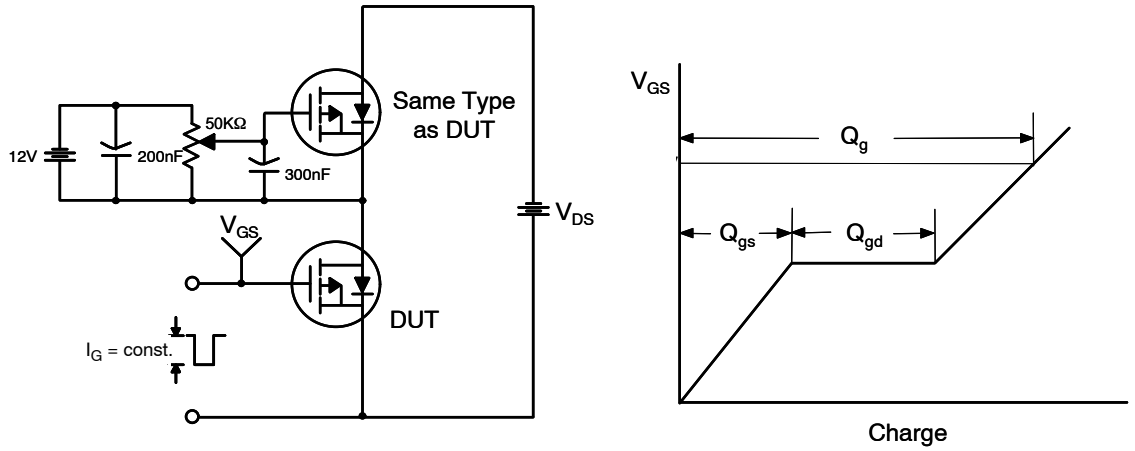


Figure 12. Gate Charge Test Circuit & Waveform

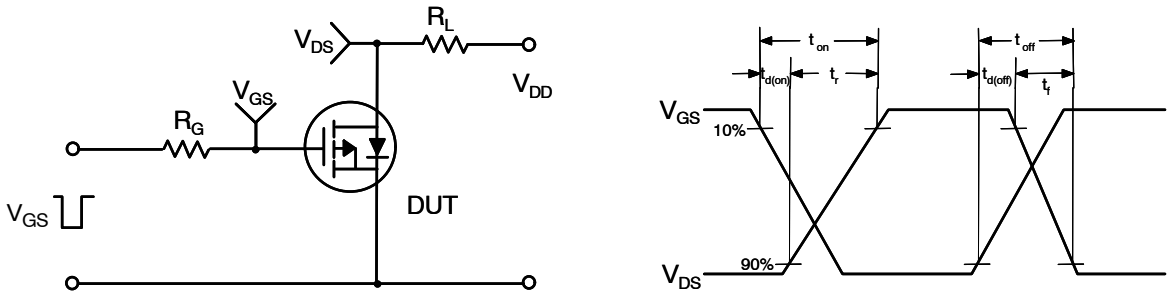


Figure 13. Resistive Switching Test Circuit & Waveforms

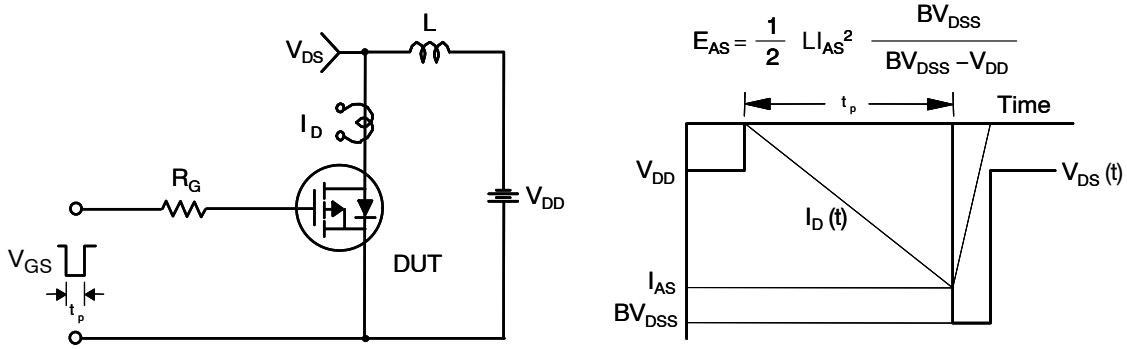


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

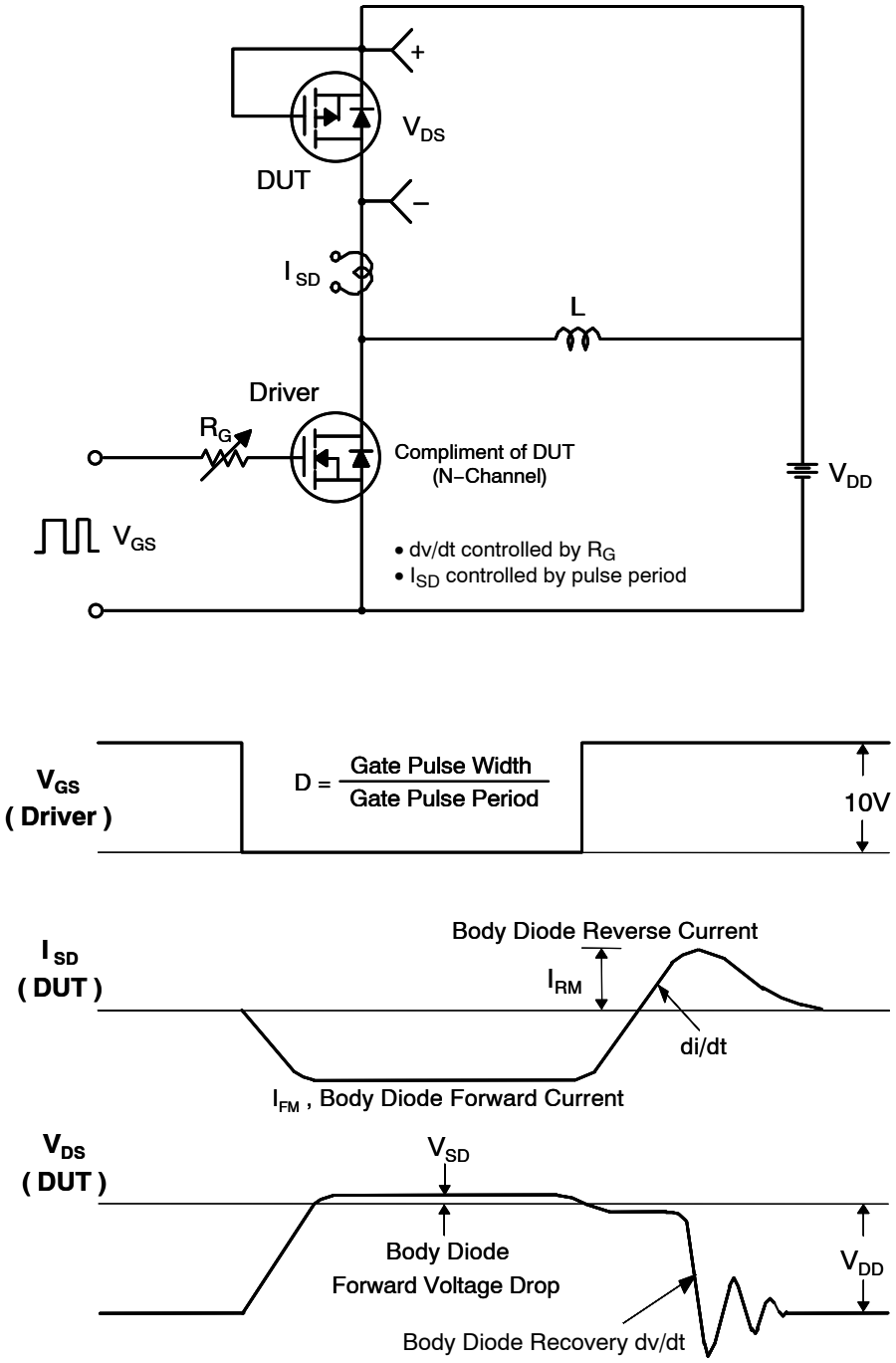


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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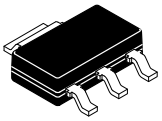
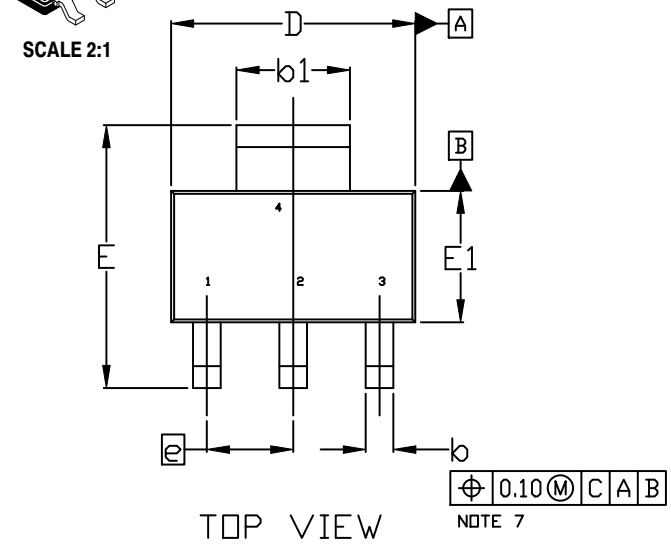
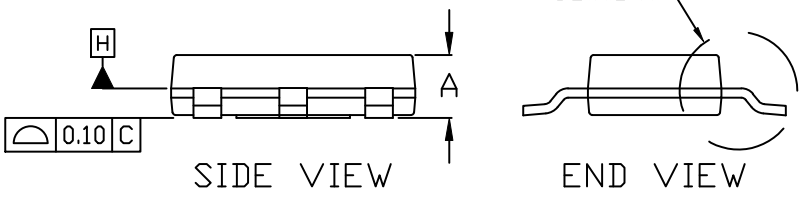
ISSUE B

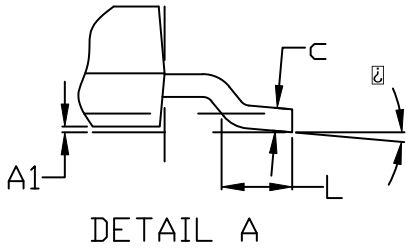
DATE 13 MAY 2020



SCALE 2:1

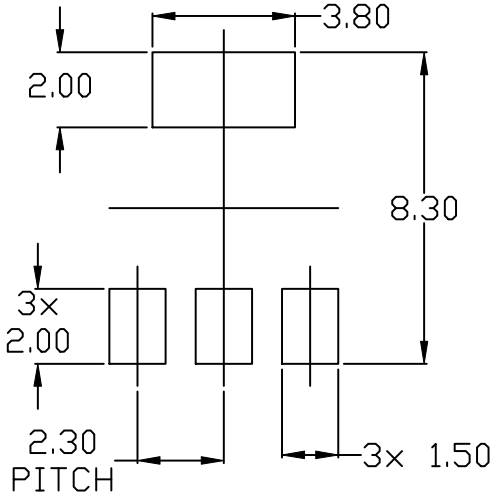






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E1 ARE DETERMINED AT DATUM H. DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. SHALL NOT EXCEED 0.23mm PER SIDE.
4. LEAD DIMENSIONS b AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBBAR PROTRUSION IS 0.08mm PER SIDE.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

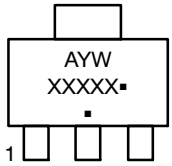
	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	---	---	1.80
A1	0.02	0.06	0.11
b	0.60	0.74	0.88
b1	2.90	3.00	3.10
c	0.24	---	0.35
D	6.30	6.50	6.70
E	6.70	7.00	7.30
E1	3.30	3.50	3.70
e	2.30 BSC		
L	0.25	---	---
θ	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**SOT−223**	**PAGE 1 OF 1**

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