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FAIRCHILD SEMICONDUCTOR®

August 2024

FQS4901

N-Channel QFET® MOSFET

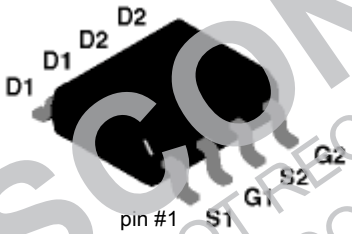
400 V, 0.45 A, 4.2 Ω

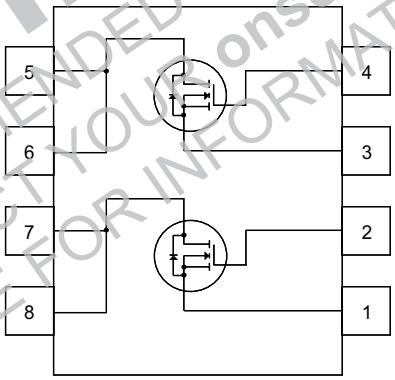
Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor®'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 0.45 A, 400 V, $R_{DS(on)}$=4.2 Ω(Max.)@V_{GS}=10 V, I_D=0.225 A
- Low Gate Charge (Typ. 5.8 nC)
- Low C_{rss} (Typ. 5 pF)
- 100% Avalanche Tested





Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

Symbol	Parameter		FQS4901	Unit
V_{DSS}	Drain-Source Voltage		400	V
I_D	Drain Current - Continuous (T_A = 25°C)		0.45	A
	- Continuous (T_A = 70°C)		0.285	A
I_{DM}	Drain Curent - Pulsed	(Note 1)	1.8	A
V_{GSS}	Gate-Source Voltage		± 25	V
dv/dt	Peak Diode Recovery dv/dt	(Note 2)	4.5	V/ns
P_D	Power Dissipation (T_A = 25°C)		2.0	W
	(T_A = 70°C)		1.3	W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	°C/W

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	400	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C	--	0.42	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 400 V, V_{GS} = 0 V	--	--	1	µA
		V_{DS} = 320 V, T_C = 125°C	--	--	10	µA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 25 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -25 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 0.225 A	--	3.2	4.2	Ω
g_{FS}	Forward Transconductance	V_{DS} = 35 V, I_D = 0.225 A (Note 3)	--	0.283	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	160	210	pF
C_{oss}	Output Capacitance		--	30	40	pF
C_{rss}	Reverse Transfer Capacitance		--	5	6.5	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 200 V, I_D = 0.45 A, R_G = 25 Ω (Note 3,4)	--	5	20	ns
t_r	Turn-On Rise Time		--	20	50	ns
$t_{d(off)}$	Turn-Off Delay Time		--	20	50	ns
t_f	Turn-Off Fall Time		--	35	80	ns
Q_g	Total Gate Charge	V_{DS} = 320 V, I_D = 0.45 A, V_{GS} = 10 V (Note 3,4)	--	5.8	7.5	nC
Q_{gs}	Gate-Source Charge		--	0.53	--	nC
Q_{gd}	Gate-Drain Charge		--	3.22	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	0.45	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	1.8	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.45 A	--	--	1.5	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 0.45 A, dI_F / dt = 100 A/µs (Note 3)	--	86	--	ns
Q_{rr}	Reverse Recovery Charge		--	0.15	--	µC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $I_{SD} \leq$ 0.45A, di/dt $\leq$ 200A/µs, $V_{DD} \leq BV_{DSS}$, Starting T_J = 25°C
3. Pulse Test : Pulse width $\leq$ 300µs, Duty cycle $\leq$ 2%
4. Essentially independent of operating temperature

Typical Characteristics

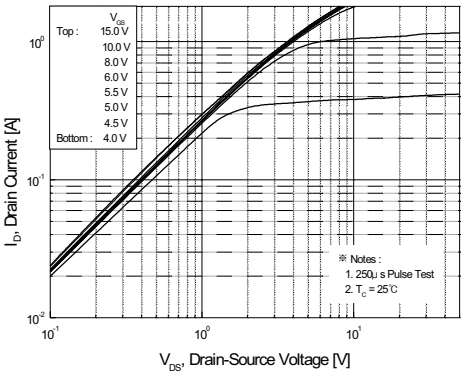


Figure 1. On-Region Characteristics

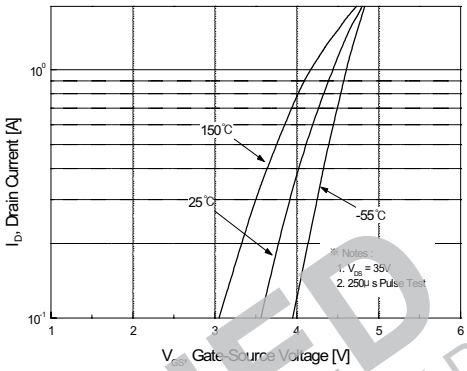


Figure 2. Transfer Characteristics

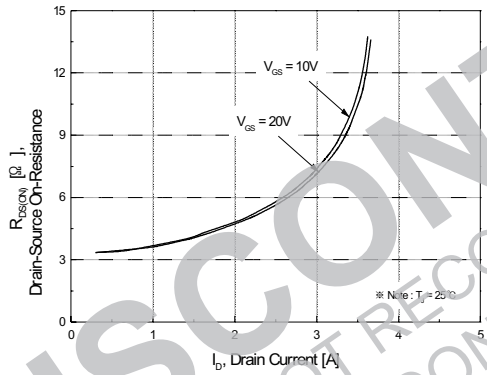


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

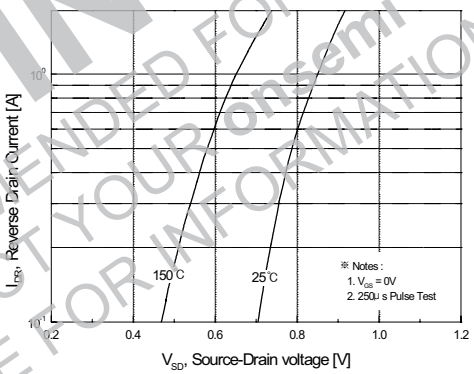


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

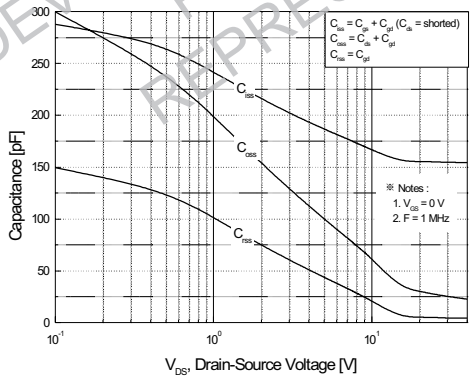


Figure 5. Capacitance Characteristics

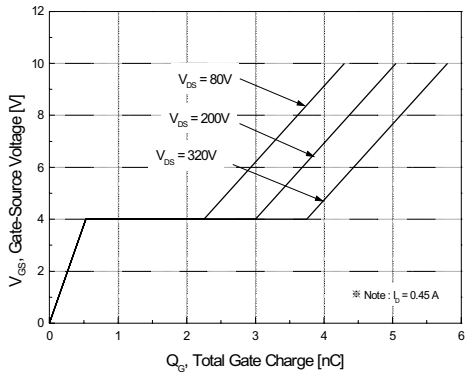


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

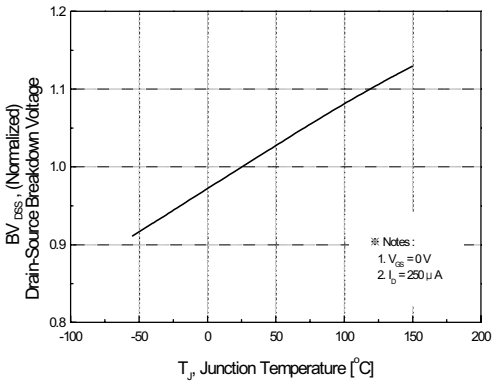


Figure 7. Breakdown Voltage Variation vs. Temperature

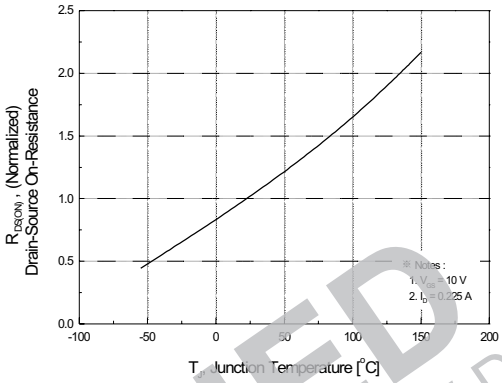


Figure 8. On-Resistance Variation vs. Temperature

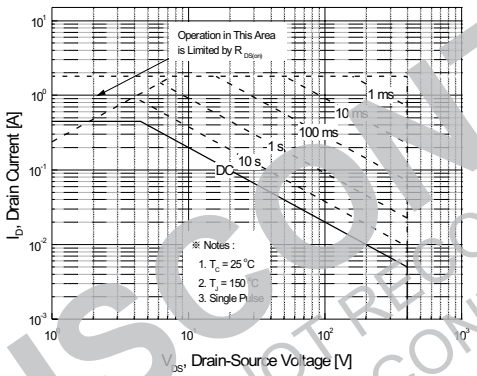


Figure 9. Maximum Safe Operating Area

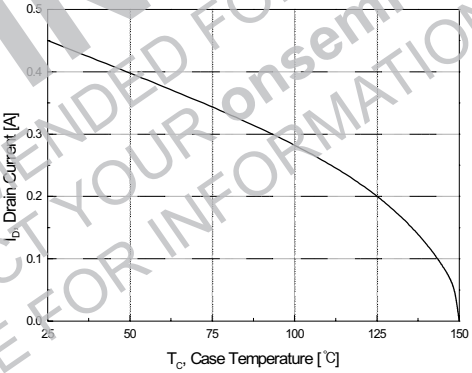


Figure 10. Maximum Drain Current vs. Case Temperature

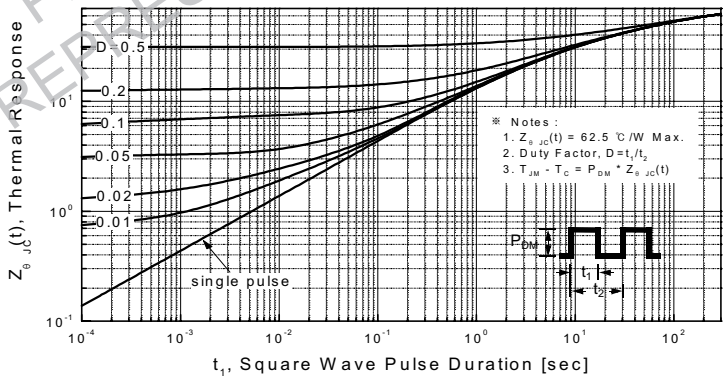
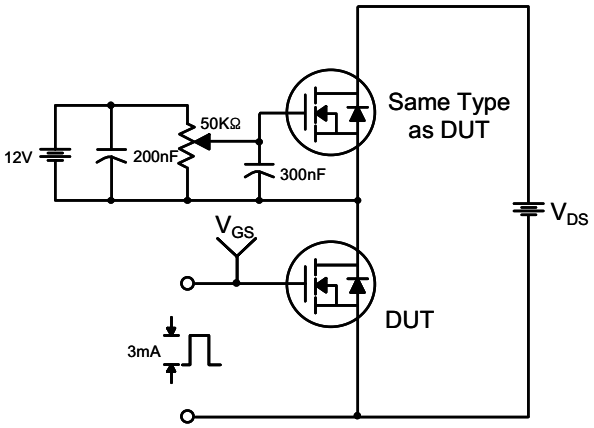
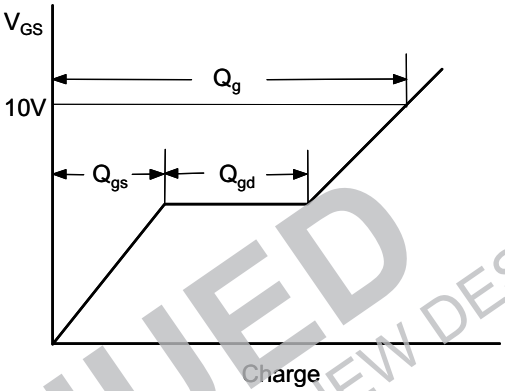


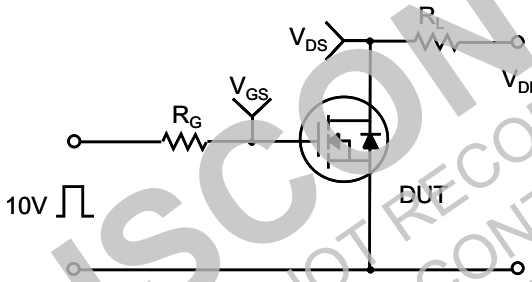
Figure 11. Transient Thermal Response Curve

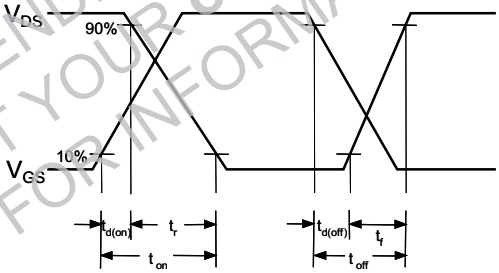
Gate Charge Test Circuit & Waveform



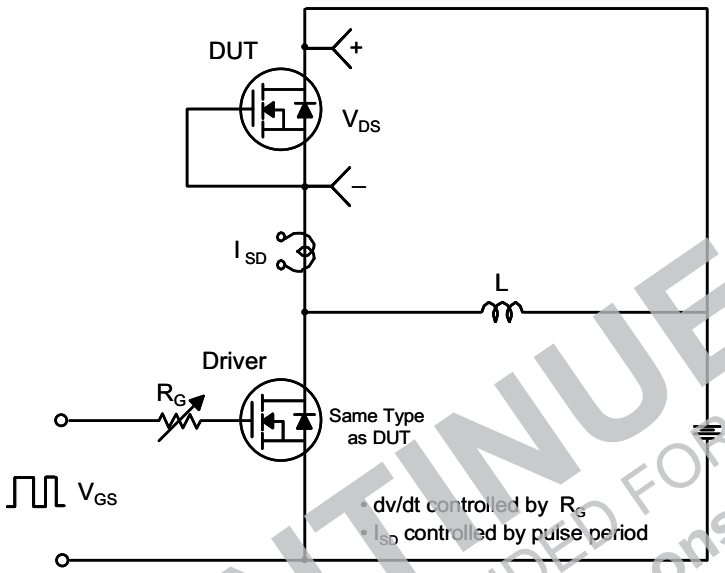


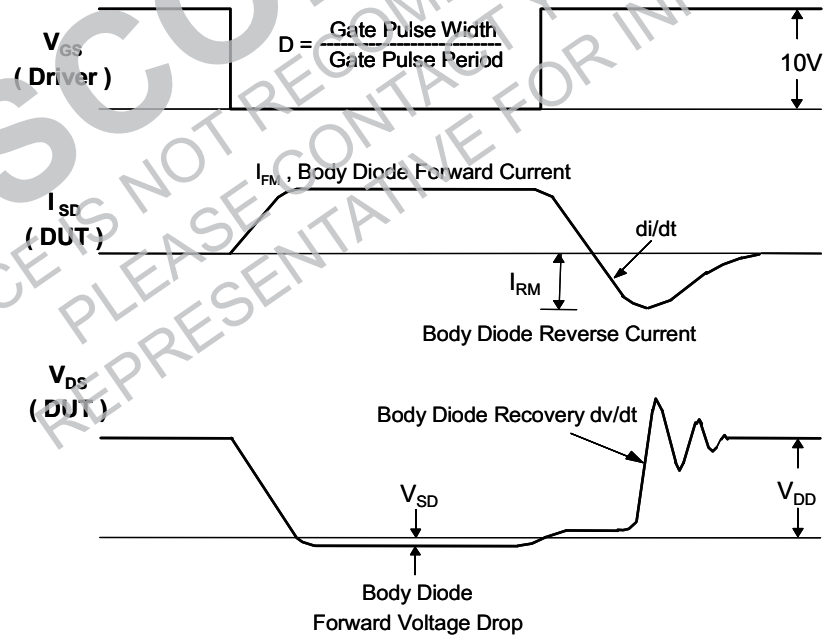
Resistive Switching Test Circuit & Waveforms





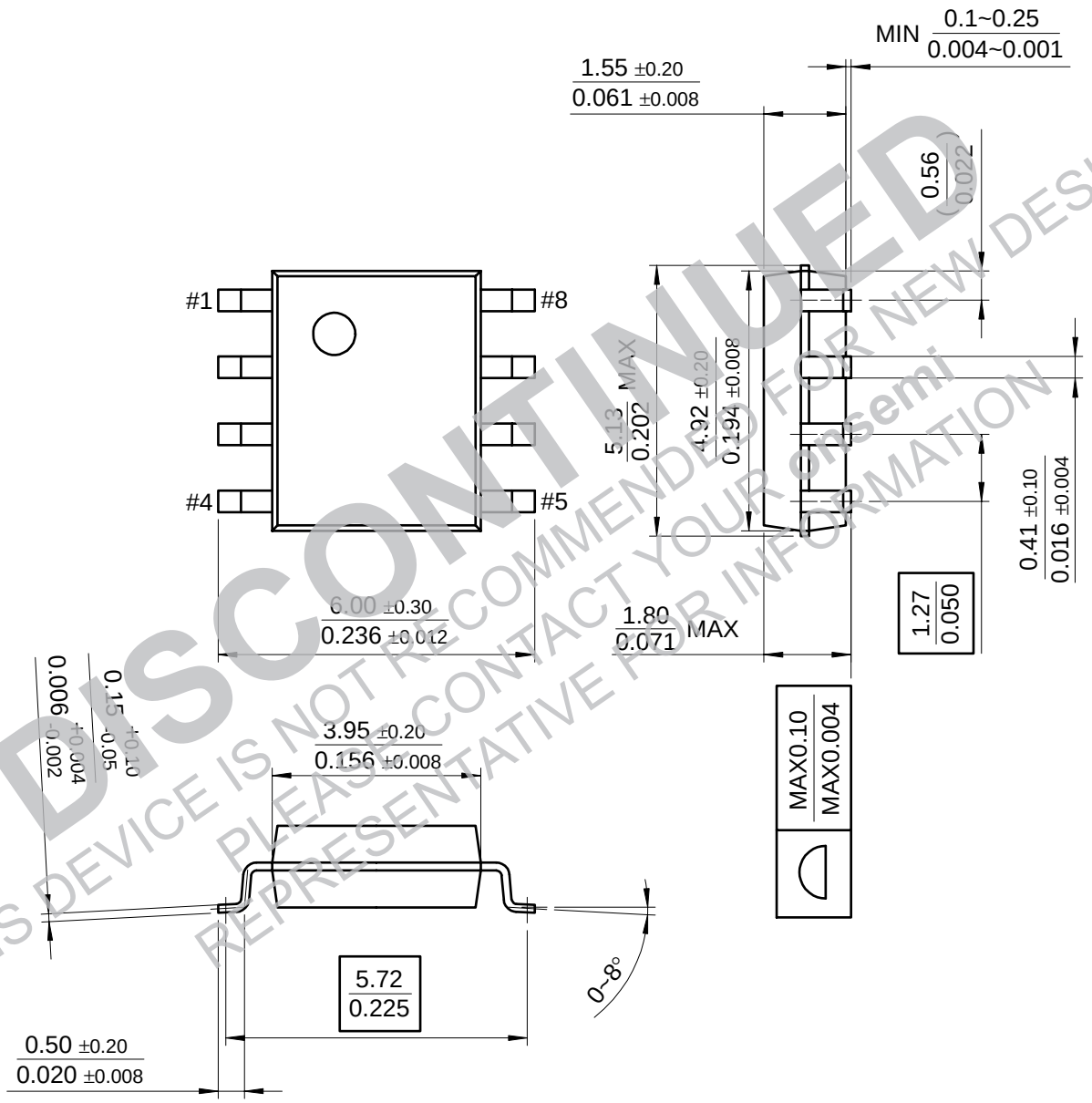
Peak Diode Recovery dv/dt Test Circuit & Waveforms





Package Dimensions

8SOP



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