

# MOSFET – P-Channel, QFET® -100 V, -16.5 A, 190 mΩ

## FQP17P10

This P-Channel enhancement mode power MOSFET is produced using onsemi's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

### Features

- -16.5 A, -100 V,  $R_{DS(on)}$  = 190 mΩ (Max.) at  $V_{GS} = -10$  V,  $I_D = -8.25$  A
- Low Gate Charge (Typ. 30 nC)
- Low  $C_{rss}$  (Typ. 100 pF)
- 100% Avalanche Tested
- 175°C Maximum Junction Temperature Rating
- This is a Pb-Free Device

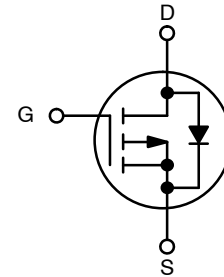
### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter		Ratings	Unit
$V_{DSS}$	Drain-Source Voltage		-100	V
$I_D$	Drain Current	Continuous ( $T_C = 25^\circ\text{C}$ )	-16.5	A
		Continuous ( $T_C = 100^\circ\text{C}$ )	-11.7	
$I_{DM}$	Drain Current	Pulsed (Note 1)	-66	A
$V_{GSS}$	Gate-Source Voltage		$\pm 30$	V
$E_{AS}$	Single Pulse Avalanche Energy (Note 2)		580	mJ
$I_{AR}$	Avalanche Current (Note 1)		-16.5	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)		10	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ (Note 3)		-6.0	V/ns
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	100	W
		Derate above $25^\circ\text{C}$	0.67	
$T_J, T_{STG}$	Operating and Storage Temperature Range		-55 to +175	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	$^\circ\text{C}$

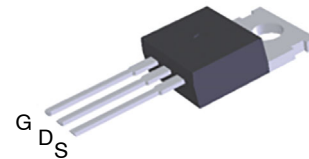
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature
2.  $L = 3.2$  mH,  $I_{AS} = -16.5$  A,  $V_{DD} = -25$  V,  $R_G = 25$  Ω, Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq -16.5$  A,  $di/dt \leq 300$  A/μs,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$

$V_{DS}$	$R_{DS(ON)}$ MAX	$I_D$ MAX
-100 V	0.19 Ω @ -10 V	-16.5 A

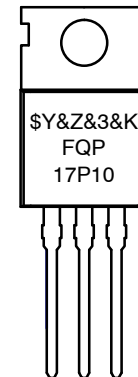


P-Channel MOSFET



TO-220-3LD  
CASE 340AT

### MARKING DIAGRAM



\$Y	= onsemi Logo
&Z	= Assembly Plant Code
&3	= Data Code (Year & Week)
&K	= Lot Code
FQP17P10	= Specific Device Code

### ORDERING INFORMATION

Device	Package	Shipping
FQP17P10	TO-220-3LD (Pb-Free)	50 Units/ Tube

# FQP17P10

## THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Maximum Thermal Resistance, Junction to Case	1.5	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink, Typ.	0.5	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient	62.5	°C/W

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
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### OFF CHARACTERISTICS

$BV_{DSS}$	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-100	–	–	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$	–	-0.1	–	V/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -100\text{ V}, V_{GS} = 0\text{ V}$	–	–	-1	$\mu\text{A}$
		$V_{DS} = -80\text{ V}, T_C = 150^\circ\text{C}$	–	–	-10	
$I_{GSSF}$	Gate –Body Leakage Current, Forward	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	–	–	-100	nA
$I_{GSSR}$	Gate –Body Leakage Current, Reverse	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$			100	nA

### ON CHARACTERISTICS

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-2.0	–	-4.0	V
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = -10\text{ V}, I_D = -8.25\text{ A}$	–	0.14	0.19	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = -40\text{ V}, I_D = -8.25\text{ A}$	–	9.9	–	S

### DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	–	850	1100	pF
$C_{oss}$	Output Capacitance		–	310	400	pF
$C_{rss}$	Reverse Transfer Capacitance		–	100	130	pF

### SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -50\text{ V}, I_D = -16.5\text{ A}, R_G = 25\text{ }\Omega$ (Note 4)	–	17	45	ns
$t_r$	Turn-On Rise Time		–	200	410	ns
$t_{d(off)}$	Turn-Off Delay Time		–	45	100	ns
$t_f$	Turn-Off Fall Time		–	100	210	ns
$Q_g$	Total Gate Charge	$V_{DS} = -80\text{ V}, I_D = -16.5\text{ A}, V_{GS} = -10\text{ V}$ (Note 4)	–	30	39	nC
$Q_{gs}$	Gate–Source Charge		–	4.8	–	nC
$Q_{gd}$	Gate–Drain Charge		–	17	–	nC

### DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

$I_S$	Maximum Continuous Drain–Source Diode Forward Current		–	–	-16.5	A
$I_{SM}$	Maximum Pulsed Drain–Source Diode Forward Current		–	–	-66	A
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -16.5\text{ A}$	–	–	-4.0	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = -16.5\text{ A}, di_F/dt = 100\text{ A}/\mu\text{s}$	–	120	–	ns
$Q_{rr}$	Reverse Recovery Charge		–	0.52	–	$\mu\text{C}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

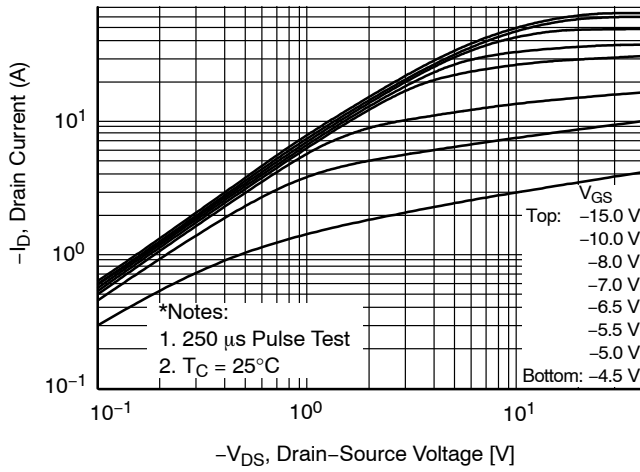


Figure 1. On-Region Characteristics

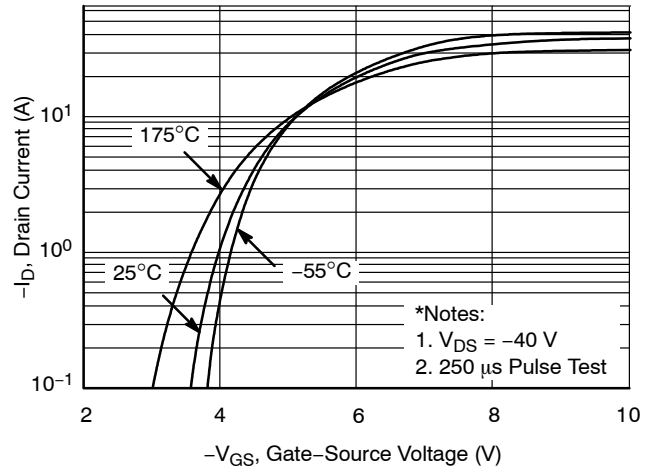


Figure 2. Transfer Characteristics

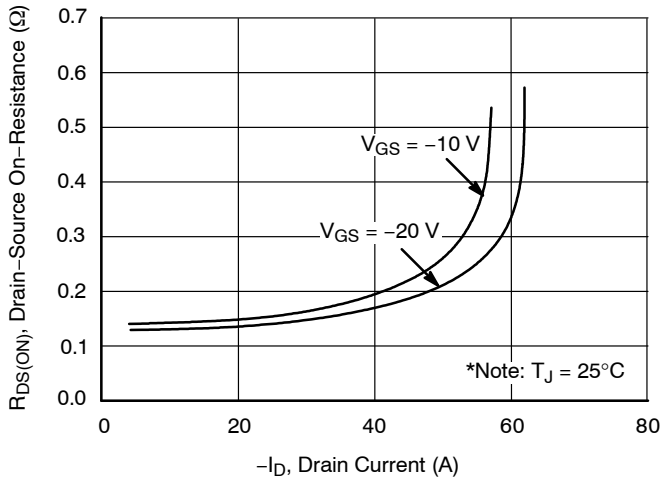


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

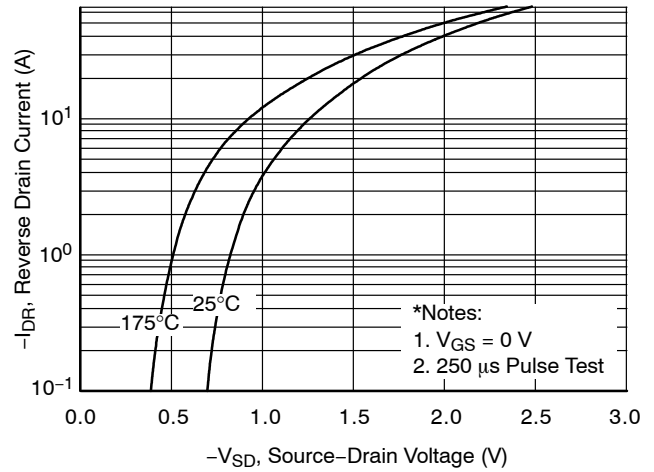


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

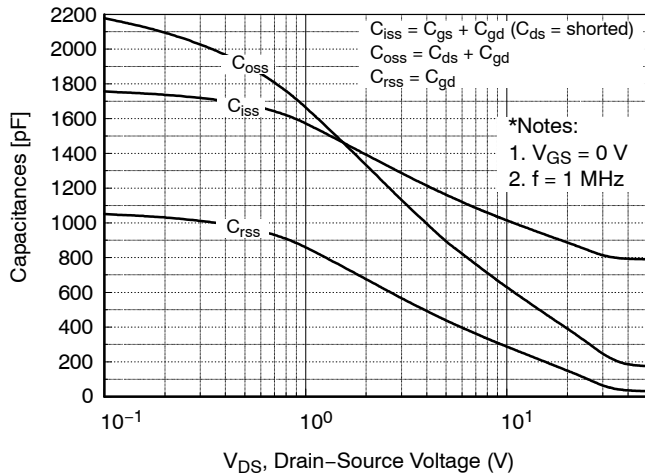


Figure 5. Capacitance Characteristics

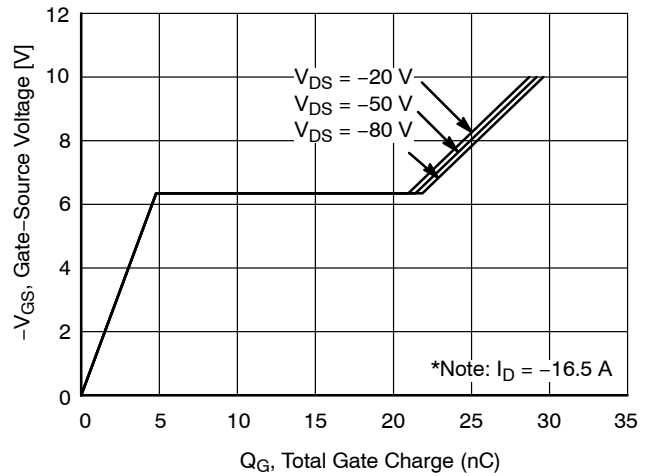
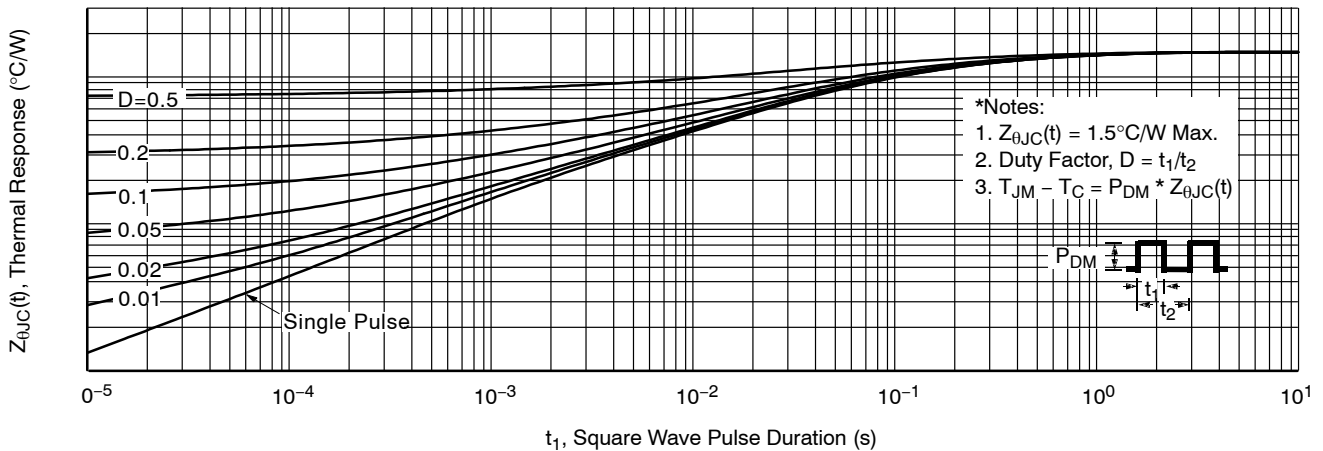
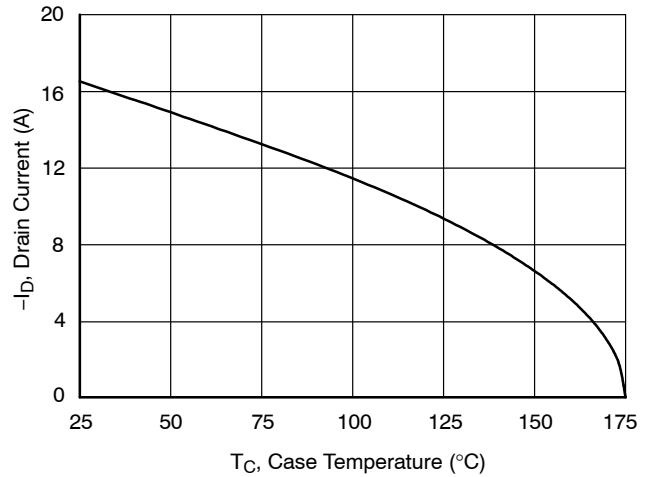
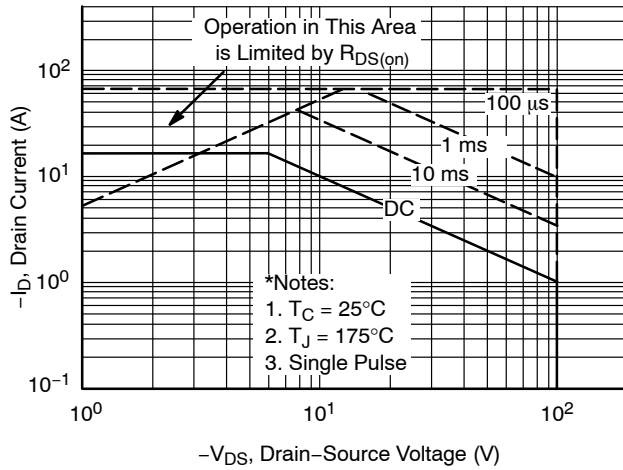
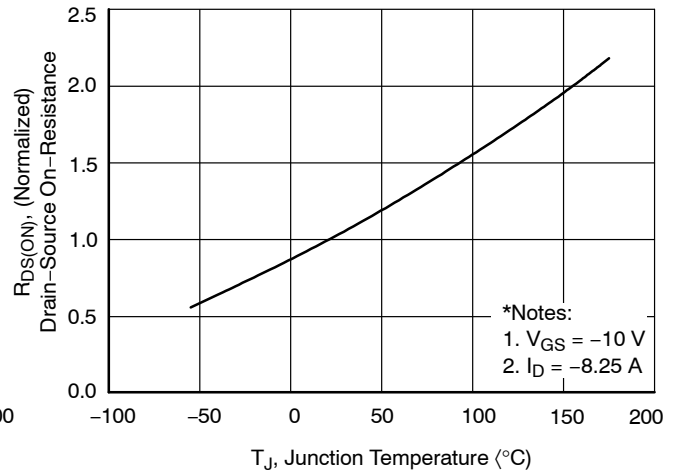
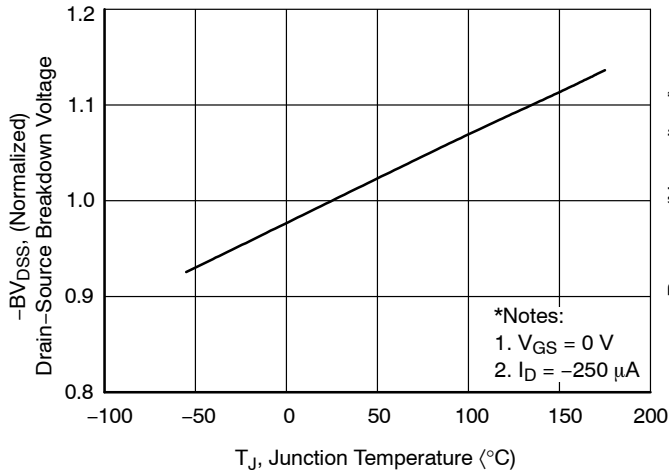


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (continued)



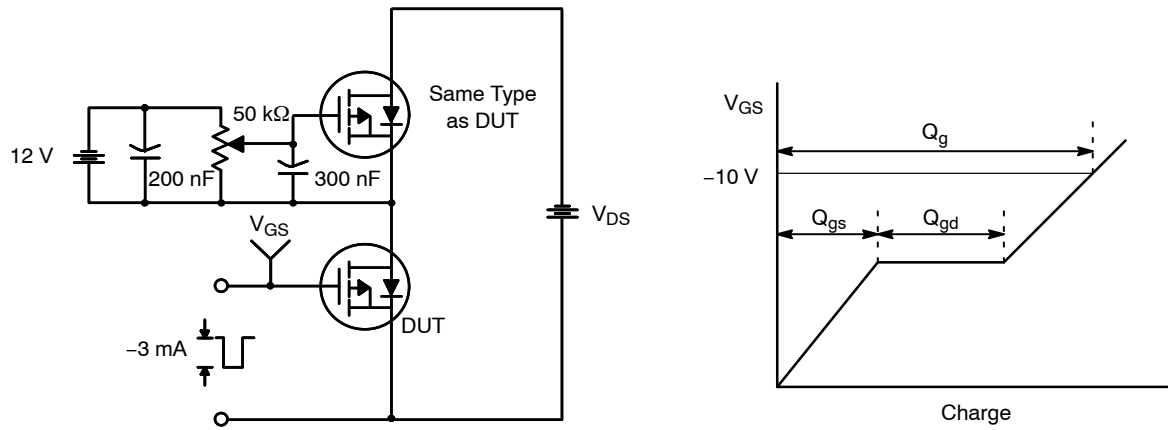


Figure 12. Gate Charge Test Circuit & Waveform

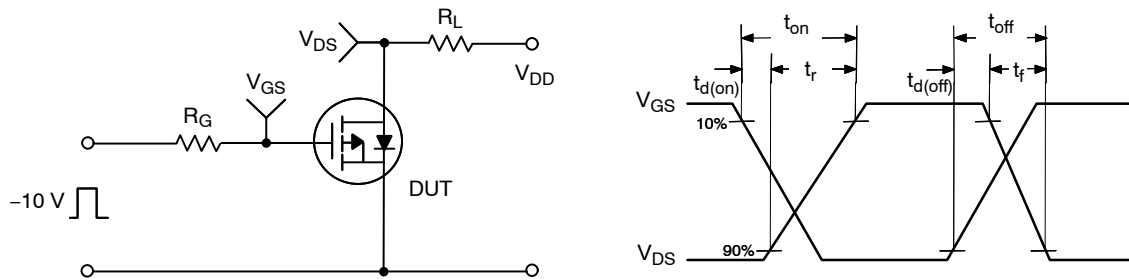


Figure 13. Resistive Switching Test Circuit & Waveforms

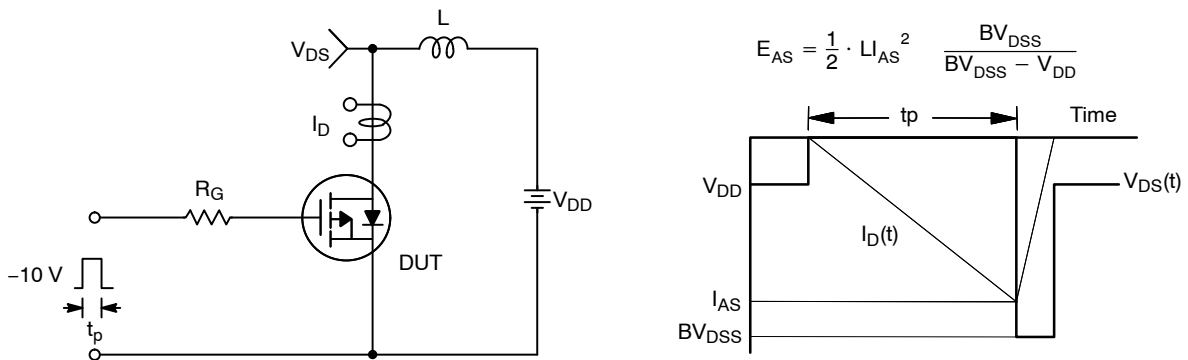
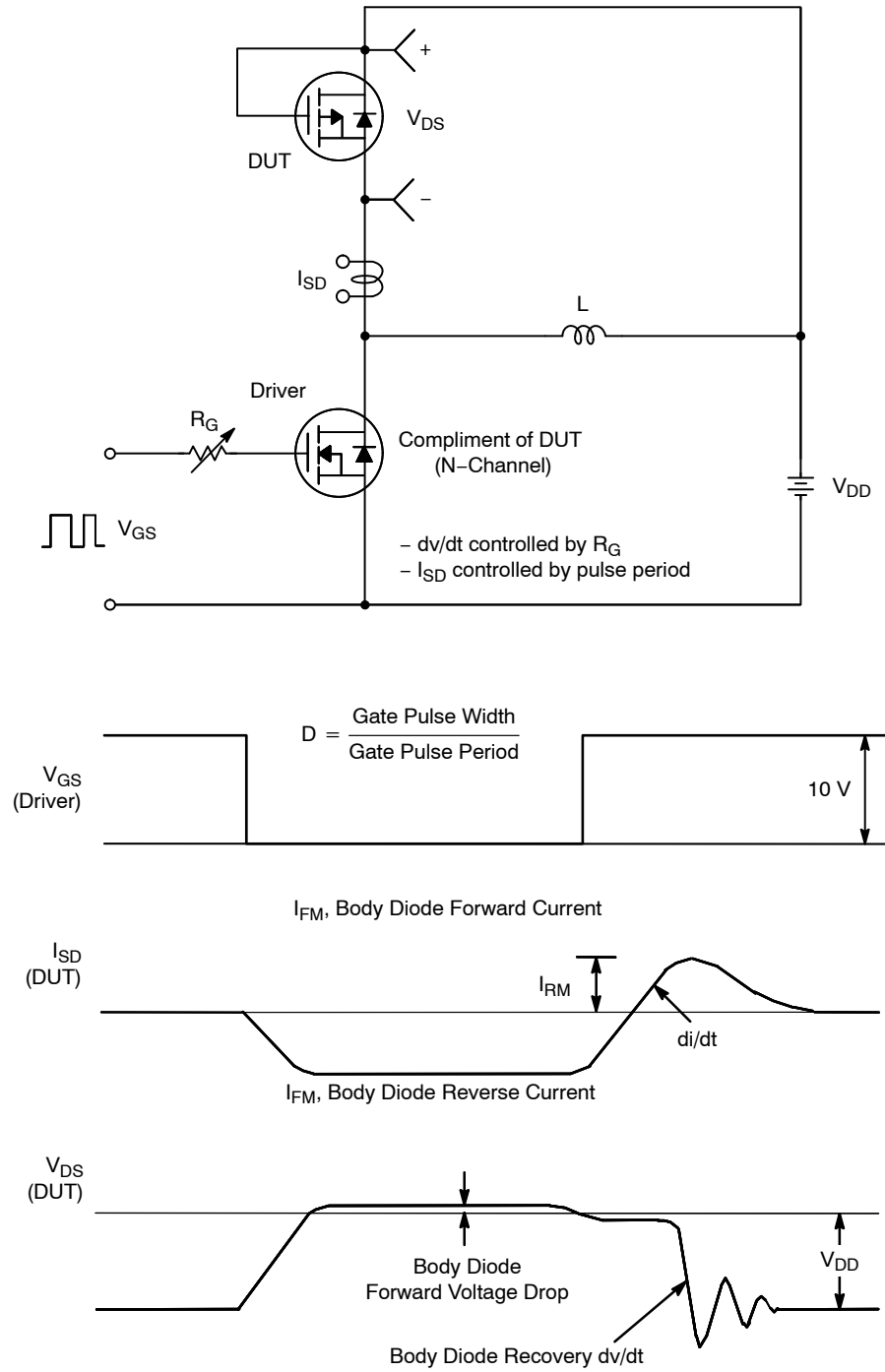
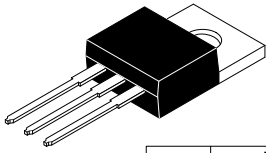


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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**Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms**



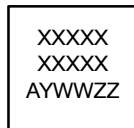
TO-220-3LD  
CASE 340AT  
ISSUE B

DATE 08 AUG 2022

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	4.00	--	4.70
A1	SEE NOTE "F"		
A2	2.10	--	2.85
b	0.55	--	1.00
b2	1.10	--	1.62
b4	1.42	--	1.62
c	0.36	--	0.60
D	13.90	--	16.30
D1	8.13	--	9.40
D2	11.50	--	14.30
D3	15.42	--	16.51
E	9.65	--	10.67
E1	7.59	--	8.65
e	2.40	--	2.67
H1	6.06	--	6.69
L	12.70	--	14.04
L1	2.70	--	4.10
P	3.50	--	4.00
Q	2.50	--	3.40
z	2.13 REF		
z1	2.06 REF		
θ	3°	--	5°

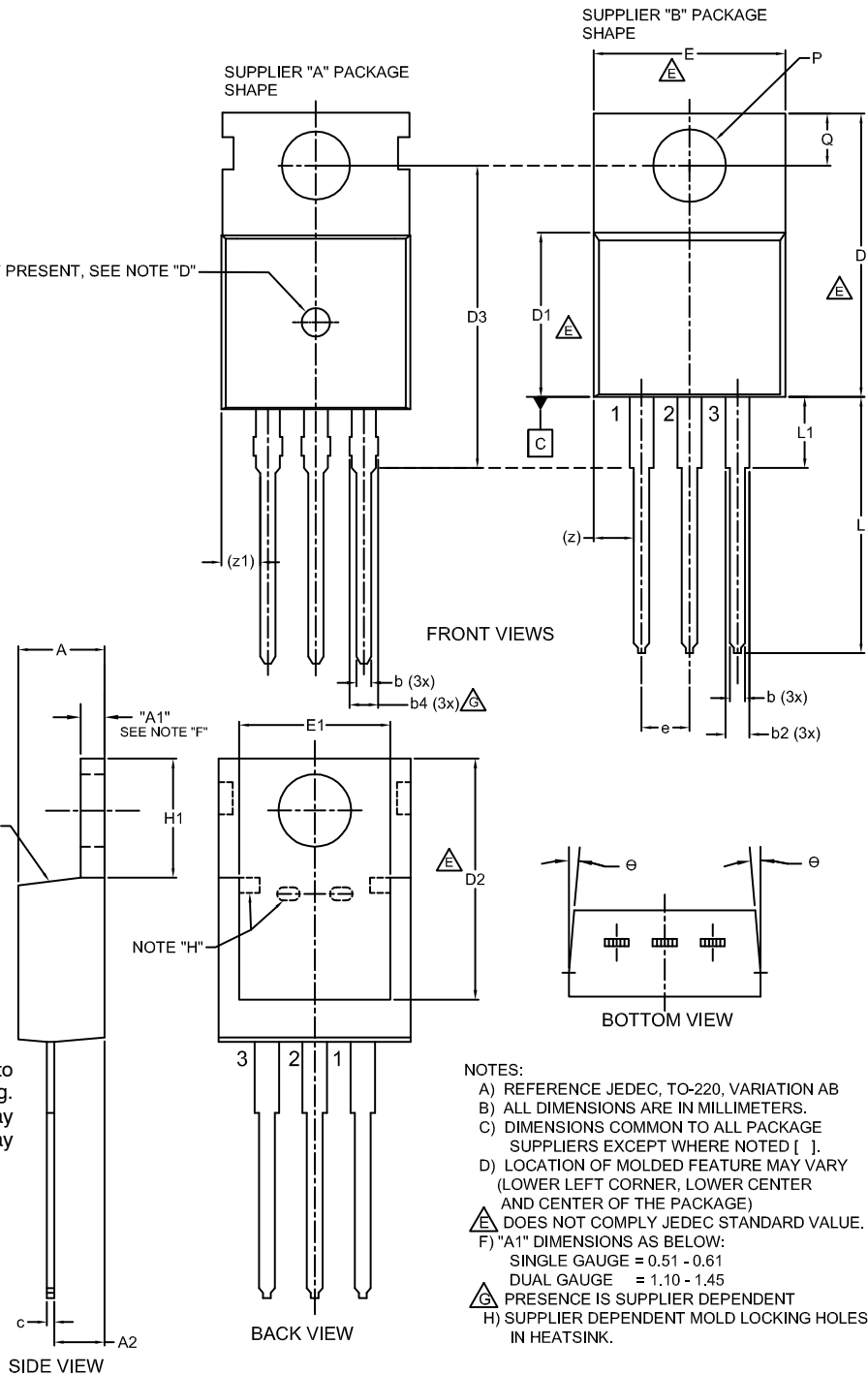
IF PRESENT, SEE NOTE "D"

GENERIC  
MARKING DIAGRAM\*



XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
ZZ = Assembly Lot Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



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