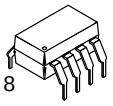
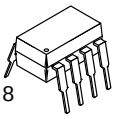
Optically Isolated Error Amplifier

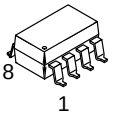
FOD2711A



PDIP8 6.6x3.81, 2.54P
CASE 646BW



PDIP8 9.655x6.61, 2.54P
CASE 646CQ



PDIP8 GW
CASE 709AC

Description

The FOD2711A Optically Isolated Amplifier consists of the popular AZ431L precision programmable shunt reference and an optocoupler. The optocoupler is a gallium arsenide (GaAs) light emitting diode optically coupled to a silicon phototransistor. The reference voltage tolerance is 1%. The current transfer ratio (CTR) ranges from 100% to 200%.

It is primarily intended for use as the error amplifier/reference voltage/optocoupler function in isolated AC to DC power supplies and dc/dc converters.

When using the FOD2711A, power supply designers can reduce the component count and save space in tightly packaged designs. The tight tolerance reference eliminates the need for adjustments in many applications.

The device comes in a 8−pin dip white package.

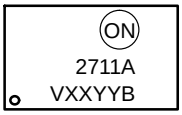
Features

- Optocoupler, Precision Reference and Error Amplifier in Single Package
- 1.240 V ±1% Reference
- CTR 100% to 200%
- 5,000 V RMS Isolation
- UL Approval E90700, Volume 2
- These are Pb−Free Devices

Applications

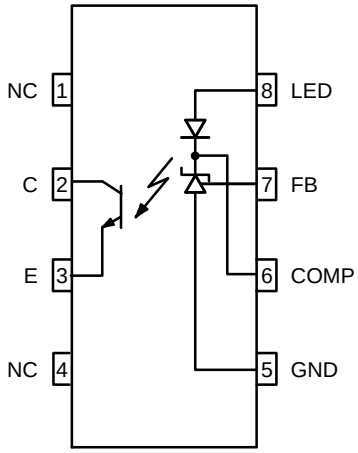
- Power Supplies Regulation
- DC to DC Converters

MARKING DIAGRAM



2711A	=	Device Code
V	=	VDE Mark (Note: Only Appears on Parts Ordered with VDE Option − See Order Entry Table)
XX	=	Two Digit Year Code, e.g., “03”
YY	=	Two Digit Work Week Ranging from “01” to “53”
B	=	Assembly Package Code

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

PIN DEFINITIONS

Pin No.	Pin Name	Pin Description
1	NC	Not Connected
2	C	Phototransistor Collector
3	E	Phototransistor Emitter
4	NC	Not connected
5	GND	Ground
6	COMP	Error Amplifier Compensation. This pin is the output of the error amplifier.*
7	FB	Voltage Feedback. This pin is the inverting input to the error amplifier
8	LED	Anode LED. This pin is the input to the light emitting diode.

*The compensation network must be attached between pins 6 and 7.

TYPICAL APPLICATION

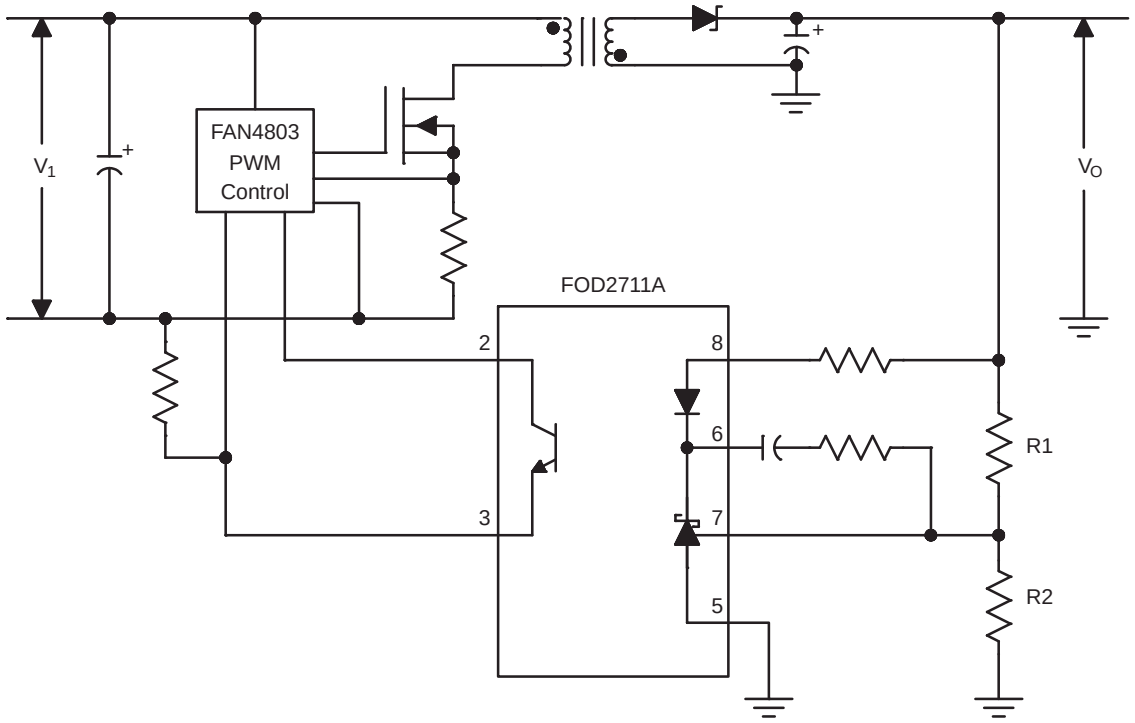


Figure 1. Typical Application

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	−40 to +125	°C
T_{OPR}	Operating Temperature	−40 to +85	°C
T_{SOL}	Lead Solder Temperature	260 for 10 sec.	°C
V_{LED}	Input Voltage	13.2	V
I_{LED}	Input DC Current	20	mA
V_{CEO}	Collector−Emitter Voltage	30	V
V_{ECO}	Emitter−Collector Voltage	7	V
I_C	Collector Current	50	mA
PD1	Input Power Dissipation (Note 1)	145	mW
PD2	Transistor Power Dissipation (Note 2)	85	mW
PD3	Total Power Dissipation (Note 3)	145	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Derate linearly from 25°C at a rate of 2.42 mW/°C.
2. Derate linearly from 25°C at a rate of 1.42 mW/°C.
3. Derate linearly from 25°C at a rate of 2.42 mW/°C.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
V_F	LED Forward Voltage	I_{LED} = 10 mA, V_{COMP} = V_{FB} (Figure 2)	–	–	1.5	V
V_{REF}	Reference Voltage −40°C to +85°C	V_{COMP} = V_{FB}, I_{LED} = 10 mA (Figure 2)	1.221	–	1.259	V
	25°C		1.228	1.240	1.252	
$V_{REF\ (DEV)}$	Deviation of V_{REF} Over Temperature (Note 4)	T_A = −40 to +85°C	–	4	12	mV
ΔV_{REF} / ΔV_{COMP}	Ratio of Vref Variation to the Output of the Error Amplifier	I_{LED} = 10 mA, V_{COMP} = V_{REF} to 12 V (Figure 3)	–	−1.5	−2.7	mV/V
I_{REF}	Feedback Input Current	I_{LED} = 10 mA, R1 = 10 kΩ (Figure 4)	–	0.15	0.5	μA
$I_{REF\ (DEV)}$	Deviation of I_{REF} Over Temperature (Note 4)	T_A = −40°C to +85°C	–	0.15	0.3	μA
$I_{LED\ (MIN)}$	Minimum Drive Current	V_{COMP} = V_{FB} (Figure 2)	–	55	80	μA
$I_{(OFF)}$	Off−State Error Amplifier Current	V_{LED} = 6 V, V_{FB} = 0 (Figure 5)	–	0.001	0.1	μA
$\|Z_{OUT}\|$	Error Amplifier Output Impedance (Note 5)	V_{COMP} = V_{FB}, I_{LED} = 0.1 mA to 15 mA, f < 1 kHZ)	–	0.25	–	Ω
OUTPUT CHARACTERISTICS						
I_{CEO}	Collector Dark Current	V_{CE} = 10 V (Figure 6)	–	–	50	nA
BV_{ECO}	Emitter−Collector Voltage Breakdown	I_E = 100 μA	7	–	–	V
BV_{CEO}	Collector−Emitter Voltage Breakdown	I_C = 1.0 mA	70	–	–	V
TRANSFER CHARACTERISTICS						
CTR	Current Transfer Ratio	I_{LED} = 10 mA, V_{COMP} = V_{FB}, V_{CE} = 5 V (Figure 7)	100	–	200	%
$V_{CE\ (SAT)}$	Collector−Emitter Saturation Voltage	I_{LED} = 10 mA, V_{COMP} = V_{FB}, I_C = 2.5 mA (Figure 7)	–	–	0.4	V
ISOLATION CHARACTERISTICS						
I_{I-O}	Input−Output Insulation Leakage Current	RH = 45%, T_A = 25°C, t = 5 s, V_{I-O} = 3000 VDC (Note 6)	–	–	1.0	μA
V_{ISO}	Withstand Insulation Voltage	RH ≤ 50%, T_A = 25°C, t = 1 min. (Note 6)	5000	–	–	Vrms
R_{I-O}	Resistance (Input to Output)	V_{I-O} = 500 VDC (Note 6)	–	10^{12}	–	Ω
SWITCHING CHARACTERISTICS						
BW	Bandwidth	(Figure 8)	–	10	–	kHZ
|CMH|	Common Mode Transient Immunity at Output HIGH	I_{LED} = 0 mA, |Vcm| = 10 V_{PP}, R_L = 2.2 kΩ (Note 7) (Figure 9)	–	1.0	–	kV/μs
|CML|	Common Mode Transient Immunity at Output LOW	I_{LED} = 1mA, |Vcm| = 10 V_{PP}, R_L = 2.2 kΩ (Note 7) (Figure 9)	–	1.0	–	kV/μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The deviation parameters $V_{REF(DEV)}$ and $I_{REF(DEV)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full−range temperature coefficient of the reference input voltage, ΔV_{REF}, is defined as:

$$|\Delta V_{REF}|(ppm/°C) = \frac{\{V_{REF(DEV)} / V_{REF}\,(T_A = 25°C)\} \times 10^6}{\Delta T_A} \qquad \text{(eq. 1)}$$

where ΔT_A is the rated operating free−air temperature range of the device.

5. The dynamic impedance is defined as $|Z_{OUT}| = \Delta V_{COMP} / \Delta I_{LED}$. When the device is operating with two external resistors (see Figure 3), the total dynamic impedance of the circuit is given by:

$$|Z_{OUT,TOT}| = \frac{\Delta V}{\Delta I} \approx |Z_{OUT}| \times \left[1 + \frac{R1}{R2}\right] \qquad \text{(eq. 2)}$$

6. Device is considered as a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
7. Common mode transient immunity at output high is the maximum tolerable (positive) dVcm/dt on the leading edge of the common mode impulse signal, Vcm, to assure that the output will remain high. Common mode transient immunity at output low is the maximum tolerable (negative) dVcm/dt on the trailing edge of the common pulse signal,Vcm, to assure that the output will remain low.

TEST CIRCUITS

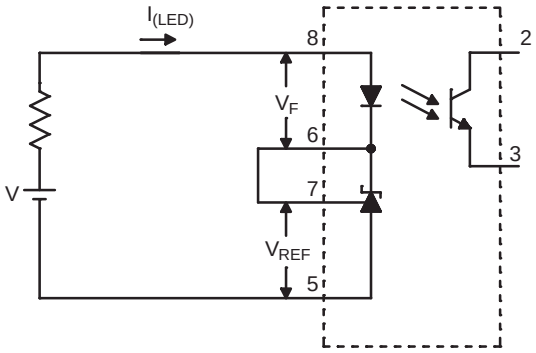


Figure 2. V_{REF}, V_F, I_{LED} (min.) Test Circuit

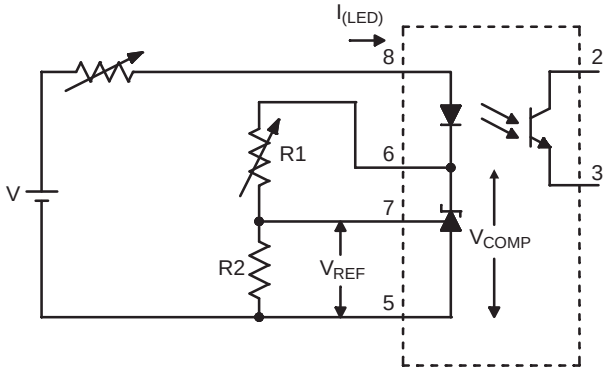


Figure 3. ΔV_{REF} / ΔV_{COMP} Test Circuit

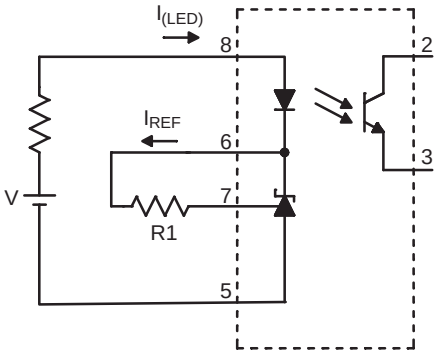


Figure 4. REF Test Circuit

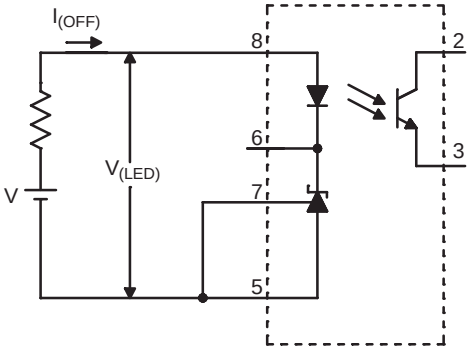


Figure 5. $I_{(OFF)}$ Test Circuit

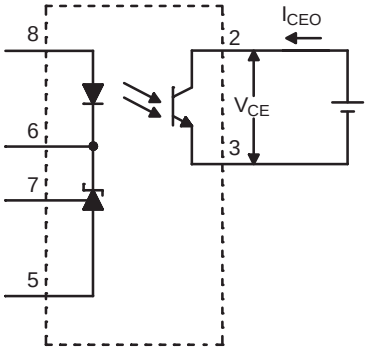


Figure 6. I_{CEO} Test Circuit

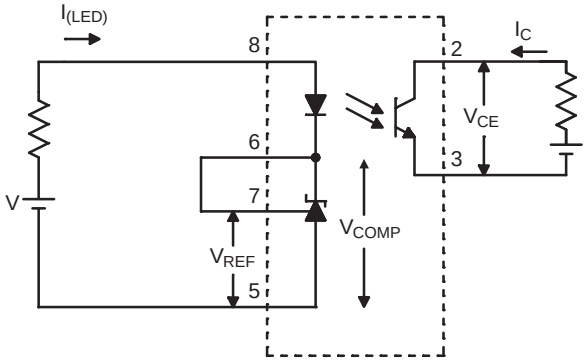


Figure 7. CTR, $V_{CE(sat)}$ Test Circuit

TEST CIRCUITS (Continued)

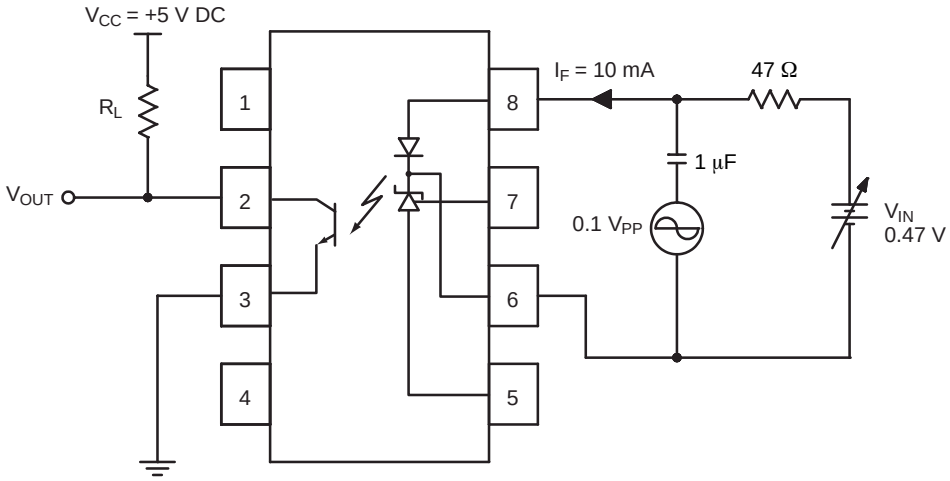


Figure 8. Frequency Response Test Circuit

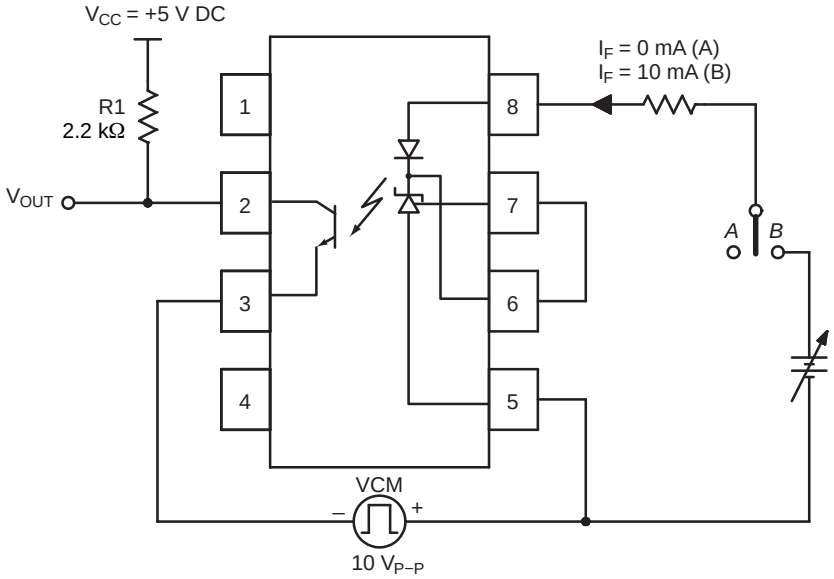


Figure 9. CMH and CML Test Circuit

TYPICAL PERFORMANCE CURVES

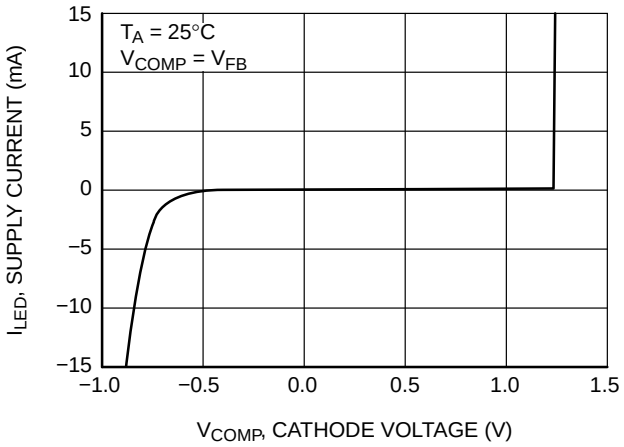


Figure 10a. LED Current vs. Cathode Voltage

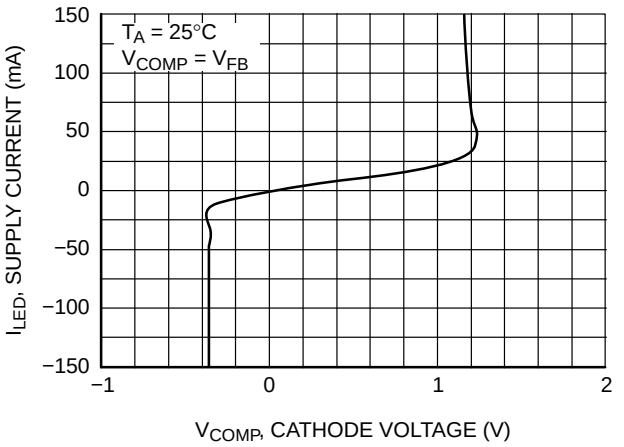


Figure 10b. LED Current vs. Cathode Voltage

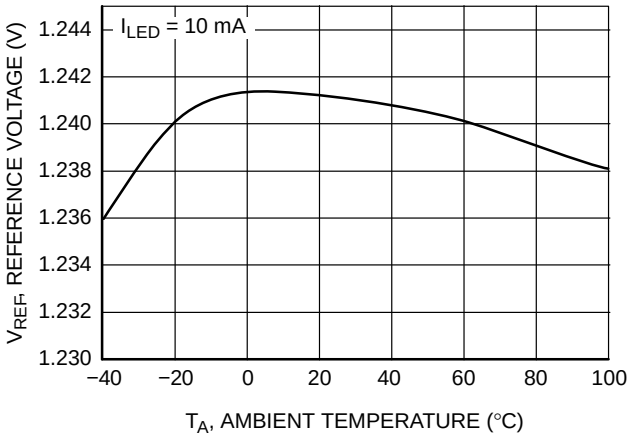


Figure 11. Reference Voltage vs. Ambient Temperature

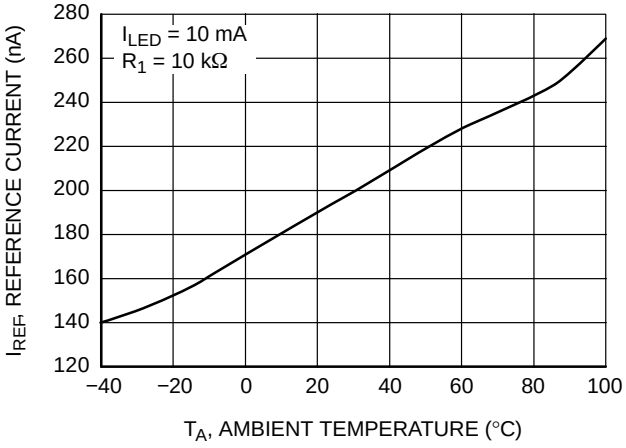


Figure 12. Reference Current vs. Ambient Temperature

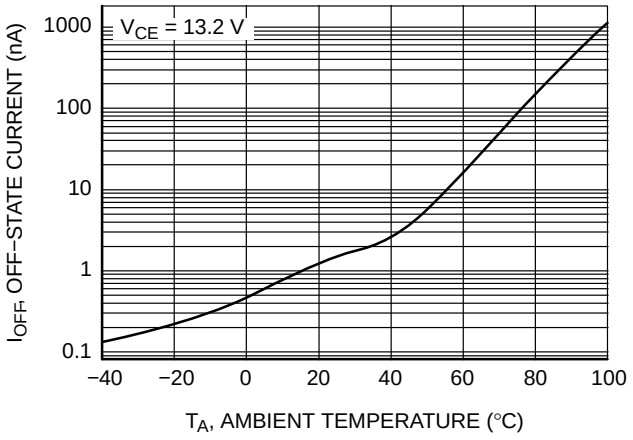


Figure 13. Off−State Current vs. Ambient Temperature

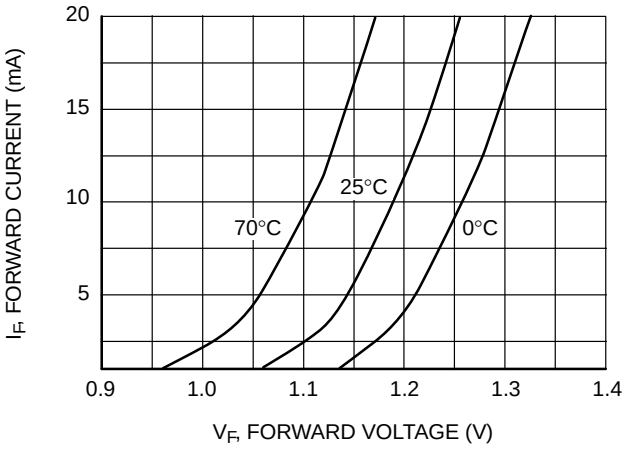


Figure 14. Forward Current vs. Forward Voltage

TYPICAL PERFORMANCE CURVES (Continued)

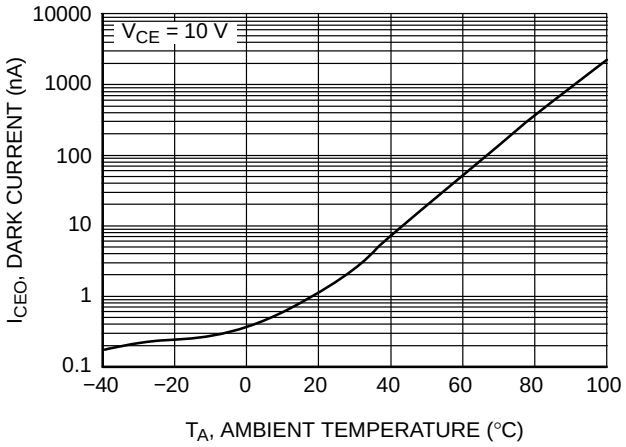


Figure 15. Dark Current vs. Ambient Temperature

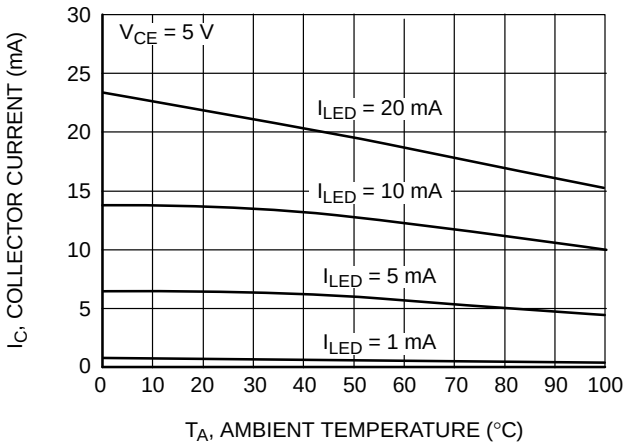


Figure 20. Collector Current vs. Ambient Temperature

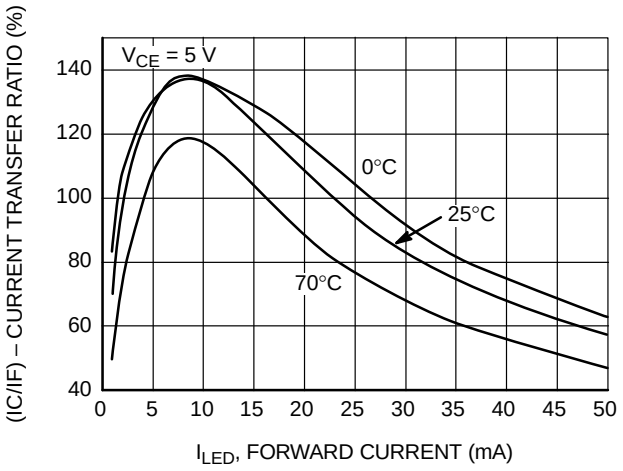


Figure 16. Current Transfer Ratio vs. LED Current

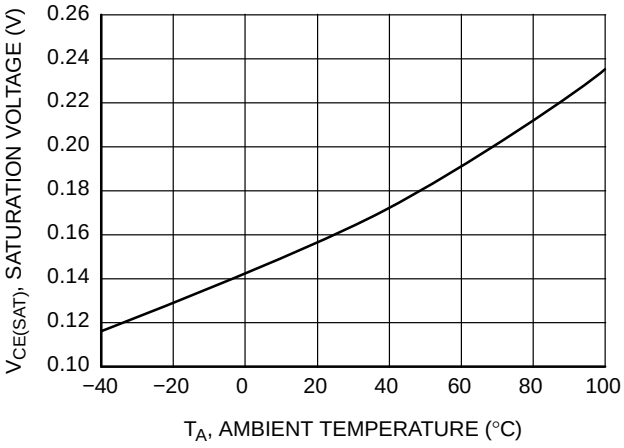


Figure 17. Saturation Voltage vs. Ambient Temperature

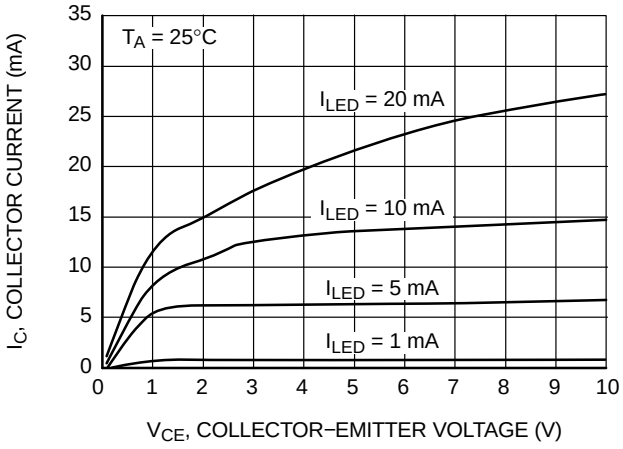


Figure 18. Collector Current vs. Collector Voltage

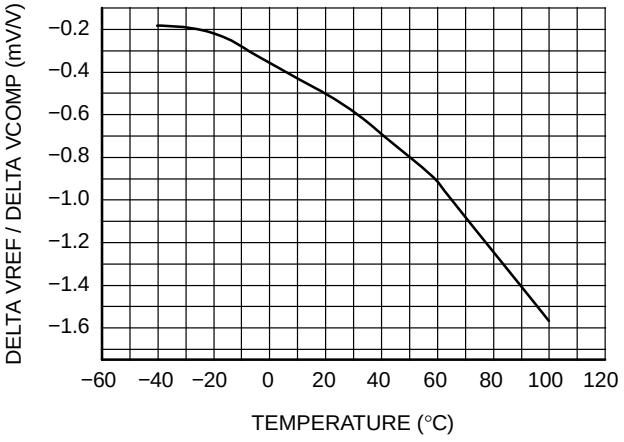


Figure 19. Rate of Change Vref to Vcomp vs. Temperature

TYPICAL PERFORMANCE CURVES (Continued)

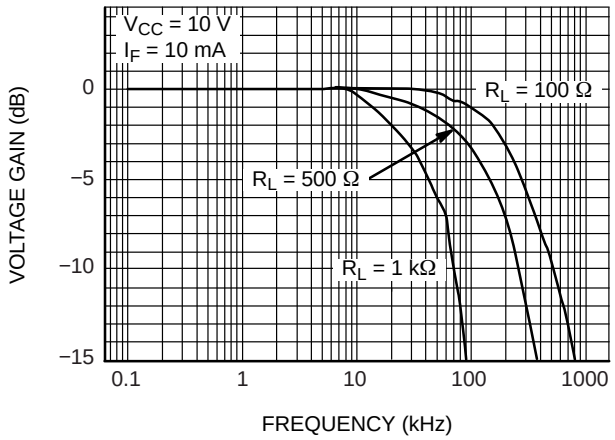


Figure 21. Voltage Gain vs. Frequency

THE FOD2711A

The FOD2711A is an optically isolated error amplifier. It incorporates three of the most common elements necessary to make an isolated power supply, a reference voltage, an error amplifier, and an optocoupler. It is functionally equivalent to the popular AZ431L shunt voltage regulator plus the CNY17F−3 optocoupler.

Powering the Secondary Side

The LED pin in the FOD2711A powers the secondary side, and in particular provides the current to run the LED. The actual structure of the FOD2711A dictates the minimum voltage that can be applied to the LED pin: The error amplifier output has a minimum of the reference voltage, and the LED is in series with that. Minimum voltage applied to the LED pin is thus 1.24 V + 1.5 V = 2.74 V. This voltage can be generated either directly from the output of the converter, or else from a slaved secondary winding. The secondary winding will not affect regulation, as the input to the FB pin may still be taken from the output winding.

The LED pin needs to be fed through a current limiting resistor. The value of the resistor sets the amount of current through the LED, and thus must be carefully selected in conjunction with the selection of the primary side resistor.

Feedback

Output voltage of a converter is determined by selecting a resistor divider from the regulated output to the FB pin. The FOD2711A attempts to regulate its FB pin to the reference voltage, 1.24 V. The ratio of the two resistors should thus be:

$$\frac{R_{TOP}}{H_{BOTTOM}} = \frac{V_{OUT}}{V_{REF}} - 1 \qquad \text{(eq. 3)}$$

The absolute value of the top resistor is set by the input offset current of 0.8 μA. To achieve 1% accuracy, the resistance of R_{TOP} should be:

$$\frac{V_{OUT} - 1.24}{R_{TOP}} > 80\ \mu A \qquad \text{(eq. 4)}$$

Compensation

The compensation pin of the FOD2711A provides the opportunity for the designer to design the frequency response of the converter. A compensation network may be placed between the COMP pin and the FB pin. In typical low−bandwidth systems, a 0.1 μF capacitor may be used. For converters with more stringent requirements, a network should be designed based on measurements of the system's loop. An excellent reference for this process may be found in "Practical Design of Power Supplies" by Ron Lenk, IEEE Press, 1998.

Secondary Ground

The GND pin should be connected to the secondary ground of the converter.

No Connect Pins

The NC pins have no internal connection. They should not have any connection to the secondary side, as this may compromise the isolation structure.

Photo−Transistor

The Photo−transistor is the output of the FOD2711A. In a normal configuration the collector will be attached to a pull−up resistor and the emitter grounded. There is no base connection necessary.

The value of the pull−up resistor, and the current limiting resistor feeding the LED, must be carefully selected to account for voltage range accepted by the PWM IC, and for the variation in current transfer ratio (CTR) of the opto−isolator itself.

Example: The voltage feeding the LED pins is +12 V, the voltage feeding the collector pull−up is +10 V, and the PWM IC is the **onsemi** KA1H0680, which has a 5 V reference. If we select a 10 kΩ resistor for the LED, the maximum current the LED can see is:

$$(12\ V - 2.74\ V) / 10\ k\Omega = 926\ \mu A. \qquad \text{(eq. 5)}$$

The CTR of the opto−isolator is a minimum of 100%, and so the minimum collector current of the photo−transistor when the diode is full on is also 926 μA. The collector resistor must thus be such that:

$$\frac{10\ V - 5\ V}{R_{COLLECTOR}} < 926\ \mu A \text{ or } R_{COLLECTOR} > 5.4\ k\Omega; \qquad \text{(eq. 6)}$$

select 10 kΩ to allow some margin.

REFLOW PROFILE

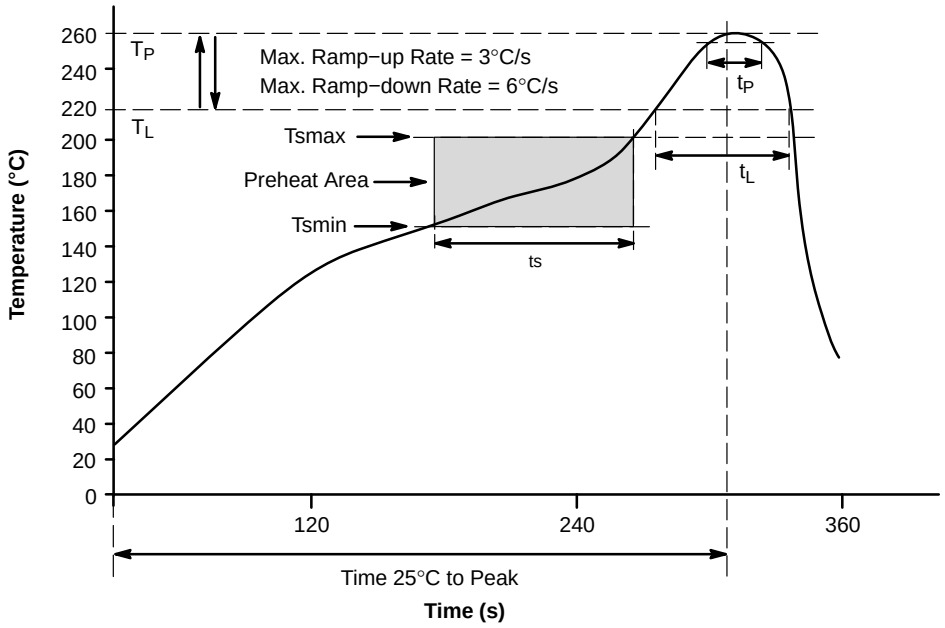


Figure 22. Reflow Profile

REFLOW PROFILE

Profile Feature	Pb−Free Assembly Profile
Temperature Min. (Tsmin)	150°C
Temperature Max. (Tsmax)	200°C
Time (t_S) from (Tsmin to Tsmax)	60−120 s
Ramp−up Rate (t_L to t_P)	3°C/s max.
Liquidous Temperature (T_L)	217°C
Time (t_L) Maintained Above (T_L)	60−150 s
Peak Body Package Temperature	260°C +0°C / −5°C
Time (t_P) within 5°C of 260°C	30 s
Ramp−down Rate (T_P to T_L)	6°C/s max.
Time 25°C to Peak Temperature	8 min max.

ORDERING INFORMATION

Option	Example Part Number	Description†
No Option	FOD2711A	Standard Through Hole
S	FOD2711AS	Surface Mount Lead Bend
SD	FOD2711ASD	Surface Mount, Tape and Reel
T	FOD2711AT	0.4” Lead Spacing
V	FOD2711AV	VDE0884
TV	FOD2711ATV	VDE0884; 0.4” Lead Spacing
SV	FOD2711ASV	VDE0884; Surface Mount
SDV	FOD2711ASDV	VDE0884; Surface Mount, Tape and Reel

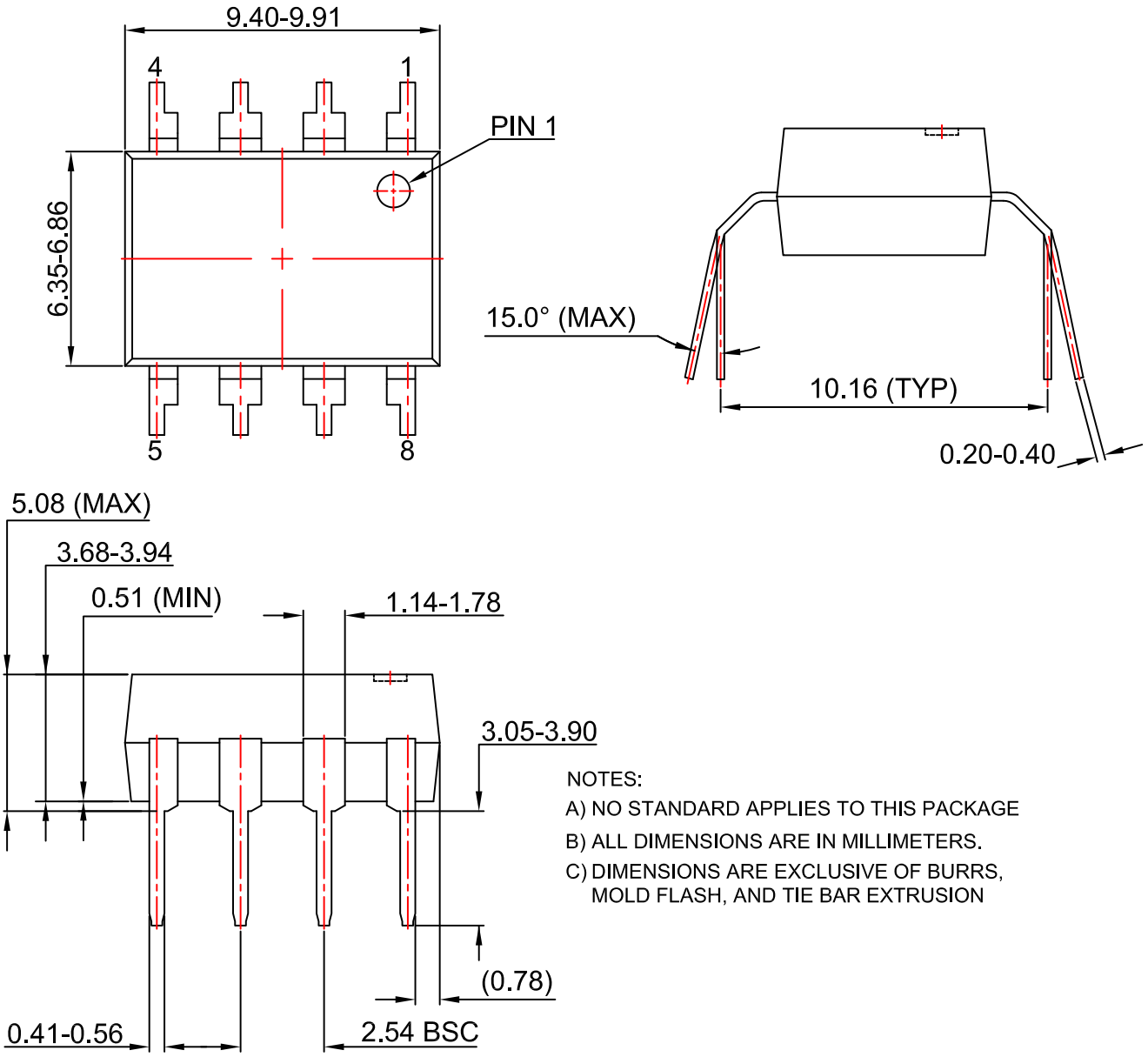
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

PDIP8 6.6x3.81, 2.54P
CASE 646BW
ISSUE O

DATE 31 JUL 2016



NOTES:
A) NO STANDARD APPLIES TO THIS PACKAGE
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSION

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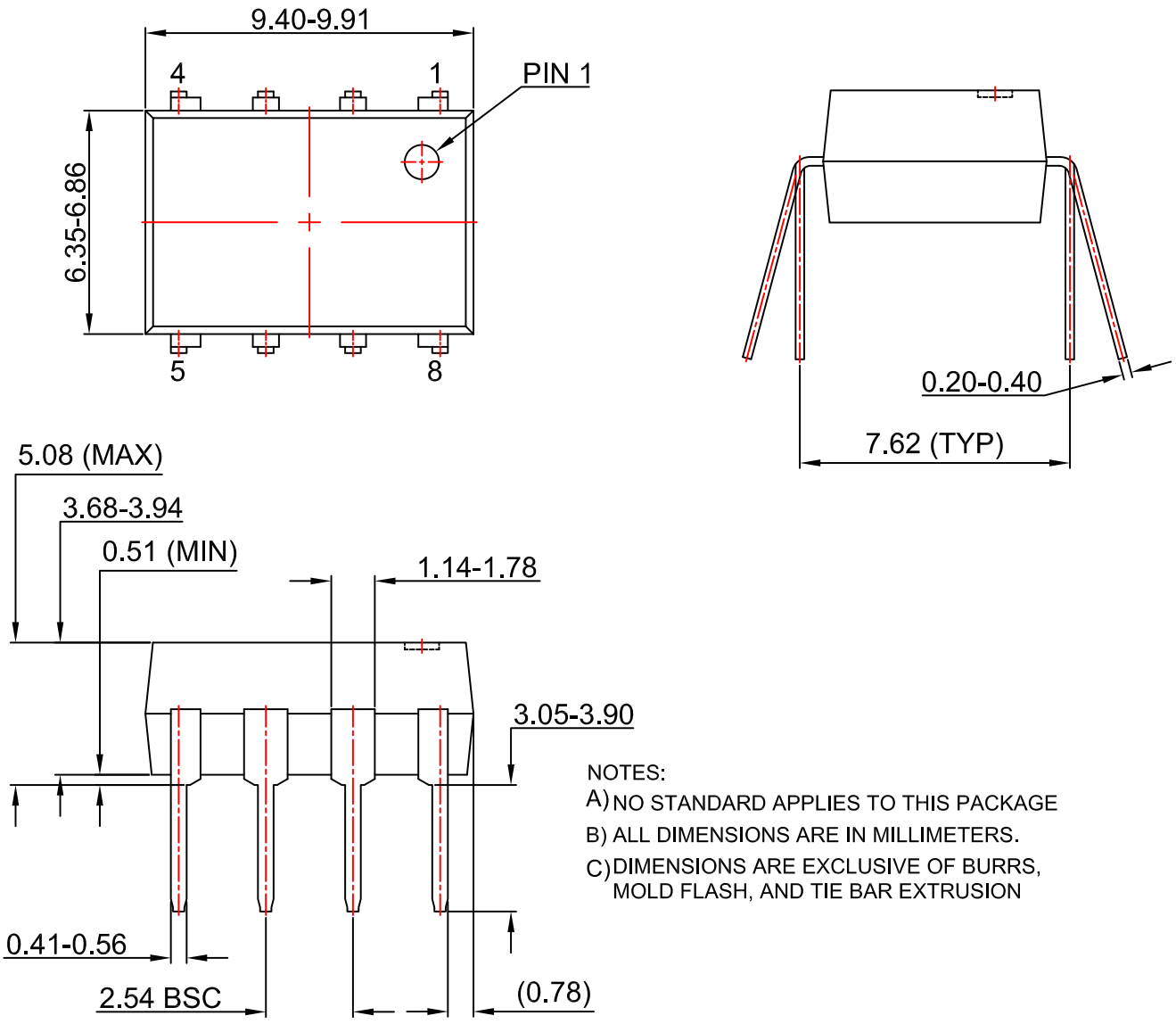
PDIP8 9.655x6.6, 2.54P
CASE 646CQ
ISSUE O

DATE 18 SEP 2017



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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

PDIP8 GW
CASE 709AC
ISSUE O

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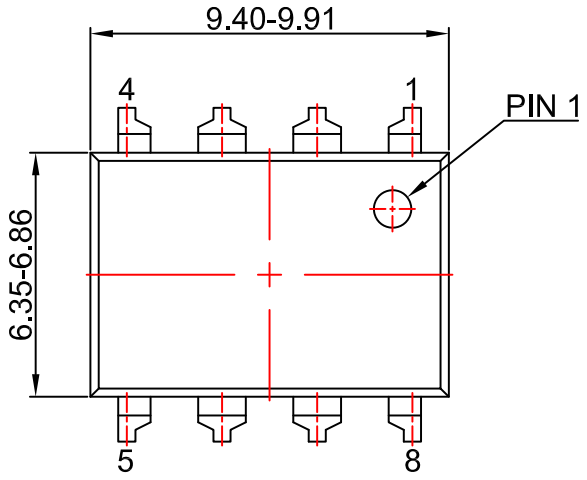
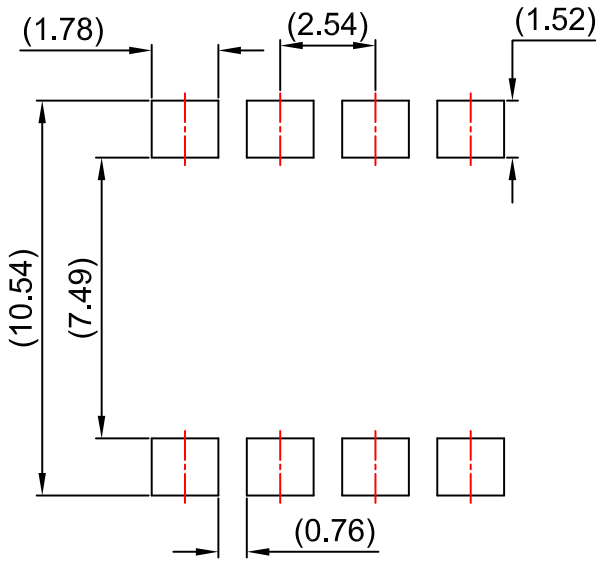
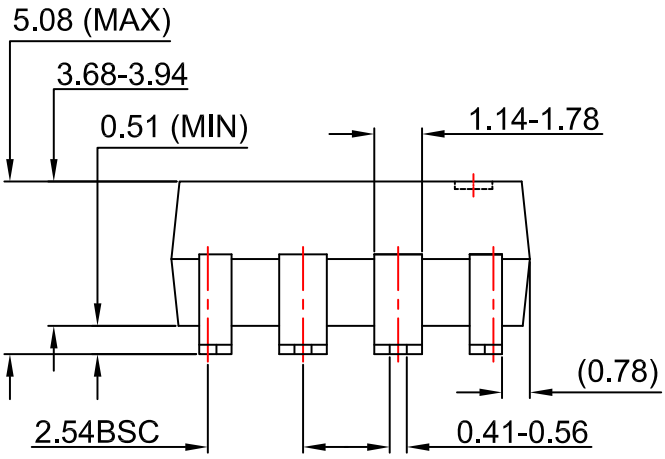
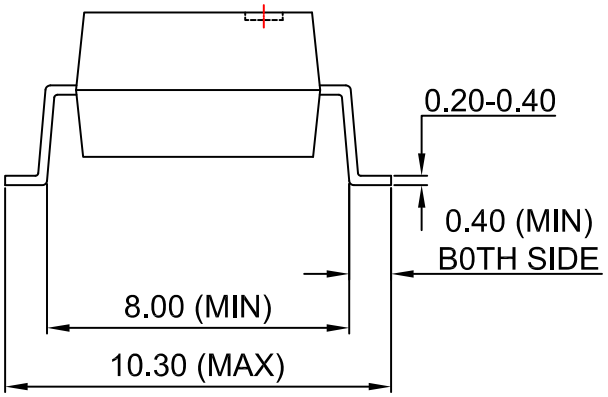




LAND PATTERN RECOMMENDATION





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