# Motion SPM® 45 Series

# FNA41560T2

### General Description

FNA41560T2 is a Motion SPM 45 module providing a fully−featured, high−performance inverter output stage for AC Induction, BLDC, and PMSM motors. These modules integrate optimized gate drive of the built−in IGBTs to minimize EMI and losses, while also providing multiple on−module protection features including under−voltage lockouts, over−current shutdown, thermal monitoring of drive IC, and fault reporting. The built−in, high−speed HVIC requires only a single supply voltage and translates the incoming logic−level gate inputs to the high−voltage, high−current drive signals required to properly drive the module's internal IGBTs. Separate negative IGBT terminals are available for each phase to support the widest variety of control algorithms.

### Features

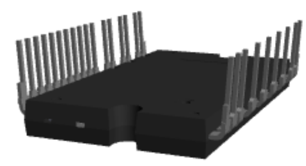
- UL Certified No. E209204 (UL1557)
- 600 V – 15 A 3−Phase IGBT Inverter with Integral Gate Drives and Protection
- Low Thermal Resistance Using Ceramic Substrate
- Low−Loss, Short−Circuit−Rated IGBTs
- Built−In Bootstrap Diodes and Dedicated Vs Pins Simplify PCB Layout
- Built−In NTC Thermistor for Temperature Monitoring
- Separate Open−Emitter Pins from Low−Side IGBTs for Three−Phase Current Sensing
- Single−Grounded Power Supply
- Isolation Rating of 2000 Vrms / 1 min.
- This is a Pb−Free and Halogen Free/BFR Free Device

### Applications

- Motion Control – Home Appliance / Industrial Motor

### Related Resources

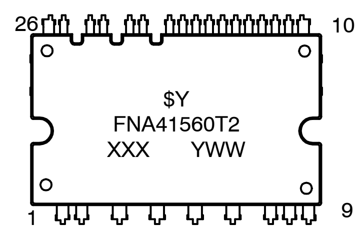
- AN−9084 – Smart Power Module, Motion SPM® 45 H V3 Series User's Guilde
- AN−9072 – Smart Power Module Motion SPM® in SPM45H Thermal Performance Information
- AN−9071 – Smart Power Module Motion SPM® in SPM45H Mounting Guidance
- AN−9760 – PCB Design Guidance for SPM®



3D Package Drawing (Click to Activate 3D Content)

**SPMAA−C26 / 26LD, PDD STD CERAMIC TYPE, LONG LEAD DUAL FORM TYPE CASE MODFC**

### MARKING DIAGRAM




| | | |
|---|---|---|
| $Y | = | **onsemi** Logo |
| FNA41560T2 | = | Specific Device Code |
| XXX | = | Trace Code |
| Y | = | Year |
| WW | = | Work Week |

### ORDERING INFORMATION

See detailed ordering and shipping information on page 14 of this data sheet.

**Integrated Power Functions**

- 600 V − 15 A IGBT inverter for three−phase DC / AC power conversion (refer to Figure 2)

**Integrated Drive, Protection, and System Control Functions**

- For inverter high−side IGBTs:
  gate−drive circuit, high−voltage isolated high−speed level−shifting control circuit,
  Under−Voltage Lock−Out Protection (UVLO)

NOTE: Available bootstrap circuit example is given in Figures 14

- For inverter low−side IGBTs:
  gate−drive circuit, Short−Circuit Protection (SCP) control supply circuit,
  Under−Voltage Lock−Out Protection (UVLO)
- Fault signaling:
  corresponding to UVLO (low−side supply) and SC faults
- Input interface:
  active−HIGH interface, works with 3.3 / 5 V logic, Schmitt−trigger input

**Pin Configuration**

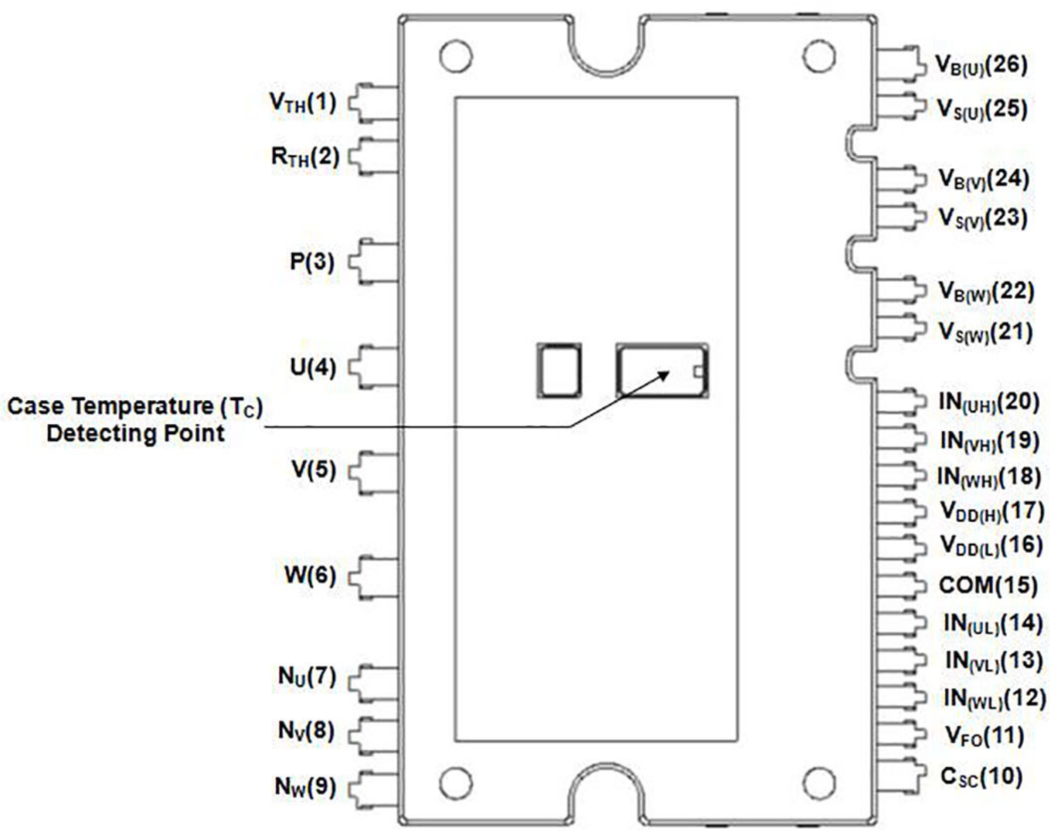
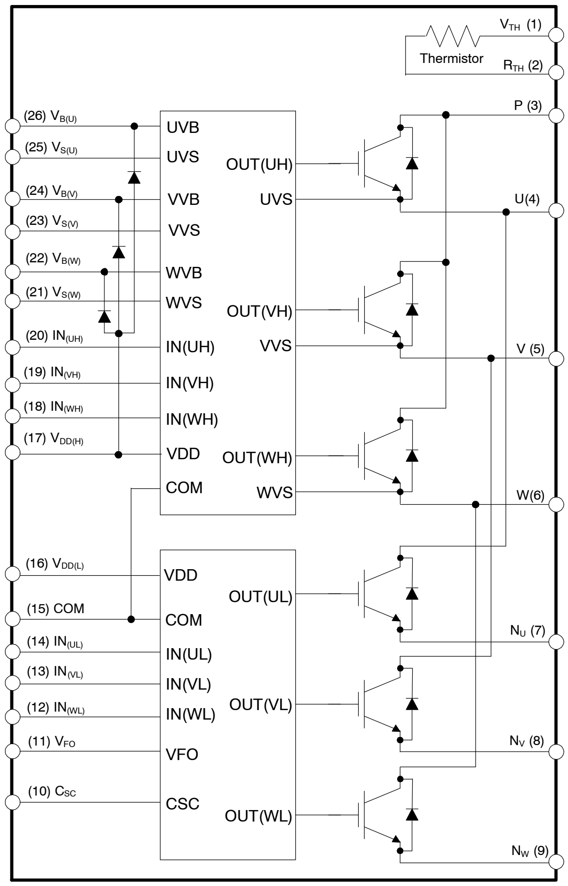



**Figure 1. Top View**

## PIN DESCRIPTIONS

| Pin No. | Pin Name | Pin Description |
|---|---|---|
| 1 | $V_{TH}$ | Thermistor Bias Voltage |
| 2 | $R_{TH}$ | Series Resistor for the Use of Thermistor (Temperature Detection) |
| 3 | P | Positive DC−Link Input |
| 4 | U | Output for U−Phase |
| 5 | V | Output for V−Phase |
| 6 | W | Output for W−Phase |
| 7 | $N_U$ | Negative DC−Link Input for U−Phase |
| 8 | $N_V$ | Negative DC−Link Input for V−Phase |
| 9 | $N_W$ | Negative DC−Link Input for W−Phase |
| 10 | $C_{SC}$ | Shut Down Input for Short−circuit Current Detection Input |
| 11 | $V_{FO}$ | Fault Output |
| 12 | $IN_{(WL)}$ | Signal Input for Low−Side W−Phase |
| 13 | $IN_{(VL)}$ | Signal Input for Low−Side V−Phase |
| 14 | $IN_{(UL)}$ | Signal Input for Low−Side U−Phase |
| 15 | COM | Common Supply Ground |
| 16 | $V_{DD(L)}$ | Low−Side Common Bias Voltage for IC and IGBTs Driving |
| 17 | $V_{DD(H)}$ | High−Side Common Bias Voltage for IC and IGBTs Driving |
| 18 | $IN_{(WH)}$ | Signal Input for High−Side W−Phase |
| 19 | $IN_{(VH)}$ | Signal Input for High−Side V−Phase |
| 20 | $IN_{(UH)}$ | Signal Input for High−Side U−Phase |
| 21 | $VS_{(W)}$ | High−Side Bias Voltage Ground for W−Phase IGBT Driving |
| 22 | $VB_{(W)}$ | High−Side Bias Voltage for W−Phase IGBT Driving |
| 23 | $VS_{(V)}$ | High−Side Bias Voltage Ground for V−Phase IGBT Driving |
| 24 | $VB_{(V)}$ | High−Side Bias Voltage for V−Phase IGBT Driving |
| 25 | $VS_{(U)}$ | High−Side Bias Voltage Ground for U−Phase IGBT Driving |
| 26 | $VB_{(U)}$ | High−Side Bias Voltage for U−Phase IGBT Driving |

### Internal Equivalent Circuit and Input/Output Pins




NOTES:
1. Inverter high−side is composed of three normal−IGBTs, freewheeling diodes, and one control IC for each IGBT.
2. Inverter low−side is composed of three sense−IGBTs, freewheeling diodes, and one control IC for each IGBT. It has gate drive and protection functions.
3. Inverter power side is composed of four inverter DC−link input terminals and three inverter output terminals.

**Figure 2. Internal Block Diagram**

**ABSOLUTE MAXIMUM RATINGS** ($T_J$ = 25°C, unless otherwise specified)

| Symbol | Parameter | Conditions | Rating | Unit |
|---|---|---|---|---|
| **INVERTER PART** | | | | |
| $V_{PN}$ | Supply Voltage | Applied between P – $N_U$, $N_V$, $N_W$ | 450 | V |
| $V_{PN(Surge)}$ | Supply Voltage (Surge) | Applied between P – $N_U$, $N_V$, $N_W$ | 500 | V |
| $V_{CES}$ | Collector – Emitter Voltage | | 600 | V |
| $\pm I_C$ | Each IGBT Collector Current | $T_C$ = 25°C, $T_J$ < 150°C | 15 | A |
| $\pm I_{CP}$ | Each IGBT Collector Current (Peak) | $T_C$ = 25°C, $T_J$ < 150°C,<br>Under 1 ms Pulse Width (Note 4) | 30 | A |
| $P_C$ | Collector Dissipation | $T_C$ = 25°C per One Chip (Note 4) | 38 | W |
| $T_J$ | Operating Junction Temperature | | –40 ~ 150 | °C |
| **CONTROL PART** | | | | |
| $V_{DD}$ | Control Supply Voltage | Applied between $V_{DD(H)}$, $V_{DD(L)}$ – COM | 20 | V |
| $V_{BS}$ | High–Side Control Bias Voltage | Applied between $V_{B(U)}$ – $V_{S(U)}$,<br>$V_{B(V)}$ – $V_{S(V)}$, $V_{B(W)}$ – $V_{S(W)}$ | 20 | V |
| $V_{IN}$ | Input Signal Voltage | Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$,<br>$IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ – COM | –0.3 ~ $V_{DD}$ + 0.3 | V |
| $V_{FO}$ | Fault Output Supply Voltage | Applied between $V_{FO}$ – COM | –0.3 ~ $V_{DD}$ + 0.3 | V |
| $I_{FO}$ | Fault Output Current | Sink Current at $V_{FO}$ pin | 1 | mA |
| $V_{SC}$ | Current–Sensing Input Voltage | Applied between $C_{SC}$ – COM | –0.3 ~ $V_{DD}$ + 0.3 | V |
| **BOOTSTRAP DIODE PART** | | | | |
| $V_{RRM}$ | Maximum Repetitive Reverse Voltage | | 600 | V |
| $I_F$ | Forward Current | $T_C$ = 25°C, $T_J$ < 150°C | 0.5 | A |
| $I_{FP}$ | Forward Current (Peak) | $T_C$ = 25°C, $T_J$ < 150°C,<br>Under 1 ms Pulse Width (Note 4) | 2.0 | A |
| $T_J$ | Operating Junction Temperature | | –40 ~ 150 | °C |
| **TOTAL SYSTEM** | | | | |
| $V_{PN(PROT)}$ | Self–Protection Supply Voltage Limit (Short–Circuit Protection Capability) | $V_{DD}$ = $V_{BS}$ = 13.5 ~ 16.5 V, $T_J$ = 150°C,<br>Non–Repetitive, < 2 μs | 400 | V |
| $T_C$ | Module Case Operation Temperature | See Figure 1 | –40 ~ 125 | °C |
| $T_{STG}$ | Storage Temperature | | –40 ~ 125 | °C |
| $V_{ISO}$ | Isolation Voltage | 60 Hz, Sinusoidal, AC 1 Minute,<br>Connect Pins to Heat Sink Plate | 2000 | $V_{rms}$ |

**THERMAL RESISTANCE**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $R_{th(j–c)Q}$ | Junction to Case Thermal Resistance (Note 5) | Inverter IGBT Part (per 1 / 6 Module) | – | – | 3.20 | °C/W |
| $R_{th(j–c)F}$ | | Inverter FWDi Part (per 1 / 6 Module) | – | – | 4.00 | °C/W |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. These values had been made an acquisition by the calculation considered to design factor.
5. For the measurement point of case temperature ($T_C$), please refer to Figure 1.

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C, unless otherwise specified)

| Symbol | | Parameter | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| **INVERTER PART** | | | | | | | | |
| $V_{CE(SAT)}$ | | Collector – Emitter Saturation Voltage | $V_{DD}$ = $V_{BS}$ = 15 V<br>$V_{IN}$ = 5 V | $I_C$ = 15 A,<br>$T_J$ = 25°C | – | 1.60 | 2.20 | V |
| $V_F$ | | FWDi Forward Voltage | $V_{IN}$ = 0 V | $I_F$ = 15 A,<br>$T_J$ = 25°C | – | 2.00 | 2.60 | V |
| HS | $t_{ON}$ | Switching Times | $V_{PN}$ = 300 V, $V_{DD}$ = $V_{BS}$ = 15 V, $I_C$ = 15 A<br>$T_J$ = 25°C<br>$V_{IN}$ = 0 V ↔ 5 V, Inductive Load<br>(Note 6) | | 0.40 | 0.80 | 1.30 | μs |
| | $t_{C(ON)}$ | | | | – | 0.20 | 0.50 | μs |
| | $t_{OFF}$ | | | | – | 0.85 | 1.35 | μs |
| | $t_{C(OFF)}$ | | | | – | 0.25 | 0.55 | μs |
| | $t_{rr}$ | | | | – | 0.10 | – | μs |
| LS | $t_{ON}$ | | $V_{PN}$ = 300 V, $V_{DD}$ = $V_{BS}$ = 15 V, $I_C$ = 15 A<br>$T_J$ = 25°C<br>$V_{IN}$ = 0 V ↔ 5 V, Inductive Load<br>(Note 6) | | 0.45 | 0.85 | 1.35 | μs |
| | $t_{C(ON)}$ | | | | – | 0.25 | 0.55 | μs |
| | $t_{OFF}$ | | | | – | 0.90 | 1.40 | μs |
| | $t_{C(OFF)}$ | | | | – | 0.25 | 0.55 | μs |
| | $t_{rr}$ | | | | – | 0.15 | – | μs |
| $I_{CES}$ | | Collector – Emitter Leakage Current | $V_{CE}$ = $V_{CES}$ | | – | – | 1 | mA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. $t_{ON}$ and $t_{OFF}$ include the propagation delay of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching times of IGBT under the given gate driving condition internally. For the detailed information, please see Figure 3.

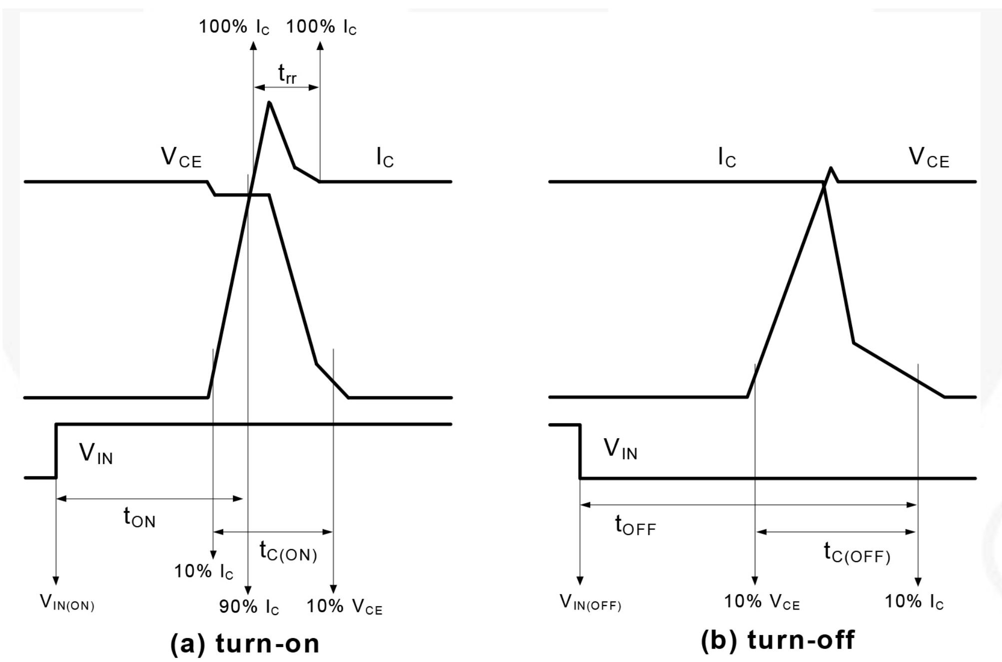



**Figure 3. Switching Time Definition**

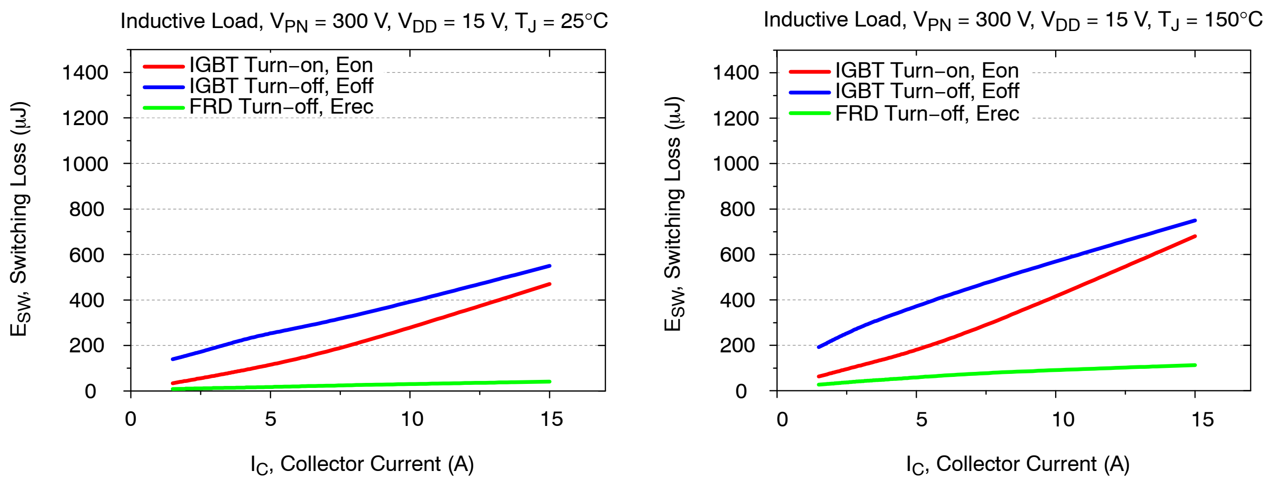



**Figure 4. Switching Loss Characteristics (Typical)**

**CONTROL PART**

| Symbol | Parameter | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{QDDH}$ | Quiescent $V_{DD}$ Supply Current | $V_{DD(H)}$ = 15 V, $IN_{(UH,VH,\ WH)}$ = 0 V | $V_{DD(H)}$ − COM | – | – | 0.10 | mA |
| $I_{QDDL}$ | | $V_{DD(L)}$ = 15 V, $IN_{(UL,VL,\ WL)}$ = 0 V | $V_{DD(L)}$ − COM | – | – | 2.65 | mA |
| $I_{PDDH}$ | Operating $V_{DD}$ Supply Current | $V_{DD(H)}$ = 15 V, $f_{PWM}$ = 20 kHz, Duty = 50%, Applied to one PWM Signal Input for High−Side | $V_{DD(H)}$ − COM | – | – | 0.15 | mA |
| $I_{PDDL}$ | | $V_{DD(L)}$ = 15V, $f_{PWM}$ = 20 kHz, Duty = 50%, Applied to one PWM Signal Input for Low−Side | $V_{DD(L)}$ − COM | – | – | 4.00 | mA |
| $I_{QBS}$ | Quiescent $V_{BS}$ Supply Current | $V_{BS}$ = 15 V, $IN_{(UH,\ VH,\ WH)}$ = 0 V | $V_{B(U)} - V_{S(U)}$, $V_{B(V)} - V_{S(V)}$, $V_{B(W)} - V_{S(W)}$ | – | – | 0.30 | mA |
| $I_{PBS}$ | Operating $V_{BS}$ Supply Current | $V_{DD}$ = $V_{BS}$ = 15 V, $f_{PWM}$ = 20 kHz, Duty = 50%, Applied to one PWM Signal Input for High−Side | $V_{B(U)} - V_{S(U)}$, $V_{B(V)} - V_{S(V)}$, $V_{B(W)} - V_{S(W)}$ | – | – | 2.00 | mA |
| $V_{FOH}$ | Fault Output Voltage | $V_{SC}$ = 0 V, $V_{FO}$ Circuit: 4.7 kΩ to 5 V Pull−up | | 4.5 | – | – | V |
| $V_{FOL}$ | | $V_{SC}$ = 1 V, $V_{FO}$ Circuit: 4.7 kΩ to 5 V Pull−up | | – | – | 0.5 | V |
| $V_{SC(ref)}$ | Short Circuit Trip Level | $V_{DD}$ = 15 V (Note 7) | $C_{SC}$ − COM | 0.45 | 0.50 | 0.55 | V |
| $UV_{DDD}$ | Supply Circuit Under− Voltage Protection | Detection Level | | 10.5 | – | 13.0 | V |
| $UV_{DDR}$ | | Reset Level | | 11.0 | – | 13.5 | V |
| $UV_{BSD}$ | | Detection Level | | 10.0 | – | 12.5 | V |
| $UV_{BSR}$ | | Reset Level | | 10.5 | – | 13.0 | V |
| $t_{FOD}$ | Fault-Out Pulse Width | | | 30 | – | – | μs |
| $V_{IN(ON)}$ | ON Threshold Voltage | Applied between $IN_{(UH,\ VH,\ WH)}$ − COM, $IN_{(UL,\ VL,\ WL)}$ − COM | | – | – | 2.6 | V |
| $V_{IN(OFF)}$ | OFF Threshold Voltage | | | 0.8 | – | – | V |
| $R_{TH}$ | Resistance of Thermistor | at $T_{TH}$ = 25°C (Note 8) | | – | 47 | – | kΩ |
| | | at $T_{TH}$ = 100°C | | – | 2.9 | – | kΩ |

7. Short−circuit current protection is functioning only at the low−sides.
8. $T_{TH}$ is the temperature of thermistor itselt. To know case temperature ($T_C$), please make the experiment considering your application.

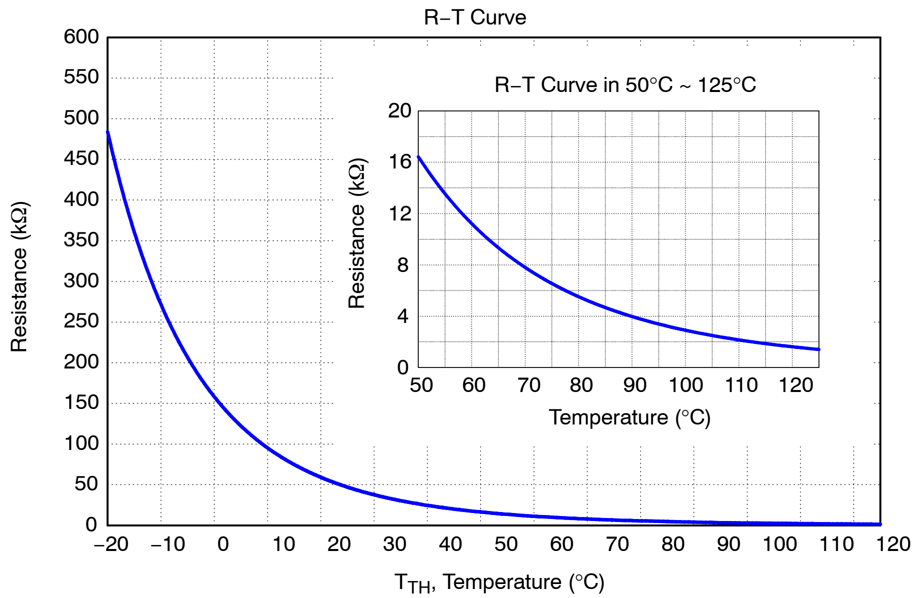
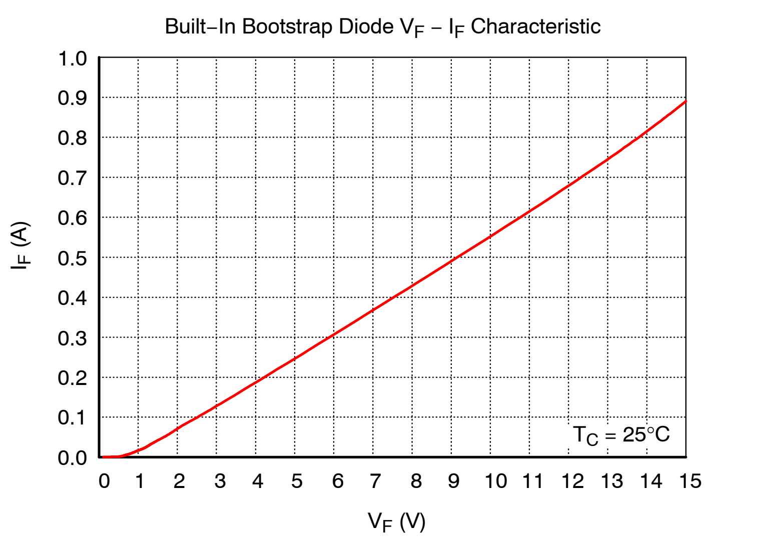



**Figure 5. R−T Curve of The Built−In Thermistor**

**BOOTSTRAP DIODE PART**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_F$ | Forward Voltage | $I_F$ = 0.1 A, $T_C$ = 25°C | – | 2.5 | – | V |
| $t_{rr}$ | Reverse−Recovery Time | $I_F$ = 0.1 A, $dI_F$ / dt = 50 A / µs, $T_J$ = 25°C | – | 80 | – | ns |




NOTE: Built−in bootstrap diode includes around 15 Ω resistance characteristic.

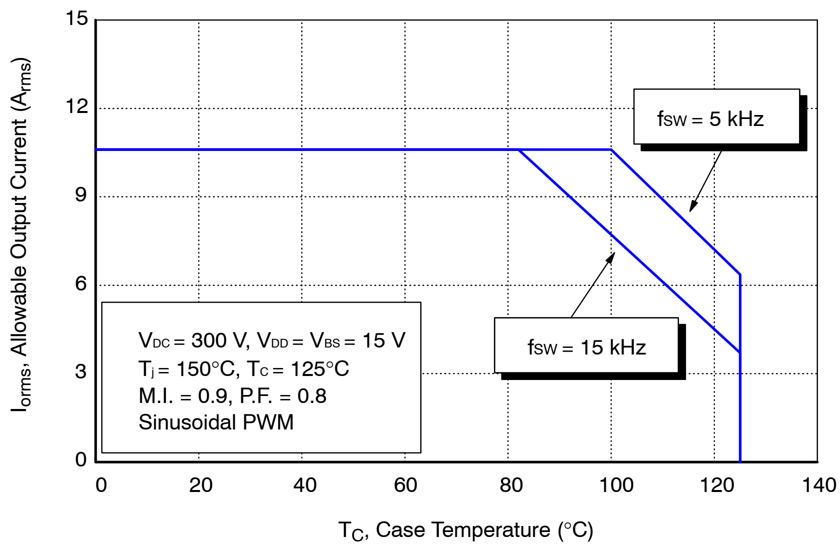
**Figure 6. Built−In Bootstrap Diode Characteristic**

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{PN}$ | Supply Voltage | Applied between P – $N_U$, $N_V$, $N_W$ | – | 300 | 400 | V |
| $V_{DD}$ | Control Supply Voltage | Applied between $V_{DD(H)}$, $V_{DD(L)}$ – COM | 13.5 | 15.0 | 16.5 | V |
| $V_{BS}$ | High–Side Bias Voltage | Applied between $V_{B(U)}$ – $V_{S(U)}$, $V_{B(V)}$ – $V_{S(V)}$, $V_{B(W)}$ – $V_{S(W)}$ | 13.0 | 15.0 | 18.5 | V |
| $dV_{DD}$ / dt, $dV_{BS}$ / dt | Control Supply Variation | | –1 | – | 1 | V / μs |
| $t_{dead}$ | Blanking Time for Preventing Arm – Short | For each input signal | 1 | – | – | μs |
| $f_{PWM}$ | PWM Input Signal | –40°C ≤ $T_C$ ≤ 125°C, –40°C ≤ $T_J$ ≤ 150°C | – | – | 20 | kHz |
| $V_{SEN}$ | Voltage for Current Sensing | Applied between $N_U$, $N_V$, $N_W$ – COM (Including Surge–Voltage) | –4 | – | 4 | V |
| $PW_{IN(ON)}$ | Minimun Input Pulse Width | $V_{DD}$ = $V_{BS}$ = 15 V, $I_C$ ≤ 15 A, Wiring Inductance between $N_{U, V, W}$ and DC Link N < 10 nH (Note 9) | 0.5 | – | – | μs |
| $PW_{IN(OFF)}$ | | | 0.5 | – | – | |
| $PW_{IN(ON)}$ | Minimun Input Pulse Width | $V_{DD}$ = $V_{BS}$ = 15 V, $I_C$ ≤ 30 A, Wiring Inductance between $N_{U, V, W}$ and DC Link N < 10 nH (Note 9) | 1.2 | – | – | μs |
| $PW_{IN(OFF)}$ | | | 1.2 | – | – | |
| $T_J$ | Junction Temperature | | –40 | – | 150 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

9. This product might not make right output response if input pulse width is less than the recommanded value.




NOTE: This allowable output current value is the reference data for the safe operation of this product. This may be different from the actual application and operating condition.

**Figure 7. Allowable Maximum Output Current**

## MECHANICAL CHARACTERISTICS AND RATINGS

| Parameter | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Device Flatness | See Figure 8 | | 0 | – | +120 | μm |
| Mounting Torque | Mounting Screw: M3<br>See Figure 9 | Recommended 0.7 N/m | 0.6 | 0.7 | 0.8 | N/m |
| | | Recommended 7.1 kg/cm | 6.2 | 7.1 | 8.1 | kg/cm |
| Weight | | | – | 11.00 | – | g |

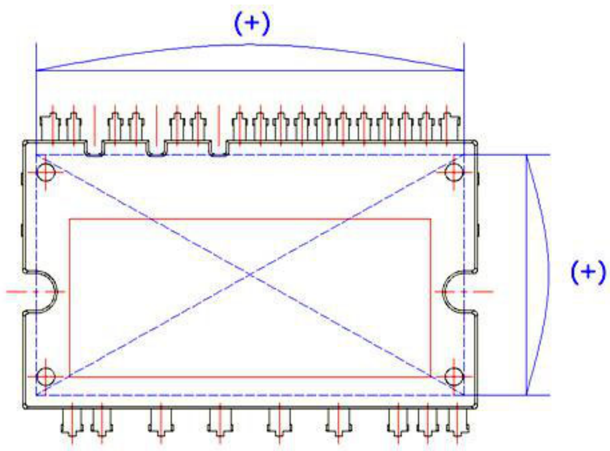



**Figure 8. Flatness Measurement Position**

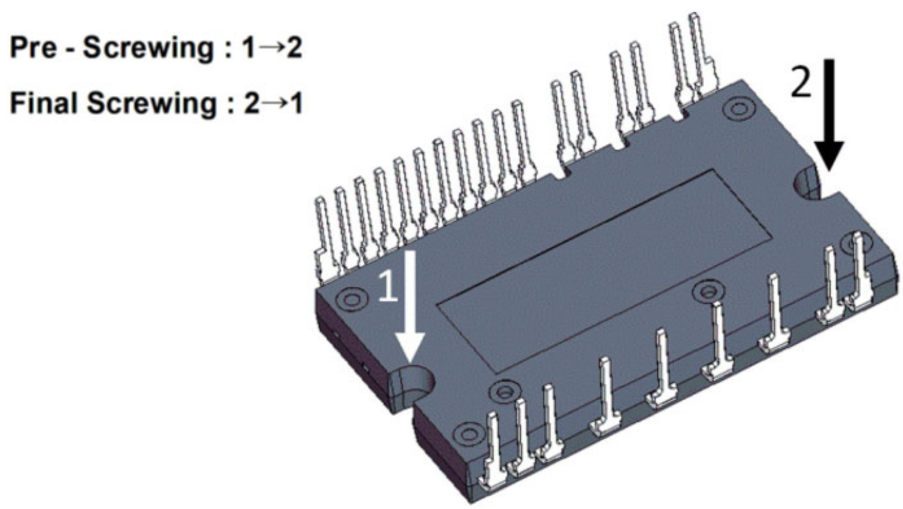
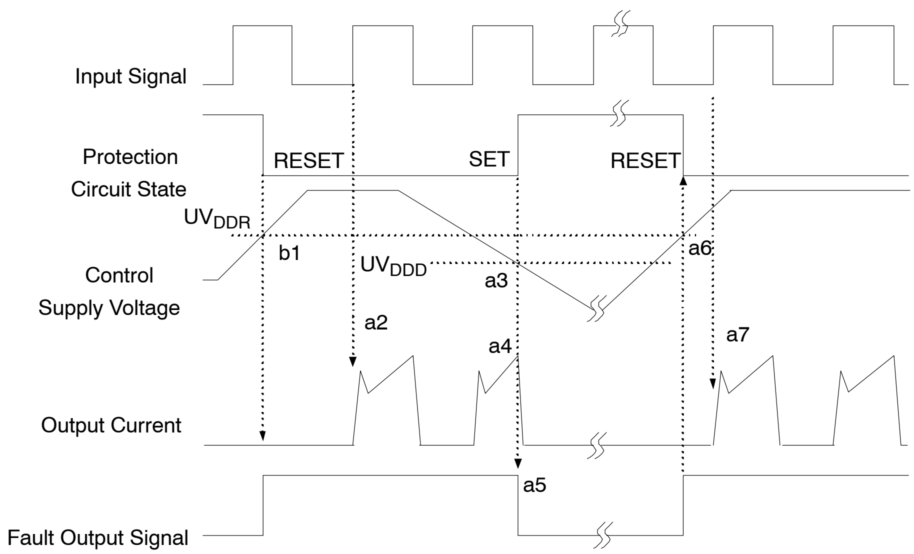



**Figure 9. Mounting Screws Torque Order**

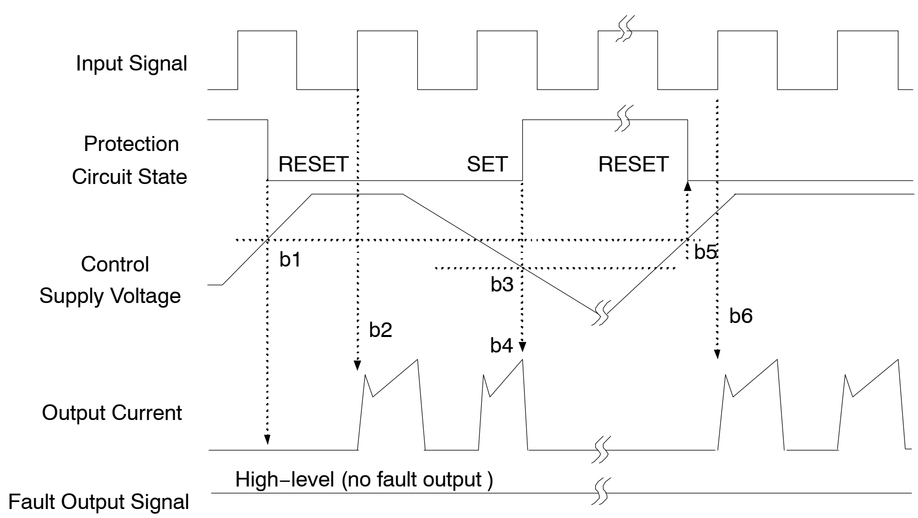
NOTES:
10. Do not make over torque when mounting screws. Much mounting torque may cause ceramic cracks, as well as bolts and Al heat−sink destruction.
11. Avoid one−sided tightening stress. Figure 9 shows the recommended torque order for the mounting screws. Uneven mounting can cause the ceramic substrate damaged. The pre−screwing torque is set to 20 ~ 30% of maximum torque rating.

### Time Charts of Protective Function



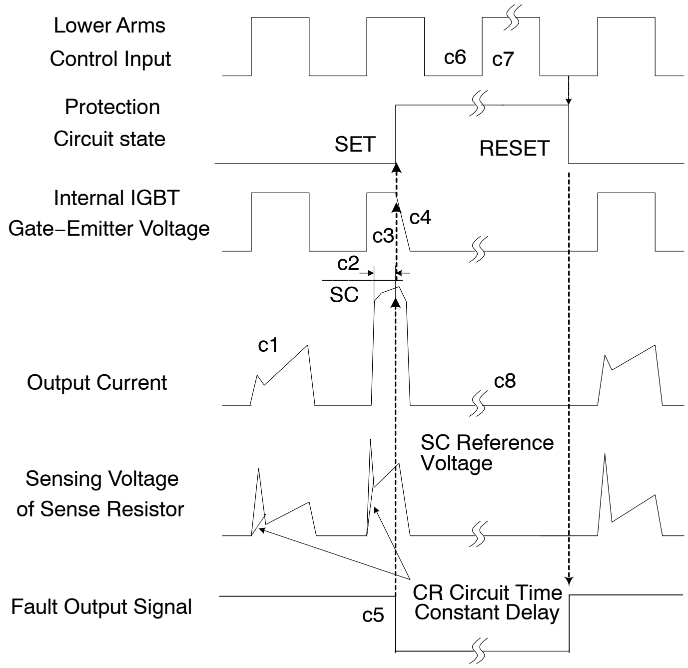

a1 : Control supply voltage rises: after the voltage rises $UV_{DDR}$, the circuits start to operate when the next input is applied.
a2 : Normal operation: IGBT ON and carrying current.
a3 : Under−voltage detection ($UV_{DDD}$).
a4 : IGBT OFF in spite of control input condition.
a5 : Fault output operation starts with a fixed pulse width.
a6 : Under−voltage reset ($UV_{DDR}$).
a7 : Normal operation: IGBT ON and carrying current by triggering next signal from LOW to HIGH.

**Figure 10. Under−Voltage Protection (Low−Side)**




b1 : Control supply voltage rises: after the voltage reaches $UV_{BSR}$, the circuits start to operate when the next input is applied.
b2 : Normal operation: IGBT ON and carrying current.
b3 : Under−voltage detection ($UV_{BSD}$).
b4 : IGBT OFF in spite of control input condition, but there is no fault output signal.
b5 : Under−voltage reset ($UV_{BSR}$).
b6 : Normal operation: IGBT ON and carrying current by triggering next signal from LOW to HIGH.

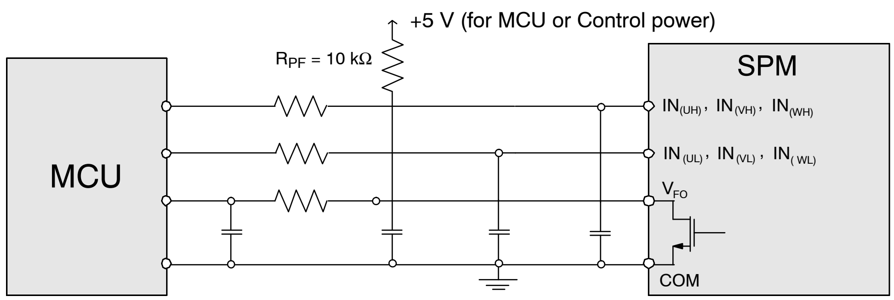
**Figure 11. Under−Voltage Protection (High−Side)**




(with the external sense resistance and RC filter connection)
c1 : Normal operation: IGBT ON and carrying current.
c2 : Short−circuit current detection (SC trigger).
c3 : All low−side IGBTs gate are hard interrupted.
c4 : All low−side IGBTs turn OFF.
c5 : Fault output operation starts with a fixed pulse width according to the condition of the external capacitor $C_{FOD}$.
c6 : Input HIGH: IGBT ON state, but during the active period of fault output, the IGBT doesn't turn ON.
c7 : Fault output operation finishes, but IGBT doesn't turn on until triggering the next signal from LOW to HIGH.
c8 : Normal operation: IGBT ON and carrying current.

**Figure 12. Short−Circuit Current Protection (Low−Side Operation only)**

### Input/Output Interface Circuit




NOTE: RC coupling at each input might change depending on the PWM control scheme used in the application and the wiring impedance of the application's printed circuit board. The input signal section of the Motion SPM 45 product integrates 5 kΩ(typ.) pull−down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.

**Figure 13. Recommended MCU I/O Interface Circuit**

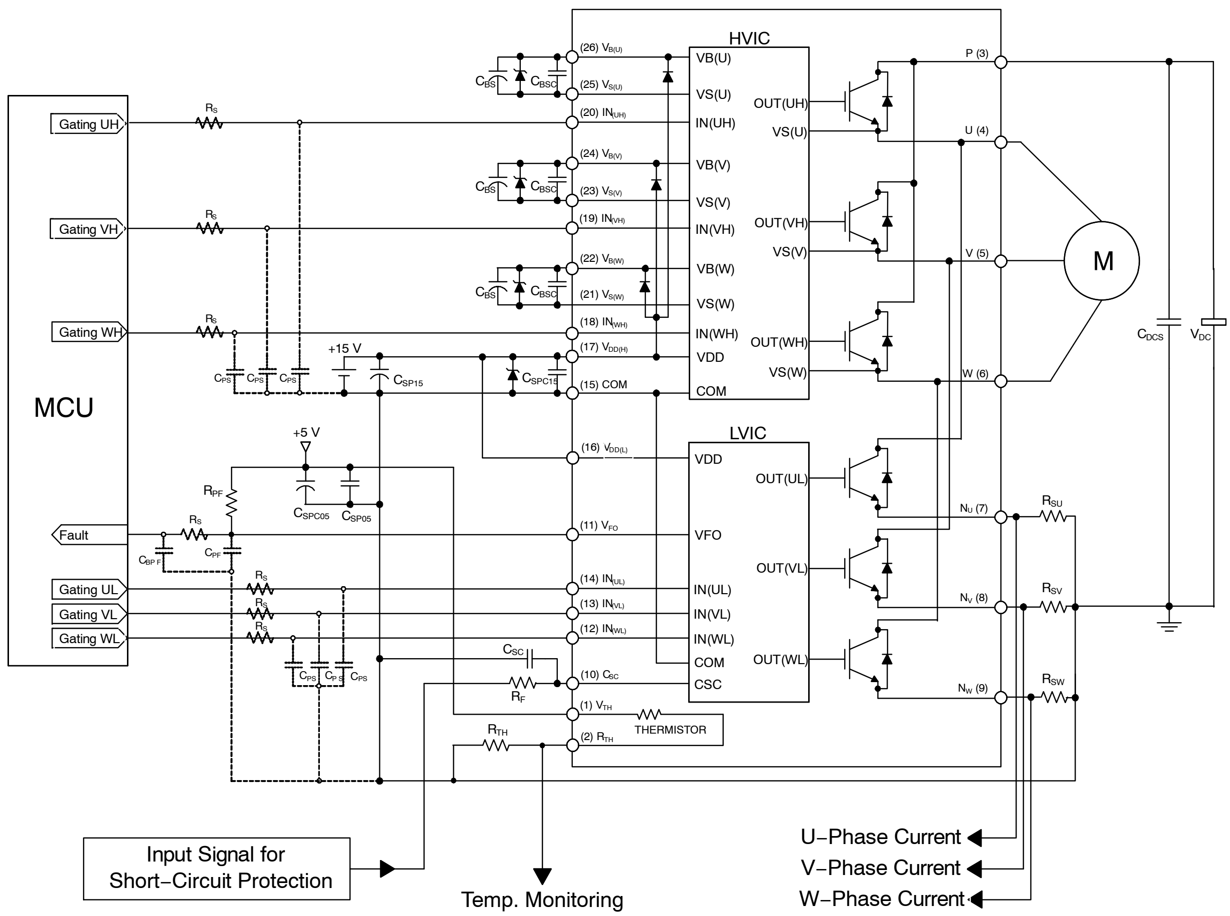



**Figure 14. Typical Application Circuit**

NOTES:

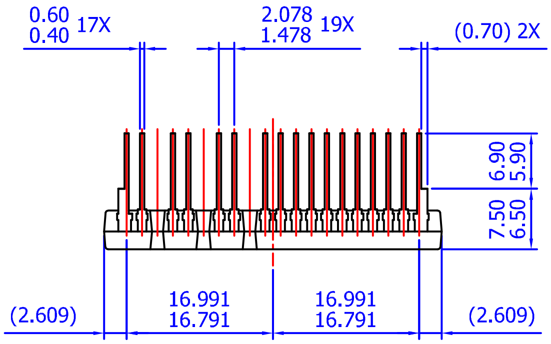
12. To avoid malfunction, the wiring of each input should be as short as possible (less than 2 − 3 cm).
13. $V_{FO}$ output is an open−drain type. This signal line should be pulled up to the positive side of the MCU or control power supply with a resistor that makes $I_{FO}$ up to 1 mA.
14. $C_{SP15}$ of around seven times larger than bootstrap capacitor $C_{BS}$ is recommended.
15. Input signal is active−HIGH type. There is a 5 kΩ resistor inside the IC to pull down each input signal line to GND. RC coupling circuits is recommanded for the prevention of input signal oscillation. $R_SC_{PS}$ time constant should be selected in the range 50 ~ 150 ns (recommended $R_S$ = 100 Ω, $C_{PS}$ = 1 nF).
16. To prevent errors of the protection function, the wiring around RF and CSC should be as short as possible.
17. In the short−circuit protection circuit, please select the $R_FC_{SC}$ time constant in the range 1.5 ~ 2 μs. Do enough evaluaiton on the real system because short−circuit protection time may vary wiring pattern layout and value of the $R_FC_{SC}$ time constant.
18. The connection between control GND line and power GND line which includes the $N_U$, $N_V$, $N_W$ must be connected to only one point. Please do not connect the control GND to the power GND by the broad pattern. Also, the wiring distance between control GND and power GND should be as short as possible.
19. Each capacitor should be mounted as close to the pins of the Motion SPM 45 product as possible.
20. To prevent surge destruction, the wiring between the smoothing capacitor and the P & GND pins should be as short as possible. The use of a high−frequency non−inductive capacitor of around 0.1 ~ 0.22 μF between the P and GND pins is recommended.
21. Relays are used in almost every systems of electrical equipment in home appliances. In these cases, there should be sufficient distance between the MCU and the relays.
22. The zener diode or transient voltage suppressor should be adopted for the protection of ICs from the surge destruction between each pair of control supply terminals (recommanded zener diode is 22 V / 1 W, which has the lower zener impedance characteristic than about 15 Ω).
23. Please choose the electrolytic capacitor with good temperature characteristic in $C_{BS}$. Also, choose 0.1 ~ 0.2 μF R−category ceramic capacitors with good temperature and frequency characteristics in $C_{BSC}$.

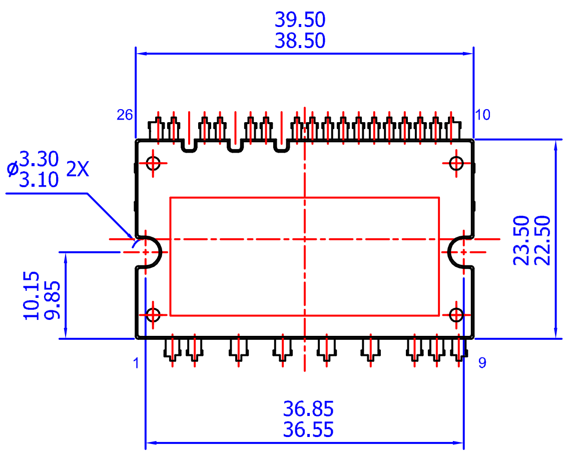
## PACKAGE MARKING AND ORDERING INFORMATION

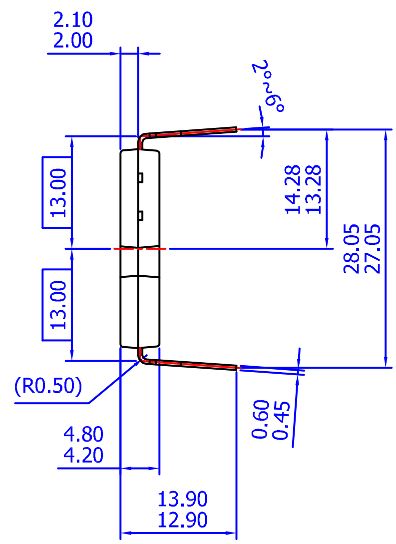
| Device | Device Marking | Package | Shipping |
|---|---|---|---|
| FNA41560T2 | FNA41560T2 | SPMAA−C26 / 26LD, PDD STD CERAMIC TYPE, LONG LEAD DUAL FORM TYPE (Pb−Free) | 12 Units / Rail |

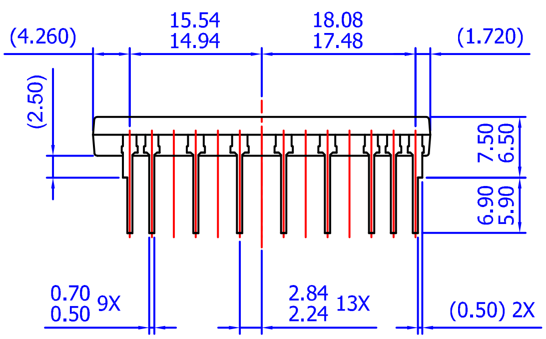
**SPMAA−C26 / 26LD, PDD STD CERAMIC TYPE, LONG LEAD DUAL FORM TYPE**
CASE MODFC
ISSUE O

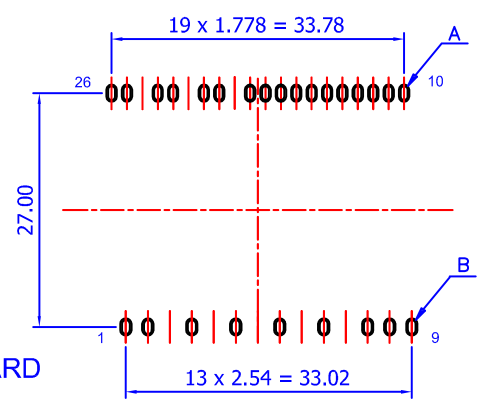
DATE 31 JAN 2017

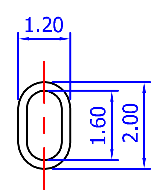


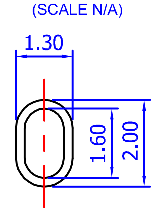




DETAIL A
(SCALE N/A)




DETAIL B
(SCALE N/A)

LAND PATTERN RECOMMENDATIONS

NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD
B) ALL DIMENSIONS ARE IN MILLIMETERS
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D) ( ) IS REFERENCE

| | | |
|---|---|---|
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| **DESCRIPTION:** | **SPMAA−C26 / 26LD, PDD STD CERAMIC TYPE, LONG LEAD DUAL** | **PAGE 1 OF 1** |

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
**onsemi Website:** www.onsemi.com

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