Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor’s system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.
FMS6144A
Four-Channel, 6th-Order SD VoltagePlus™ Video Filter Driver

Features
- Four-Channel 6th-Order 8MHz (SD) Filter
- Drives Single, AC- or DC-Coupled Video Loads (150Ω)
- Transparent Input Clamping
- Supply Range: 3.3V to 5.0V
- AC- or DC-Coupled Inputs and Outputs
- Robust 9kV ESD Protection
- Lead-Free TSSOP 14-Pin Package

Description
The FMS6144A VoltagePlus™ video filter is intended to replace passive LC filters and drivers with a cost-effective integrated device. Four 6th-order filters provide improved image quality compared to typical 2nd and 3rd order passive solutions.

The FMS6144A may be directly driven by a DC-coupled DAC output or an AC-coupled signal. Internal diode clamps and bias circuitry may be used if AC-coupled inputs are required (see the Applications section for details).

The outputs can drive AC- or DC-coupled single (150Ω) or dual (75Ω) video loads. DC coupling the outputs removes the need for large output coupling capacitors. The input DC levels are offset approximately +280mV at the output (see the Applications section for details).

Related Applications Notes
AN-6024 – FMS6xxx Product Series Understanding Analog Video Signal Clamps, Bias, DC Restore, and AC or DC coupling Methods
AN-6041 – PCB Layout Considerations for Video Filter / Drivers

Figure 1. Block Diagram

Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Operating Temperature Range</th>
<th>Package</th>
<th>Packing Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>FMS6144AMTC14X</td>
<td>-40°C to +85°C</td>
<td>14-Lead TSSOP</td>
<td>2500 per Reel</td>
</tr>
</tbody>
</table>
Pin Configuration

Figure 2. 14-Lead TSSOP (Top View)

Pin Definitions

<table>
<thead>
<tr>
<th>Pin#</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>IN1</td>
<td>Input</td>
<td>Video Input Channel 1</td>
</tr>
<tr>
<td>2</td>
<td>IN2</td>
<td>Input</td>
<td>Video Input Channel 2</td>
</tr>
<tr>
<td>3</td>
<td>IN3</td>
<td>Input</td>
<td>Video Input Channel 3</td>
</tr>
<tr>
<td>4</td>
<td>IN4</td>
<td>Input</td>
<td>Video Input Channel 4</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>Input</td>
<td>Device Ground Connection</td>
</tr>
<tr>
<td>6</td>
<td>NA</td>
<td>NA</td>
<td>No Connection</td>
</tr>
<tr>
<td>7</td>
<td>NA</td>
<td>NA</td>
<td>No Connection</td>
</tr>
<tr>
<td>8</td>
<td>NA</td>
<td>NA</td>
<td>No Connection</td>
</tr>
<tr>
<td>9</td>
<td>NA</td>
<td>NA</td>
<td>No Connection</td>
</tr>
<tr>
<td>10</td>
<td>Vcc</td>
<td>Input</td>
<td>Positive Power Supply</td>
</tr>
<tr>
<td>11</td>
<td>OUT4</td>
<td>Output</td>
<td>Filtered Output Channel 4</td>
</tr>
<tr>
<td>12</td>
<td>OUT3</td>
<td>Output</td>
<td>Filtered Output Channel 3</td>
</tr>
<tr>
<td>13</td>
<td>OUT2</td>
<td>Output</td>
<td>Filtered Output Channel 2</td>
</tr>
<tr>
<td>14</td>
<td>OUT1</td>
<td>Output</td>
<td>Filtered Output Channel 1</td>
</tr>
</tbody>
</table>
**Absolute Maximum Ratings**

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>DC Supply Voltage</td>
<td>-0.3</td>
<td>6.0</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IO}$</td>
<td>Analog and Digital I/O</td>
<td>-0.3</td>
<td>$V_{CC}+0.3$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>Maximum Output Current, Do Not Exceed</td>
<td></td>
<td>50</td>
<td>mA</td>
</tr>
</tbody>
</table>

**Electrostatic Discharge Information**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD</td>
<td>Human Body Model, JESD22-A114</td>
<td>9</td>
<td>kV</td>
</tr>
<tr>
<td></td>
<td>Charged Device Model, JESD22-C101</td>
<td>2</td>
<td></td>
</tr>
</tbody>
</table>

**Reliability Information**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_J$</td>
<td>Junction Temperature</td>
<td></td>
<td>+150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>$T_{STG}$</td>
<td>Storage Temperature Range</td>
<td>-65</td>
<td>+150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>$T_L$</td>
<td>Lead Temperature (Soldering, 10 Seconds)</td>
<td></td>
<td>+300</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>$\Theta_{JA}$</td>
<td>Thermal Resistance, JEDEC Standard, Multilayer Test Boards, Still Air</td>
<td>90</td>
<td></td>
<td>°C/W</td>
<td></td>
</tr>
</tbody>
</table>

**Recommended Operating Conditions**

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_A$</td>
<td>Operating Temperature Range</td>
<td>-40</td>
<td>+85</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>$V_{CC}$</td>
<td>Supply Voltage Range</td>
<td>3.14</td>
<td>3.30</td>
<td>5.25</td>
<td>V</td>
</tr>
</tbody>
</table>
## DC Electrical Characteristics

\( T_A = 25^\circ C, \ V_{CC} = 3.3V, \ R_S = 37.5\Omega, \) all inputs are AC-coupled with 0.1µF, and all outputs are AC coupled with 220µF into 150Ω load; unless otherwise noted.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_C )</td>
<td>Supply Voltage Range</td>
<td>( V_S ) Range</td>
<td>3.14</td>
<td>3.30</td>
<td>5.25</td>
<td>V</td>
</tr>
<tr>
<td>( I_{CC} )</td>
<td>Quiescent Supply Current((1))</td>
<td>( V_S = +3.3V), No Load</td>
<td>21</td>
<td>24</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = +5.0V), No Load</td>
<td>25</td>
<td>29</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{IN} )</td>
<td>Video Input Voltage Range</td>
<td></td>
<td>1.4</td>
<td>( V_{pp} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
<td>DC (all Channels)</td>
<td>-65</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
</tbody>
</table>

**Note:**
1. 100% tested at \( T_A = 25^\circ C \)

## AC Electrical Characteristics

\( T_A = 25^\circ C, \ V_{CC} = 3.3V, \ R_S = 37.5\Omega, \) all inputs are AC-coupled with 0.1µF, and all outputs are AC coupled with 220µF into 150Ω load, unless otherwise noted.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( AV )</td>
<td>Channel Gain((2))</td>
<td>Active Video Input Range = 1Vpp</td>
<td>5.8</td>
<td>6.0</td>
<td>6.2</td>
<td>dB</td>
</tr>
<tr>
<td>( BW_{0.1dB} )</td>
<td>±0.1dB Bandwidth</td>
<td>( R_{SOURCE}=75\Omega, \ R_L=150\Omega )</td>
<td>5</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>( BW_{1.0dB} )</td>
<td>-1.0 dB Bandwidth</td>
<td>( R_{SOURCE}=75\Omega, \ R_L=150\Omega )</td>
<td>7</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>( BW_{3.0dB} )</td>
<td>-3.0 dB Bandwidth</td>
<td>( R_{SOURCE}=75\Omega, \ R_L=150\Omega )</td>
<td>8</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>( Att_{27MHz} )</td>
<td>Normalized Stopband Attenuation((2))</td>
<td>( R_{SOURCE}=75\Omega, \ f=27MHz )</td>
<td>45</td>
<td>60</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>( DG )</td>
<td>Differential Gain - NTSC/PAL</td>
<td>Active Video Input Range = 1Vpp</td>
<td>0.6</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>( DP )</td>
<td>Differential Phase - NTSC/PAL</td>
<td>Active Video Input Range = 1Vpp</td>
<td>0.6</td>
<td></td>
<td></td>
<td>°</td>
</tr>
<tr>
<td>( THD )</td>
<td>Total Harmonic Distortion</td>
<td>( f=1.00MHz; \ V_{OUT}=1.4Vpp )</td>
<td>0.2</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>( X_{talk} )</td>
<td>Crosstalk (Channel to Channel)</td>
<td>( f=1.00MHz; \ V_{OUT}=1.4Vpp )</td>
<td>-65</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>SNR</td>
<td>Peak Signal to RMS Noise</td>
<td>NTC-7 Weighting: 100kHz to 4.2MHz</td>
<td>74</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>( T_{pd} )</td>
<td>Propagation Delay</td>
<td>Delay from Input to Output; 100KHz to 4.5MHz</td>
<td>90</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>CLG</td>
<td>Chroma-Luma Gain((2))</td>
<td>400Khz to 3.58Mhz</td>
<td>95</td>
<td>100</td>
<td>105</td>
<td>%</td>
</tr>
<tr>
<td>CLD</td>
<td>Chroma-Luma Delay</td>
<td>400Khz to 3.58Mhz</td>
<td>7.5</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

**Note:**
2. 100% tested at \( T_A = 25^\circ C \)
Typical Performance Characteristics

Unless otherwise noted, $T_A = 25^\circ C$, $V_{CC} = 2.7V$, $R_S = 37.5\Omega$, and AC-coupled output into $150\Omega$ load.

**Figure 3.** Delay vs. Frequency

**Figure 4.** Frequency Response
Typical Performance Characteristics

Unless otherwise noted, $T_A = 25^\circ C$, $V_{CC} = 2.7V$, $R_S = 37.5\Omega$, and AC-coupled output into 150$\Omega$ load.

**Figure 5. Frequency Response Flatness**

**Figure 6. Noise vs. Frequency**
**Typical Performance Characteristics**

Unless otherwise noted, $T_A = 25°C$, $V_{CC} = 2.7V$, $R_S = 37.5Ω$, and AC-coupled output into $150Ω$ load.

**Figure 9. Differential Gain**

<table>
<thead>
<tr>
<th>Differential Gain (%)</th>
<th>min</th>
<th>max</th>
<th>p-p max</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0.00</td>
<td>0.02</td>
<td>-0.13</td>
</tr>
<tr>
<td></td>
<td>0.00</td>
<td>0.02</td>
<td>-0.22</td>
</tr>
<tr>
<td></td>
<td>-0.31</td>
<td>-0.31</td>
<td>-0.31</td>
</tr>
</tbody>
</table>

**Figure 10. Differential Phase**

<table>
<thead>
<tr>
<th>Differential Phase (deg)</th>
<th>min</th>
<th>max</th>
<th>pk-pk</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0.00</td>
<td>0.03</td>
<td>0.17</td>
</tr>
<tr>
<td></td>
<td>0.40</td>
<td>0.50</td>
<td>0.52</td>
</tr>
</tbody>
</table>

Average 128 → 128 Reference(1) is not defined

**Figure 11. Chroma / Luma Gain & Delay**

Chroma Gain = 100.1 %
Chroma Delay = 4.4 n sec

Chroma Gain (%)

Chroma Delays (n sec)
Applications Information

The following circuit may be used for direct DC-coupled drive by DACs with an output voltage range of 0V to 1.4V_{pp}.

Figure 12. Typical Application
Application Information

Application Circuits
The FMS6144A VoltagePlus™ video filter provides 6dB gain from input to output. In addition, the input is slightly offset to optimize the output driver performance. The offset is held to the minimum required value to decrease the standing DC current into the load. Typical voltage levels are shown in Figure 13:

\[
\begin{align*}
1.0 & \rightarrow 1.02V \\
0.65 & \rightarrow 0.67V \\
0.3 & \rightarrow 0.32V \\
0.0 & \rightarrow 0.02V \\
2.28V & \\
1.56V & \\
0.88V & \\
0.28V & \\
0.85V & \\
0.5V & \\
0.15V & \\
1.98V & \\
1.28V & \\
0.58V & \\
\end{align*}
\]

There is a 280mV offset from the DC input level to the DC output level. \( V_{OUT} = 2 \times V_{IN} + 280mV \).

\[
\begin{align*}
V_{IN} & \\
V_{OUT} & \\
\end{align*}
\]

Figure 13. Typical Voltage Levels

The FMS6144A provides an internal diode clamp to support AC-coupled input signals. If the input signal does not go below ground, the input clamp does not operate. This allows DAC outputs to directly drive the FMS6144A without an AC-coupling capacitor. When the input is AC coupled, the diode clamp sets the sync tip (or lowest voltage) just below ground. The worst-case sync tip compression due to the clamp cannot exceed 7mV. The input level set by the clamp, combined with the internal DC offset, keeps the output within its acceptable range.

For symmetric signals like Chroma, U, V, Pb, and Pr; the average DC bias is fairly constant and the inputs can be AC-coupled with the addition of a pull-up resistor to set the DC input voltage. DAC outputs can also drive these same signals without the AC coupling capacitor. A conceptual illustration of the input clamp circuit is shown in Figure 14.

I/O Configurations
For a DC-coupled DAC drive with DC-coupled outputs, use the configuration in Figure 15.

Figure 14. Input Clamp Circuit

Figure 15. DC-Coupled Inputs and Outputs

Alternatively, if the DAC’s average DC output level causes the signal to exceed the range of 0V to 1.4V, it can be AC coupled as follows:

Figure 16. AC-Coupled Inputs, DC-Coupled Outputs

When FMS6144A is driven by an unknown external source or a SCART switch with its own clamping circuitry, the inputs should be AC coupled like Figure 17.

Figure 17. SCART with DC-Coupled Outputs
The same method can be used for biased signals, with the addition of a pull-up resistor to make sure the clamp never operates. The internal pull-down resistance is 800Ω ±20%, so the external resistance should be 7.5MΩ to set the DC level to 500mV.

External video source must be AC coupled

\[ \text{LCVF Bias Input} \]

\[ \begin{align*}
\text{0.1µ} & \quad \text{7.5MΩ} \\
\text{75Ω} & \quad \text{500mV +1-350mV} \\
\end{align*} \]

Figure 18. Biased SCART with DC-Coupled Outputs

The same circuits can be used with AC-coupled outputs if desired.

\[ \begin{align*}
\text{0V - 1.4V} & \quad \text{220µF} \\
\text{75Ω} & \quad \text{LCVF Clamp Active} \\
\text{75Ω} & \quad \text{DAC Output} \\
\text{0.1µ} & \quad \text{LCVF Clamp Active} \\
\text{75Ω} & \quad \text{DAC Output} \\
\end{align*} \]

Figure 19. DC-Coupled Inputs, AC-Coupled Outputs

Figure 20. AC-Coupled Inputs and Outputs

![Diagram of video filter driver with AC-coupled inputs and outputs](image)

Power Dissipation

The output drive configuration must be considered when calculating overall power dissipation. Care must be taken not to exceed the maximum die junction temperature. The following example can be used to calculate the power dissipation and internal temperature rise.

\[ T_J = T_A + P_D \cdot \theta_{JA} \] (1)

where:

\[ P_D = P_{CL1} + P_{CL2} + P_{CL3} \] (2)

and

\[ P_{CLX} = V_{CC} \cdot I_{CH} - \left( V_O^2 / R_L \right) \] (3)

where:

\[ V_O = 2V_{IN} + 0.280V \] (4)

\[ I_{CH} = (I_{CC} / 3) + (V_O / R_L) \] (5)

\[ V_{IN} = \text{RMS value of input signal} \]

\[ I_{CC} = 19mA \]

\[ V_{CC} = 3.3V. \]

\[ R_L = \text{channel load resistance} \]

Board layout can also affect thermal characteristics. Refer to the Layout Considerations section for details.

The FMS6144A is specified to operate with output currents typically less than 50mA, more than sufficient for a dual (75Ω) video load. Internal amplifiers are current limited to a maximum of 100mA and should withstand brief-duration short-circuit conditions. This capability is not guaranteed.

NOTE: The video tilt or line time distortion is dominated by the AC-coupling capacitor. The value may need to be increased beyond 220µF to obtain satisfactory operation in some applications.
Layout Considerations

General layout and supply bypassing play a major role in high-frequency performance and thermal characteristics. Fairchild offers a four-layer board with full power and ground planes board to guide layout and aid device evaluation. The demo board is a four-layer board with full power and ground planes. Following this layout configuration provides optimum performance and thermal characteristics for the device. For best results, follow the steps and recommended routing rules below.

Recommended Routing / Layout Rules

- Do not run analog and digital signals in parallel.
- Use separate analog and digital power planes to supply power.
- Traces should run on top of the ground plane at all times.
- No trace should run over ground/power splits.
- Avoid routing at 90-degree angles.
- Minimize clock and video data trace length differences.
- Include 10μF and 0.1μF ceramic power supply bypass capacitors.
- Place the 0.1μF capacitor within 2.54mm (0.1in) of the device power pin.
- Place the 10μF capacitor within 19.05mm (0.75in) of the device power pin.
- For multi-layer boards, use a large ground plane to help dissipate heat.
- For two-layer boards, use a ground plane that extends beyond the device body at least 12.7mm (0.5in) on all sides. Include a metal paddle under the device on the top layer.
- Minimize all trace lengths to reduce series inductance.

Output Considerations

The outputs are DC offset from the input by 150mV therefore $V_{OUT} = 2 \cdot V_{IN} \text{ DC} + 150\text{mV}$. This offset is required for optimal performance from the output driver and is held at the minimum value to decrease the standing DC current into the load. Since the FMS6144A has a 2x (6dB) gain, the output is typically connected via a 75Ω series back-matching resistor followed by the 75Ω video cable. Because of the inherent divide by two of this configuration, the blanking level at the load of the video signal is always less than 1V. When AC-coupling the output, ensure that the coupling capacitor passes the lowest frequency content in the video signal and that line time distortion (video tilt) is kept as low as possible.

The selection of the coupling capacitor is a function of the subsequent circuit input impedance and the leakage current of the input being driven. To obtain the highest quality output video signal, the series termination resistor must be placed as close to the device output pin as possible. This greatly reduces the parasitic capacitance and inductance effect on the output driver. The distance from the device pin to the series termination resistor should be no greater than 2.54mm (0.1in).

Figure 22. Termination Resistor Placement

Thermal Considerations

Since the interior of most systems, such as set-top boxes, TVs, and DVD players; are at +70ºC; consideration must be given to providing an adequate heat sink for the device package for maximum heat dissipation. When designing a system board, determine how much power each device dissipates. Ensure that devices of high power are not placed in the same location, such as directly above (top plane) or below (bottom plane) each other, on the PCB.

PCB Thermal Layout Considerations

- Understand the system power requirements and environmental conditions.
- Maximize thermal performance of the PCB.
- Consider using 70μm of copper for high-power designs.
- Make the PCB as thin as possible by reducing FR4 thickness.
- Use vias in power pad to tie adjacent layers together.
- Remember that baseline temperature is a function of board area, not copper thickness.
- Modeling techniques provide a first-order approximation.
Physical Dimensions

Figure 23. 14-Lead TSSOP

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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CoreFLUX™
CorePOWER™
CROSSVOX™
CTL™
Current Transfer Logic™
DEUXPEX™
Dual Cool™
EcoSPARK™
EfficientMax™
ESPRIT™
Fairchild®
Fairchild Semiconductor®
FACT®
FAC™
FastCore™
FETBench™
FlashWriter™
FPS™
FFPS™
FFSM™
Global Power Resource™
Green FPS™
Green FPS® e-Series™
Graex™
GTO®
IntelliMAX™
ISOPLANAR™
Making Small Speakers Sound Louder and Better™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroFET®
MicroPair™
MillerDrive™
MoboMax™
Motion-SFET™
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OptiHi™
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OPTOPLANAR™
FDP-SMP™
Power-SMP™
PowerTrench™
PowerUPS™
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
Saving our world, 1myWatt at a time™
SignalMode™
SmartMax™
SMART START™
SMP™
STEALTH™
SuperFET™
SuperSOT-M®
SuperSOT™K
SuperSOT™K-8
SuperSOT™8
SuperMOS™
SyncFET™
SyncLink™
SYSTEM GENERAL™
Wavelink™
The Power Franchise®
Power franchises
TinyBoost™
TinyBuck™
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TinyLogic™
TinyOCPT™
TinyPower™
TinyPWM™
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<th>Datasheet Identification</th>
<th>Product Status</th>
<th>Definition</th>
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<td>Advance Information</td>
<td>Formative / In Design</td>
<td>Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.</td>
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<td>Preliminary</td>
<td>First Production</td>
<td>Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.</td>
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