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## FIN1104

### LVDS 4 Port High Speed Repeater

#### General Description

This 4 port repeater is designed for high speed interconnects utilizing Low Voltage Differential Signaling (LVDS) technology. The FIN1104 accepts and outputs LVDS levels with a typical differential output swing of 330 mV which provides low EMI at ultra low power dissipation even at high frequencies. The FIN1104 provides a  $V_{BB}$  reference for AC coupling on the inputs. In addition the FIN1104 can directly accept LVPECL, HSTL, and SSTL-2 for translation to LVDS.

#### Features

- Greater than 800 Mbps data rate
- 3.3V power supply operation
- 3.5 ps maximum random jitter and 135 ps maximum deterministic jitter
- Wide rail-to-rail common mode range
- LVDS receiver inputs accept LVPECL, HSTL, and SSTL-2 directly
- Ultra low power consumption
- 20 ps typical channel-to-channel skew
- Power off protection
- > 7.5 kV HBM ESD Protection
- Meets or exceeds the TIA/EIA-644-A LVDS standard
- Available in space saving 24-Lead TSSOP package
- Open circuit fail safe protection
- $V_{BB}$  reference output

#### Ordering Code:

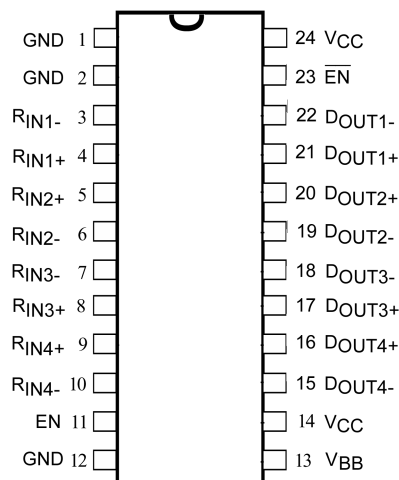
| Order Number | Package Number | Package Description                                                         |
|--------------|----------------|-----------------------------------------------------------------------------|
| FIN1104MTC   | MTC24          | 24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

#### Pin Descriptions

| Pin Name                                                 | Description                                 |
|----------------------------------------------------------|---------------------------------------------|
| $R_{IN1+}$ , $R_{IN2+}$ ,<br>$R_{IN3+}$ , $R_{IN4+}$     | Non-inverting LVDS Input                    |
| $R_{IN1-}$ , $R_{IN2-}$ ,<br>$R_{IN3-}$ , $R_{IN4-}$     | Inverting LVDS Input                        |
| $D_{OUT1+}$ , $D_{OUT2+}$ ,<br>$D_{OUT3+}$ , $D_{OUT4+}$ | Non-inverting Driver Output                 |
| $D_{OUT1-}$ , $D_{OUT2-}$ ,<br>$D_{OUT3-}$ , $D_{OUT4-}$ | Inverting Driver Output                     |
| EN                                                       | Driver Enable Pin for All Output            |
| $\overline{EN}$                                          | Inverting Driver Enable Pin for all Outputs |
| $V_{CC}$                                                 | Power Supply                                |
| GND                                                      | Ground                                      |
| $V_{BB}$                                                 | Reference Voltage Output                    |

#### Connection Diagram



## Function Table

| Inputs |                        |                  |                  | Outputs           |                   |
|--------|------------------------|------------------|------------------|-------------------|-------------------|
| EN     | $\overline{\text{EN}}$ | D <sub>IN+</sub> | D <sub>IN-</sub> | D <sub>OUT+</sub> | D <sub>OUT-</sub> |
| H      | L                      | H                | L                | H                 | L                 |
| H      | L                      | L                | H                | L                 | H                 |
| H      | L                      | Fail Safe Case   |                  | H                 | L                 |
| X      | H                      | X                | X                | Z                 | Z                 |
| L      | X                      | X                | X                | Z                 | Z                 |

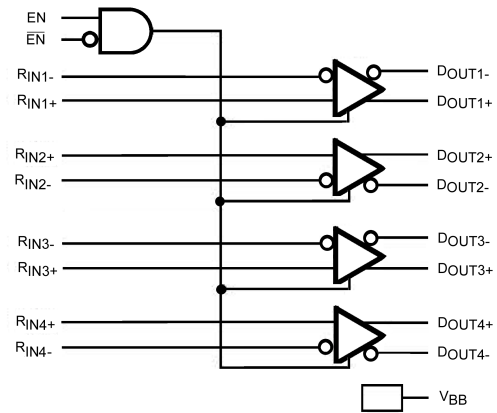
H = HIGH Logic Level

L = LOW Logic Level

X = Don't Care

Z = High Impedance

## Functional Diagram



**Absolute Maximum Ratings**(Note 1)

|                                                       |                  |
|-------------------------------------------------------|------------------|
| Supply Voltage ( $V_{CC}$ )                           | –0.5V to +4.6V   |
| LVDS DC Input Voltage ( $V_{IN}$ )                    | –0.5V to +4.6V   |
| LVDS DC Output Voltage ( $V_{OUT}$ )                  | –0.5V to +4.6V   |
| Driver Short Circuit Current ( $I_{OSD}$ )            | Continuous 10 mA |
| Storage Temperature Range ( $T_{STG}$ )               | –65°C to +150°C  |
| Max Junction Temperature ( $T_J$ )                    | 150°C            |
| Lead Temperature ( $T_L$ )<br>(Soldering, 10 seconds) | 260°C            |
| ESD (Human Body Model)                                | 7500V            |
| ESD (Machine Model)                                   | 400V             |

**Recommended Operating Conditions**

|                                                  |                                                   |
|--------------------------------------------------|---------------------------------------------------|
| Supply Voltage ( $V_{CC}$ )                      | 3.0V to 3.6V                                      |
| Magnitude of Differential Voltage ( $ V_{ID} $ ) | 100 mV to $V_{CC}$                                |
| Common Mode Voltage Range ( $V_{IC}$ )           | (0V + $ V_{ID} /2$ ) to ( $V_{CC} -  V_{ID} /2$ ) |
| Operating Temperature ( $T_A$ )                  | –40°C to +85°C                                    |

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. Fairchild does not recommend operation of circuits outside databook specification.

**DC Electrical Characteristics**

| Symbol          | Parameter                                                                     | Test Conditions                                                                       | Min               | Typ<br>(Note 2) | Max                     | Units   |
|-----------------|-------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|-------------------|-----------------|-------------------------|---------|
| $V_{TH}$        | Differential Input Threshold HIGH                                             | See Figure 1; $V_{IC} = +0.05V, +1.2V$ , or $V_{CC} - 0.05V$                          |                   |                 | 100                     | mV      |
| $V_{TL}$        | Differential Input Threshold LOW                                              | See Figure 1; $V_{IC} = +0.05V, +1.2V$ , or $V_{CC} - 0.05V$                          | –100              |                 |                         | mV      |
| $V_{IH}$        | Input HIGH Voltage ( $\overline{EN}$ or $\overline{EN}$ )                     |                                                                                       | 2.0               |                 | $V_{CC}$                | V       |
| $V_{IL}$        | Input LOW Voltage ( $\overline{EN}$ or $\overline{EN}$ )                      |                                                                                       | GND               |                 | 0.8                     | V       |
| $V_{OD}$        | Output Differential Voltage                                                   | $R_L = 100 \Omega$ , Driver Enabled,<br>See Figure 2                                  | 250               | 330             | 450                     | mV      |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change from Differential LOW-to-HIGH                       |                                                                                       |                   |                 | 25                      | mV      |
| $V_{OS}$        | Offset Voltage                                                                |                                                                                       | 1.125             | 1.23            | 1.375                   | V       |
| $\Delta V_{OS}$ | Offset Magnitude Change from Differential LOW-to-HIGH                         |                                                                                       |                   |                 | 25                      | mV      |
| $I_{OS}$        | Short Circuit Output Current                                                  | $D_{OUT+} = 0V$ and $D_{OUT-} = 0V$ ,<br>Driver Enabled                               |                   | –3.4            | –6                      | mA      |
|                 |                                                                               | $V_{OD} = 0V$ , Driver Enabled                                                        |                   | $\pm 3.4$       | $\pm 6$                 | mA      |
| $I_{IN}$        | Input Current ( $\overline{EN}$ , $\overline{EN}$ , $D_{INX+}$ , $D_{INX-}$ ) | $V_{IN} = 0V$ to $V_{CC}$ , Other Input = $V_{CC}$ or 0V<br>(for Differential Inputs) |                   |                 | $\pm 20$                | $\mu A$ |
| $I_{OFF}$       | Power Off Input or Output Current                                             | $V_{CC} = 0V$ , $V_{IN}$ or $V_{OUT} = 0V$ to 3.6V                                    |                   |                 | $\pm 20$                | $\mu A$ |
| $I_{CCZ}$       | Disabled Power Supply Current                                                 | Drivers Disabled                                                                      |                   | 5.4             | 11                      | mA      |
| $I_{CC}$        | Power Supply Current                                                          | Drivers Enabled, Any Valid Input Condition                                            |                   | 30.4            | 41                      | mA      |
| $I_{OZ}$        | Disabled Output Leakage Current                                               | Driver Disabled, $D_{OUT+} = 0V$ to 3.6V or<br>$D_{OUT-} = 0V$ to 3.6V                |                   |                 | $\pm 20$                | $\mu A$ |
| $V_{IC}$        | Common Mode Voltage Range                                                     | $ V_{ID}  = 100 \text{ mV}$ to $V_{CC}$                                               | $0V +  V_{ID} /2$ |                 | $V_{CC} - ( V_{ID} /2)$ | V       |
| $C_{IN}$        | Input Capacitance                                                             | Enable Input                                                                          |                   | 2.6             |                         | pF      |
|                 |                                                                               | LVDS Input                                                                            |                   | 2.1             |                         |         |
| $C_{OUT}$       | Output Capacitance                                                            |                                                                                       |                   | 2.8             |                         | pF      |
| $V_{BB}$        | Output Reference Voltage                                                      | $V_{CC} = 3.3V$ , $I_{BB} = 0$ to $-275 \mu A$                                        | 1.125             | 1.2             | 1.375                   | V       |

**Note 2:** All typical values are at  $T_A = 25^\circ C$  and with  $V_{CC} = 3.3V$ .

## AC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

| Symbol                         | Parameter                                            | Test Conditions                                                                                                                                                                                         | Min  | Typ<br>(Note 3) | Max  | Units |
|--------------------------------|------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-----------------|------|-------|
| $t_{PLHD}$                     | Differential Output Propagation Delay<br>LOW-to-HIGH | $R_L = 100\ \Omega$ , $C_L = 5\ \text{pF}$ ,<br>$V_{ID} = 200\ \text{mV}$ to $450\ \text{mV}$ ,<br>$V_{IC} =  V_{ID} /2$ to $V_{CC} - ( V_{ID} /2)$ ,<br>Duty Cycle = 50%,<br>See Figure 1 and Figure 3 | 0.75 | 1.1             | 1.75 | ns    |
| $t_{PHLD}$                     | Differential Output Propagation Delay<br>HIGH-to-LOW |                                                                                                                                                                                                         | 0.75 | 1.1             | 1.75 | ns    |
| $t_{TLHD}$                     | Differential Output Rise Time (20% to 80%)           |                                                                                                                                                                                                         | 0.29 | 0.4             | 0.58 | ns    |
| $t_{THLD}$                     | Differential Output Fall Time (80% to 20%)           |                                                                                                                                                                                                         | 0.29 | 0.4             | 0.58 | ns    |
| $t_{SK(P)}$                    | Pulse Skew $ t_{PLH} - t_{PHL} $                     |                                                                                                                                                                                                         |      | 0.02            | 0.2  | ns    |
| $t_{SK(LH)}$ ,<br>$t_{SK(HL)}$ | Channel-to-Channel Skew<br>(Note 4)                  |                                                                                                                                                                                                         |      | 0.02            | 0.15 | ns    |
| $t_{SK(PP)}$                   | Part-to-Part Skew (Note 5)                           |                                                                                                                                                                                                         |      |                 | 0.5  | ns    |
| $f_{MAX}$                      | Maximum Frequency (Note 6)(Note 7)                   |                                                                                                                                                                                                         | 400  | 800             |      | MHz   |
| $t_{PZHD}$                     | Differential Output Enable Time<br>from Z to HIGH    | $R_L = 100\ \Omega$ , $C_L = 5\ \text{pF}$ ,<br>See Figure 2 and Figure 3                                                                                                                               |      | 2.2             | 5    | ns    |
| $t_{PZLD}$                     | Differential Output Enable Time<br>from Z to LOW     |                                                                                                                                                                                                         |      | 2.5             | 5    | ns    |
| $t_{PHZD}$                     | Differential Output Disable Time<br>from HIGH to Z   |                                                                                                                                                                                                         |      | 1.8             | 5    | ns    |
| $t_{PLZD}$                     | Differential Output Disable Time<br>from LOW to Z    |                                                                                                                                                                                                         |      | 2.1             | 5    | ns    |
| $t_{DJ}$                       | LVDS Data Jitter,<br>Deterministic                   | $V_{ID} = 300\ \text{mV}$ , $\text{PRBS} = 2^{23} - 1$ ,<br>$V_{IC} = 1.2\ \text{V}$ at 800 Mbps                                                                                                        |      | 85              | 135  | ps    |
| $t_{RJ}$                       | LVDS Clock Jitter,<br>Random (RMS)                   | $V_{ID} = 300\ \text{mV}$ ,<br>$V_{IC} = 1.2\ \text{V}$ at 400 MHz                                                                                                                                      |      | 2.1             | 3.5  | ps    |

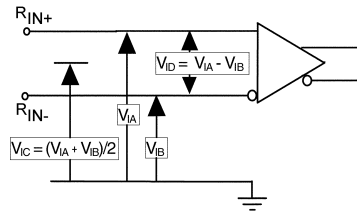
**Note 3:** All typical values are at  $T_A = 25^\circ\text{C}$  and with  $V_{CC} = 3.3\text{V}$ .

**Note 4:**  $t_{SK(LH)}$ ,  $t_{SK(HL)}$  is the skew between specified outputs of a single device when the outputs have identical loads and are switching in the same direction.

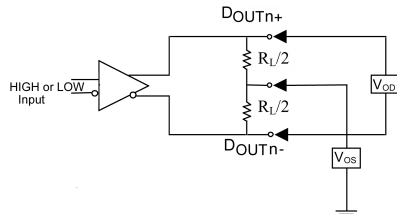
**Note 5:**  $t_{SK(PP)}$  is the magnitude of the difference in propagation delay times between any specified terminals of two devices switching in the same direction (either Low-to-HIGH or HIGH-to-LOW) when both devices operate with the same supply voltage, same temperature, and have identical test circuits.

**Note 6:** Passing criteria for maximum frequency is the output  $V_{OD} > 200\ \text{mV}$  and the duty cycle is 45% to 55% with all channels switching.

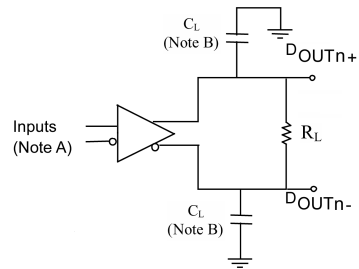
**Note 7:** Output loading is transmission line environment only;  $C_L$  is  $< 1\ \text{pF}$  of stray test fixture capacitance.



**FIGURE 1. Differential Receiver Voltage Definitions and Propagation and Transition Time Test Circuit**



**FIGURE 2. Differential Driver DC Test Circuit**



**Note A:** All LVDS input pulses have frequency = 10 MHz,  $t_R$  or  $t_F < 0.5\ \text{ns}$

**Note B:**  $C_L$  includes all probe and test fixture capacitances

**FIGURE 3. Differential Driver Propagation Delay and Transition Time Test Circuit**

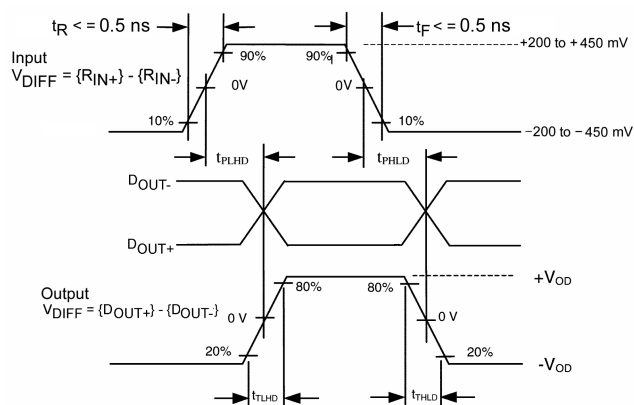
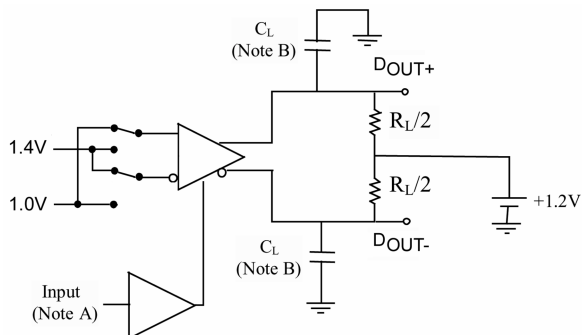


FIGURE 4. AC Waveform



Note A: All LVTTTL input pulses have frequency = 10MHz,  $t_R$  or  $t_F \leq 2$  ns

Note B:  $C_L$  includes all probe and jig capacitances

FIGURE 5. Differential Driver Enable and Disable Circuit

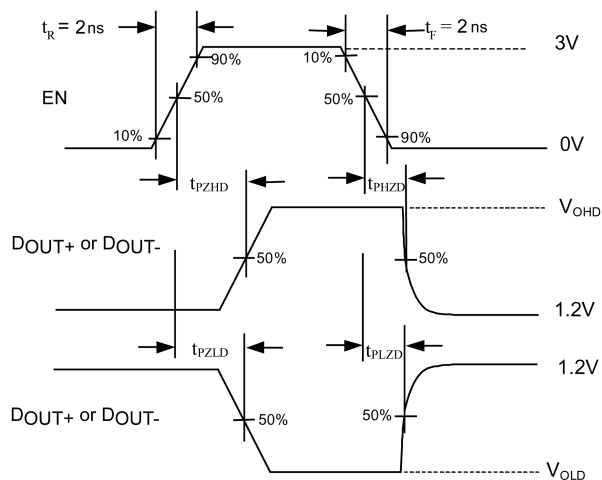
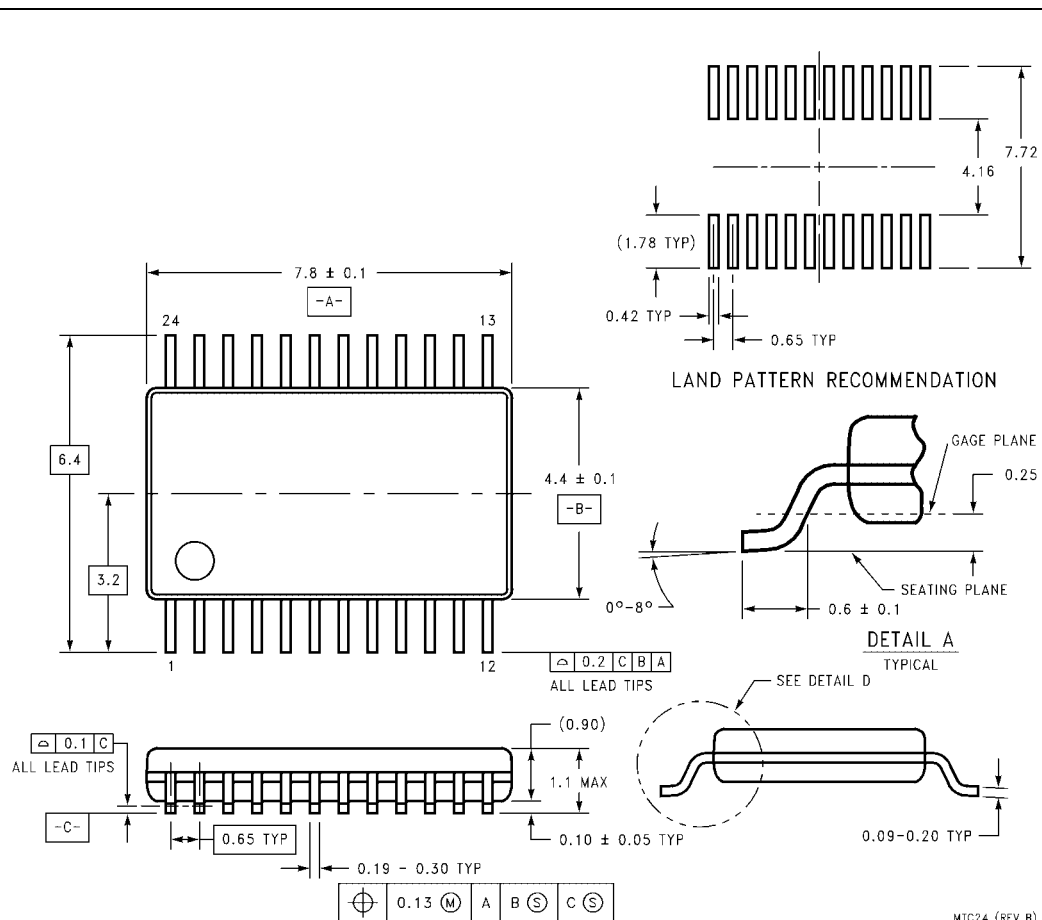


FIGURE 6. Enable and Disable AC Waveforms



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