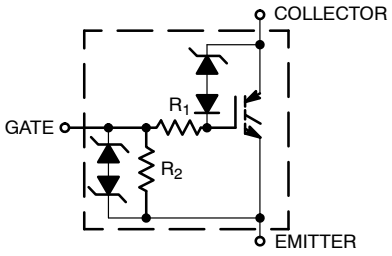
EcoSPARK® 2 N-Channel Ignition IGBT

FGD3325G2-F085V

330 mJ, 250 V

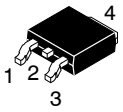


Features

- SCIS Energy = 330 mJ at T_J = 25 °C
- Logic Level Gate Drive
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Automotive Ignition Coil Driver Circuits
- Coil On Plug Applications



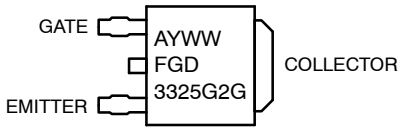
DPAK (SINGLE GAUGE)
CASE 369C

MAXIMUM RATINGS (T_A = 25 °C unless otherwise stated)

Symbol	Parameter	Value	Unit
BV_{CER}	Collector to Emitter Breakdown Voltage (I_C = 1 mA)	250	V
BV_{ECS}	Emitter to Collector Voltage – Reverse Battery Condition (I_C = 10 mA)	28	V
E_{SCIS25}	I_{SCIS} = 14.8 A, L = 3.0 mHy, R_{GE} = 1 KΩ, T_C = 25 °C	330	mJ
$E_{SCIS150}$	I_{SCIS} = 11.4 A, L = 3.0 mHy, R_{GE} = 1 KΩ, T_C = 150 °C	195	mJ
I_{C25}	Collector Current Continuous at V_{GE} = 5.0 V, T_C = 25 °C	41	A
I_{C110}	Collector Current Continuous at V_{GE} = 5.0 V, T_C = 110 °C	25	A
V_{GEM}	Gate to Emitter Voltage Continuous	±10	V
P_D	Power Dissipation Total, T_C = 25 °C	150	W
	Power Dissipation Derating, T_C > 25 °C	1.0	W/°C
T_J, T_{STG}	Operating Junction and Storage Temperature Range	−55 to +175	°C
T_L	Max. Lead Temperature for Soldering (Leads at 1.6 mm from case for 10 s)	300	°C
T_{PKG}	Reflow Soldering according to JESD020C	260	°C
ESD	HBM−Electrostatic Discharge Voltage at 100 pF, 1500 Ω	4	kV
	CDM−Electrostatic Discharge Voltage at 1 Ω	2	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
FGD3325G2 = Device Code
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
OFF STATE CHARACTERISTICS							
BV_{CER}	Collector to Emitter Breakdown Voltage	I_{CE} = 2 mA, V_{GE} = 0 V, R_{GE} = 1 kΩ, T_J = −40 to 150 °C		225	–	275	V
BV_{CES}	Collector to Emitter Breakdown Voltage	I_{CE} = 10 mA, V_{GE} = 0 V, R_{GE} = 0, T_J = −40 to 150 °C		240	–	290	V
BV_{ECS}	Emitter to Collector Breakdown Voltage	I_{CE} = −75 mA, V_{GE} = 0 V, T_J = 25 °C		28	–	–	V
BV_{GES}	Gate to Emitter Breakdown Voltage	I_{GES} = ±2 mA		±12	±14	–	V
I_{CER}	Collector to Emitter Leakage Current	V_{CE} = 175 V, R_{GE} = 1 kΩ	T_J = 25 °C	–	–	25	μA
			T_J = 150 °C	–	–	1	
I_{ECS}	Emitter to Collector Leakage Current	V_{EC} = 24 V	T_J = 25 °C	–	–	1	mA
			T_J = 150 °C	–	–	40	
R_1	Series Gate Resistance			–	120	–	Ω
R_2	Gate to Emitter Resistance			10K	–	30K	Ω
ON STATE CHARACTERISTICS							
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	I_{CE} = 6 A, V_{GE} = 4 V, T_J = 25 °C		–	1.15	1.25	V
		I_{CE} = 10 A, V_{GE} = 4.5 V, T_J = 150 °C		–	1.35	1.50	
		I_{CE} = 15 A, V_{GE} = 4.5 V, T_J = 150 °C		–	1.68	1.85	
DYNAMIC CHARACTERISTICS							
$Q_{G(ON)}$	Gate Charge	I_{CE} = 10 A, V_{CE} = 12 V, V_{GE} = 5 V		–	21	–	nC
$V_{GE(TH)}$	Gate to Emitter Threshold Voltage	I_{CE} = 1 mA, V_{CE} = V_{GE}	T_J = 25 °C	1.3	1.5	2.2	V
			T_J = 150 °C	0.75	1.1	1.8	
V_{GEP}	Gate to Emitter Plateau Voltage	V_{CE} = 12 V, I_{CE} = 10 A		–	2.7	–	V
SWITCHING CHARACTERISTICS							
$t_{d(ON)R}$	Current Turn-On Delay Time-Resistive	V_{CE} = 14 V, R_L = 1 Ω, V_{GE} = 5 V, R_G = 1 KΩ, T_J = 25 °C		–	0.8	4	μs
t_{rR}	Current Rise Time-Resistive			–	1.2	7	
$t_{d(OFF)L}$	Current Turn-Off Delay Time-Inductive	V_{CE} = 190 V, L = 1 mH, V_{GE} = 5 V, R_G = 1 KΩ, I_{CE} = 6.5 A, T_J = 25 °C		–	5.1	15	
t_{fL}	Current Fall Time-Inductive			–	2.2	15	
THERMAL CHARACTERISTICS							
$R_{\theta JC}$	Thermal Resistance Junction to Case			–	–	1	°C/W

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Diameter	Tape Width	Shipping†
FGD3325G2	FGD3325G2-F085V	DPAK (Pb-Free)	330 mm	16 mm	2500 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

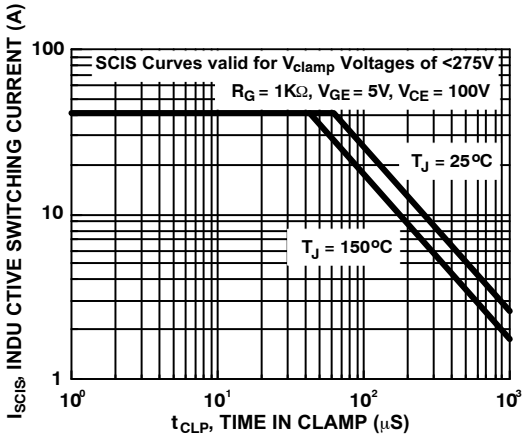


Figure 1. Self Clamped Inductive Switching Current vs. Time in Clamp

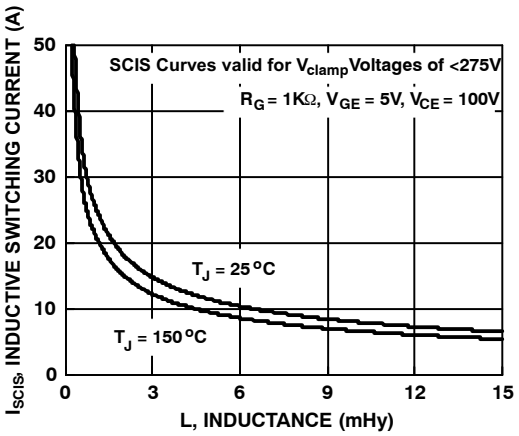


Figure 2. Self Clamped Inductive Switching Current vs. Inductance

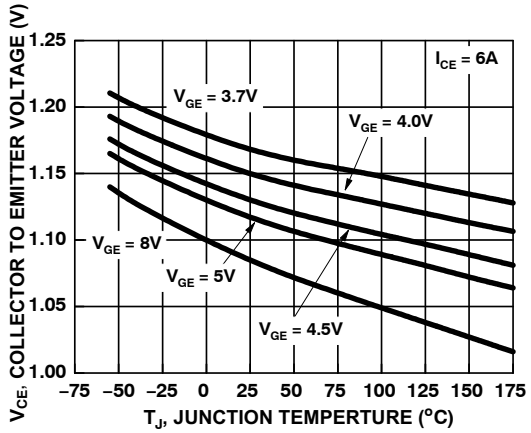


Figure 3. Collector to Emitter On-State Voltage vs. Junction Temperature

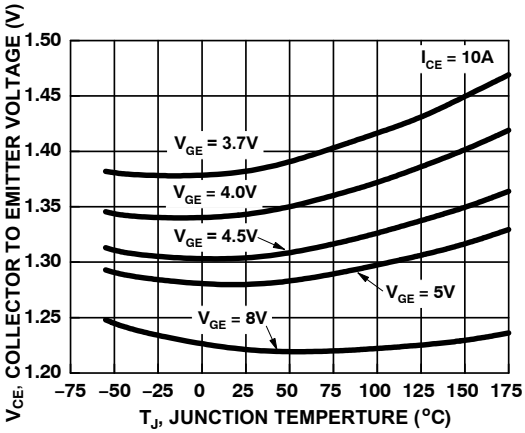


Figure 4. Collector to Emitter On-State Voltage vs. Junction Temperature

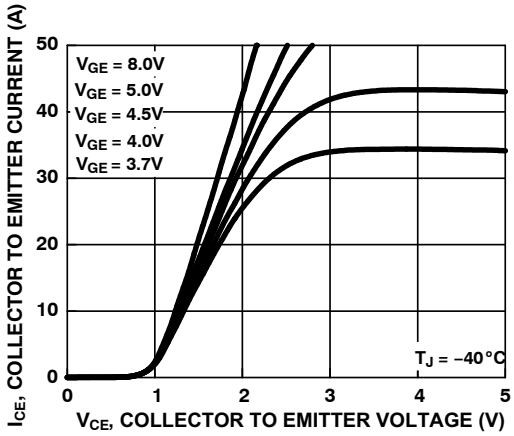


Figure 5. Collector to Emitter On-State Voltage vs. Collector Current

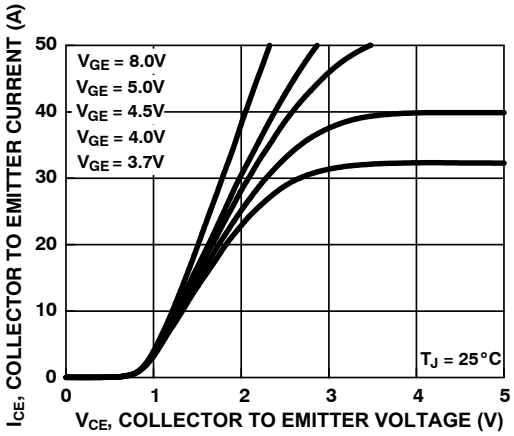


Figure 6. Collector to Emitter On-State Voltage vs. Collector Current

TYPICAL CHARACTERISTICS

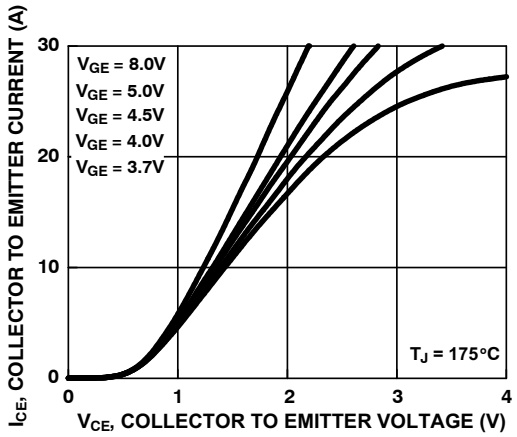


Figure 7. Collector to Emitter On-State Voltage vs. Collector Current

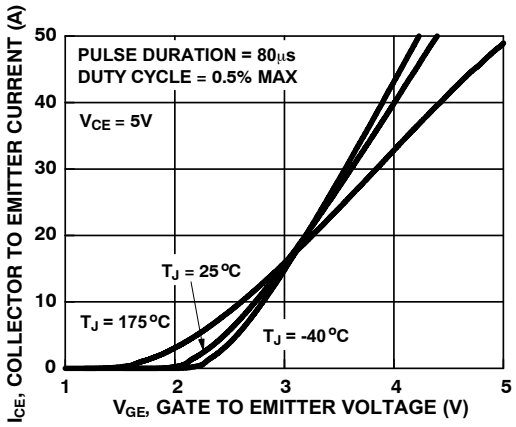


Figure 8. Transfer Characteristics

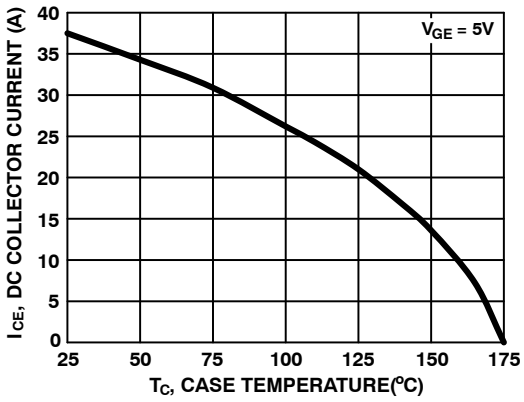


Figure 9. DC Collector Current vs. Case Temperature

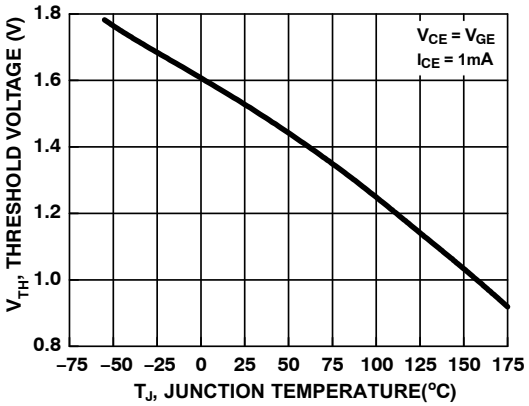


Figure 10. Threshold Voltage vs. Junction Temperature

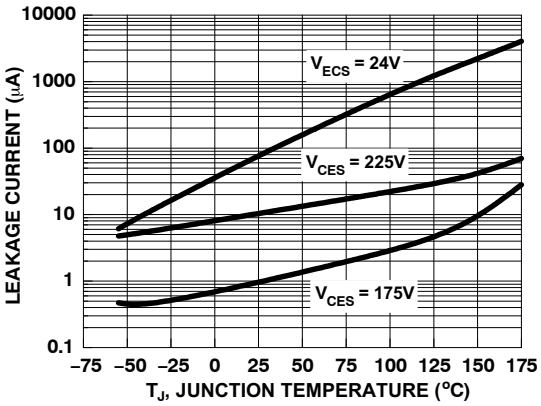


Figure 11. Leakage Current vs. Junction Temperature

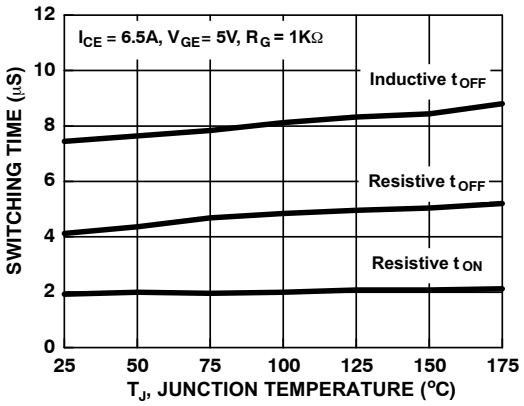


Figure 12. Switching Time vs. Junction Temperature

TYPICAL CHARACTERISTICS

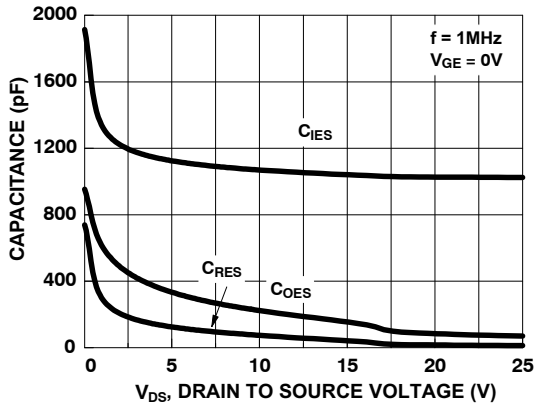


Figure 13. Capacitance vs. Collector to Emitter

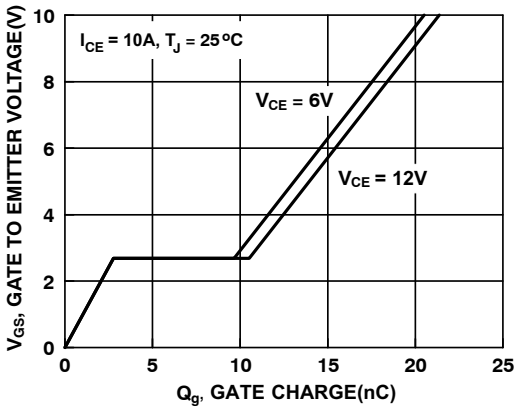


Figure 14. Gate Charge

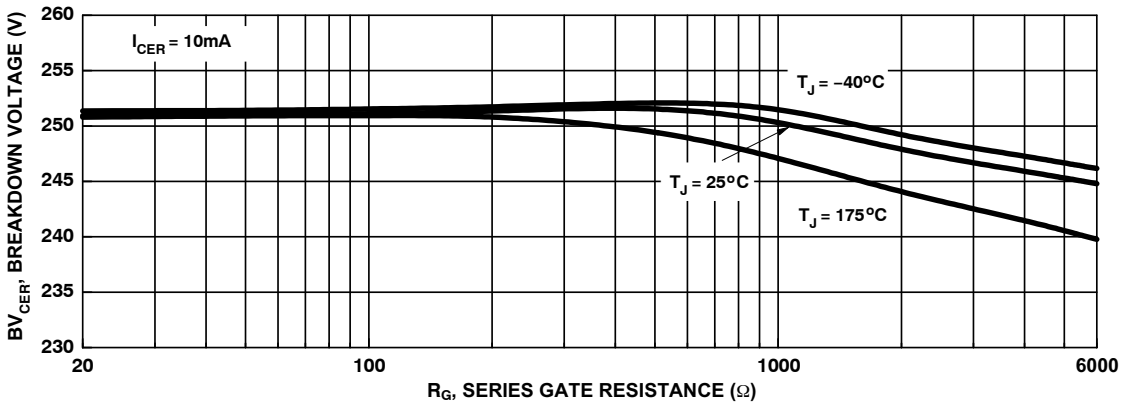


Figure 15. Break Down Voltage vs. Series Gate Resistance

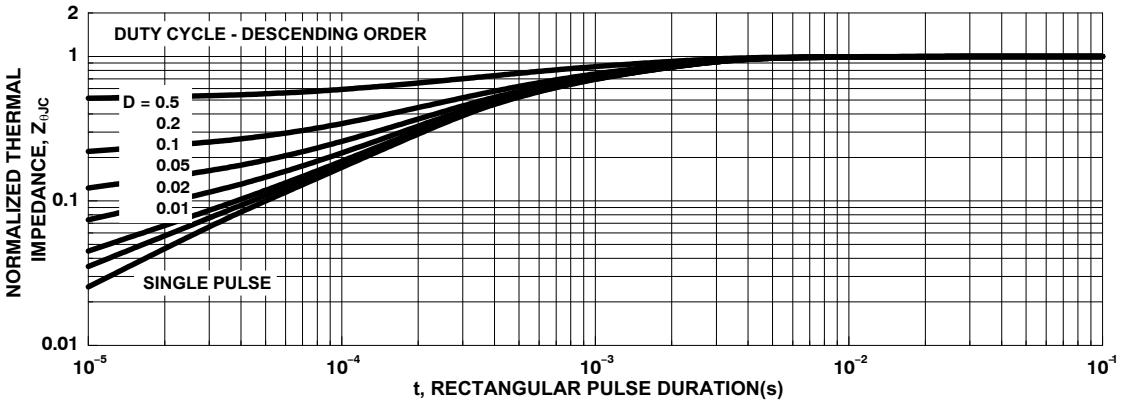


Figure 16. IGBT Normalized Transient Thermal Impedance, Junction to Case

TYPICAL CHARACTERISTICS

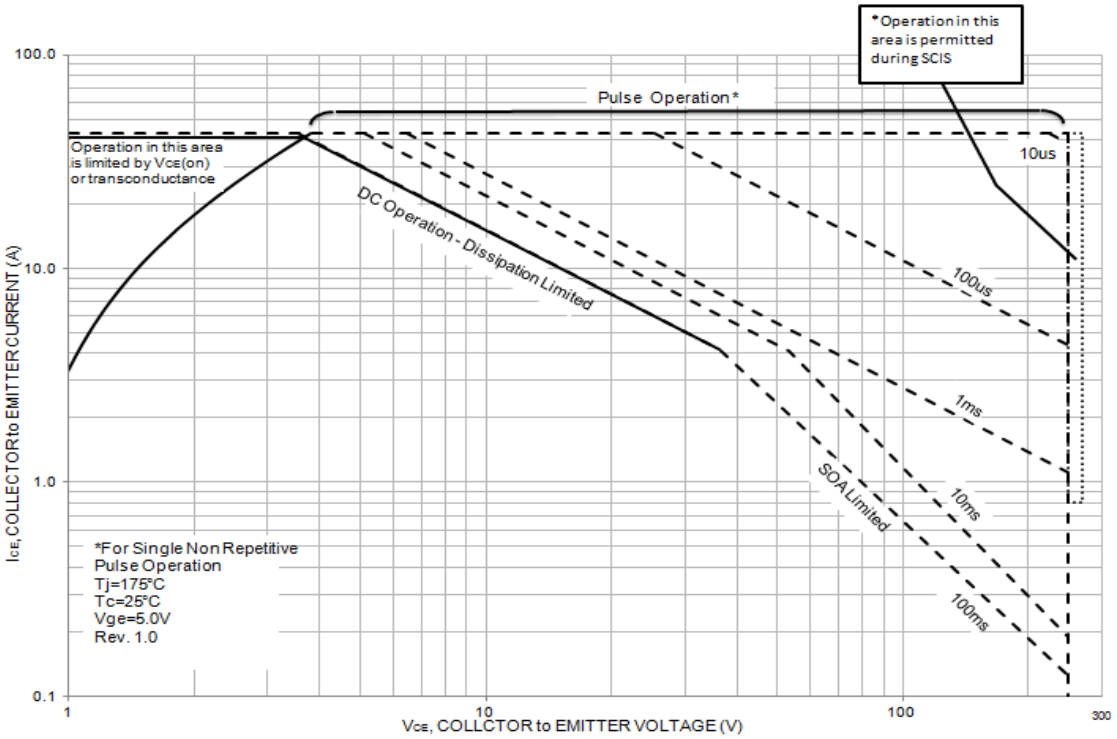


Figure 17. Forward Safe Operating Area

TEST CIRCUIT AND WAVEFORMS

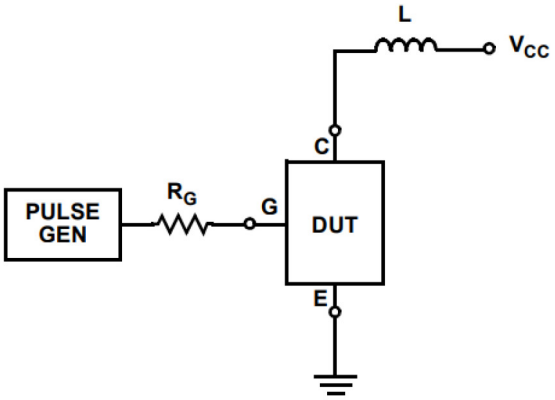


Figure 18. Inductive Switching Test Circuit

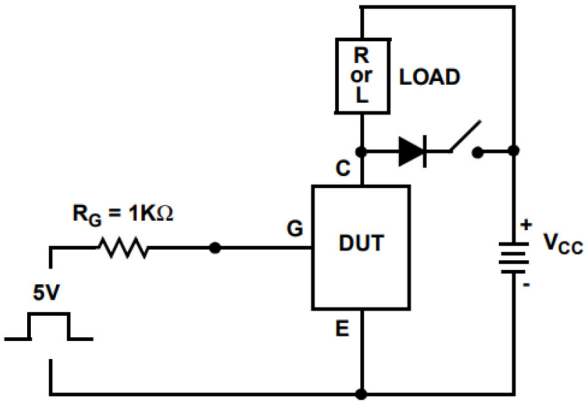


Figure 19. t_{ON} and t_{OFF} Switching Test Circuit

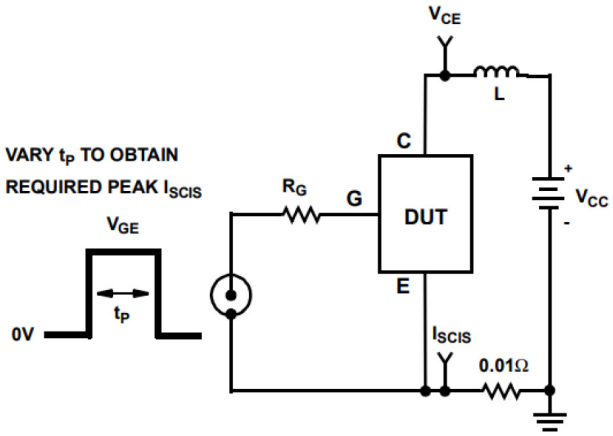


Figure 20. Energy Test Circuit

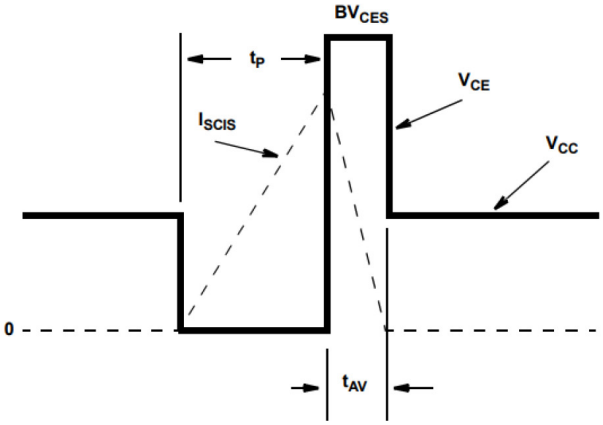
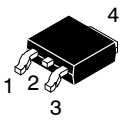


Figure 21. Energy Waveforms

REVISION HISTORY

Revision	Description of Changes	Date
1	Rebranded the Data Sheet to onsemi format	9/15/2025

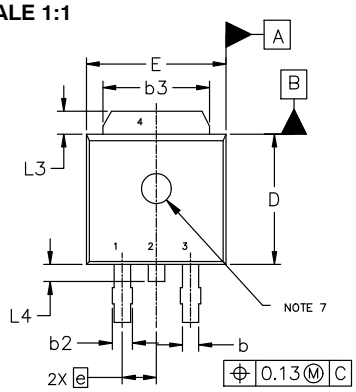
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



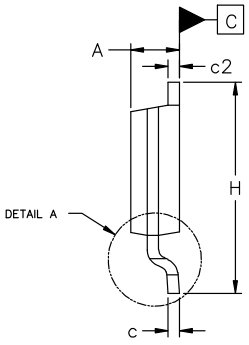
SCALE 1:1

DPAK3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE J

DATE 12 AUG 2025

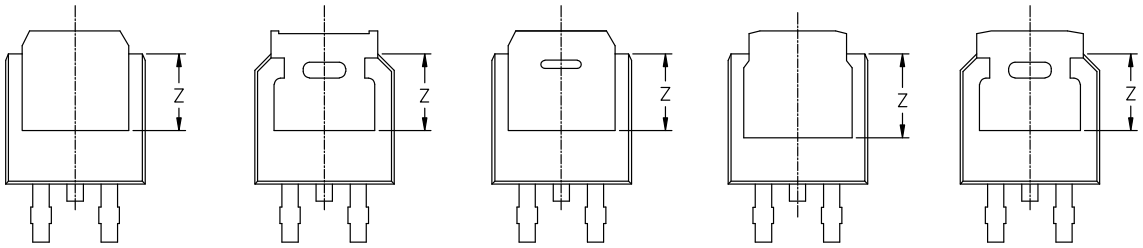


TOP VIEW



SIDE VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.18	2.28	2.38
A1	0.00	---	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	---	1.27
L4	---	---	1.01
Z	3.93	---	---

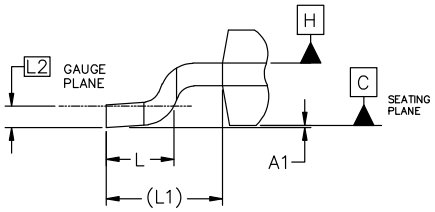


BOTTOM VIEW

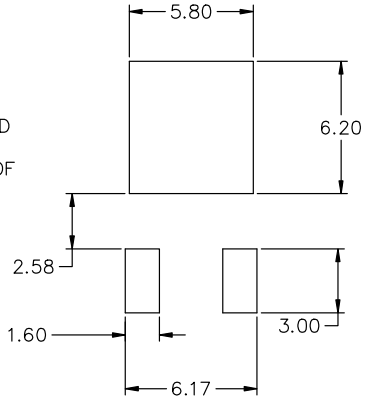
ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.



DETAIL A
ROTATED 90° CW



RECOMMENDED MOUNTING FOOTPRINT*

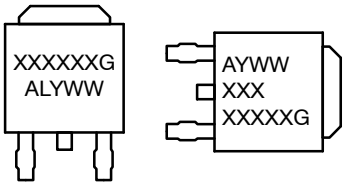
*FOR ADDITIONAL INFORMATION ON OUR PB–FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON10527D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**DPAK3 6.10x6.54x2.28, 2.29P**	**PAGE 1 OF 2**

DPAK3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE J

DATE 12 AUG 2025

GENERIC MARKING DIAGRAM*



IC **Discrete**

XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales